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CAVCH4T245MRSVREP

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TEXAS INSTRUMENTS

SN74AVCH4T245-EP

4-BIT DUAL-SUPPLY BUS TRANSCEIVER
# WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

FEATURES

- **Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage**
- **Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2-V to 3.6-V Power-Supply Range**
- **I/Os Are 4.6-V Tolerant**
- **I_{off} Supports Partial Power-Down-Mode Operation**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Max Data Rates**
    - **380 Mbps (1.8-V to 3.3-V Translation)**
    - **200 Mbps (<1.8-V to 3.3-V Translation)**
    - **200 Mbps (Translate to 2.5 V or 1.8 V)**
    - **150 Mbps (Translate to 1.5 V)**
    - **100 Mbps (Translate to 1.2 V)**

- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
    - **8000-V Human-Body Model (A114-A)**
    - **200-V Machine Model (A115-A)**
    - **1000-V Charged-Device Model (C101)**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range**[1]
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(1) Additional temperature ranges are available – contact factory

RSV PACKAGE
(TOP VIEW)
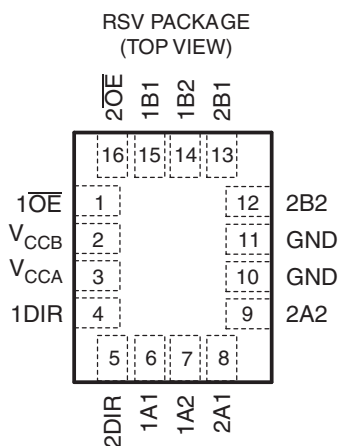
DESCRIPTION/ORDERING INFORMATION

This 4-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. The SN74AVCH4T245 is optimized to operate with V_{CCA}/V_{CCB} set at 1.4 V to 3.6 V. It is operational with V_{CCA}/V_{CCB} as low as 1.2 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The SN74AVCH4T245 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable ($\overline{\text{OE}}$) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

The SN74AVCH4T245 is designed so that the control pins (1DIR, 2DIR, 1$\overline{\text{OE}}$, and 2$\overline{\text{OE}}$) are supplied by V_{CCA}.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, then both ports are in the high-impedance state. The bus-hold circuitry on the powered-up side always stays active.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION[1]

T_A	PACKAGE[2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−55°C to 125°C	QFN – RSV	Tape and reel	CAVCH4T245MRSVREP	SODM

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLE[1]
(EACH 2-BIT SECTION)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{\text{OE}}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os are always active.

LOGIC DIAGRAM (POSITIVE LOGIC) FOR 1/2 OF AVCH4T245

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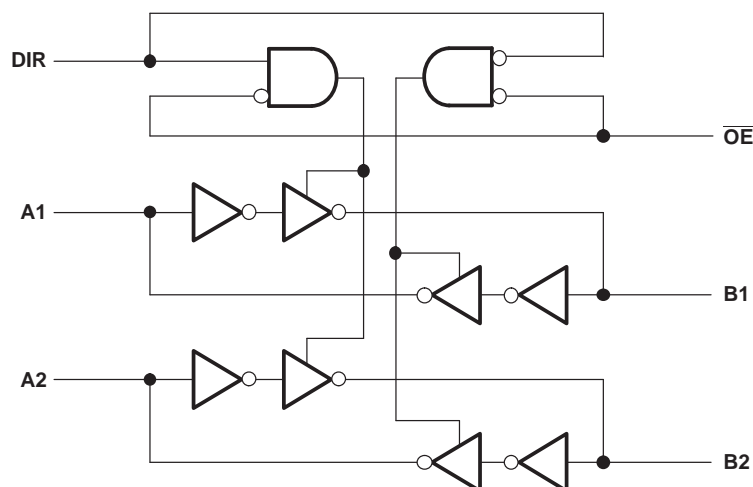
Absolute Maximum Ratings[(1)]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage range		−0.5	4.6	V
V_I	Input voltage range[(2)]	I/O ports (A port)	−0.5	4.6	V
		I/O ports (B port)	−0.5	4.6	
		Control inputs	−0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state[(2)]	A port	−0.5	4.6	V
		B port	−0.5	4.6	
V_O	Voltage range applied to any output in the high or low state[(2)(3)]	A port	−0.5	V_{CCA} + 0.5	V
		B port	−0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	$V_I < 0$		−50	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
θ_{JA}	Package thermal impedance			184	°C/W
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

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Recommended Operating Conditions[1][2][3][4][5]

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}	Supply voltage				1.2	3.6	V
V_{IH}	High-level input voltage	Data inputs[4]	1.2 V to 1.95 V		$V_{CCI} \times 0.65$		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Data inputs[4]	1.2 V to 1.95 V			$V_{CCI} \times 0.35$	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA})[5]	1.2 V to 1.95 V		$V_{CCA} \times 0.65$		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA})[5]	1.2 V to 1.95 V			$V_{CCA} \times 0.35$	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.2 V		−3	mA
				1.4 V to 1.6 V		−6	
				1.65 V to 1.95 V		−8	
				2.3 V to 2.7 V		−9	
				3 V to 3.6 V		−12	
I_{OL}	Low-level output current			1.2 V		3	mA
				1.4 V to 1.6 V		6	
				1.65 V to 1.95 V		8	
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				−55	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = $V_{CCI} \times 0.7$ V, V_{IL} max = $V_{CCI} \times 0.3$ V.
(5) For V_{CCA} values not specified in the data sheet, V_{IH} min = $V_{CCA} \times 0.7$ V, V_{IL} max = $V_{CCA} \times 0.3$ V.

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Electrical Characteristics[1][2]

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	$T_A = 25°C$			−55°C to 125°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
V_{OH}		$I_{OH} = -100$ µA	$V_I = V_{IH}$	1.2 V to 3.6 V	1.2 V to 3.6 V				$V_{CCO} - 0.2$		V
		$I_{OH} = -3$ mA		1.2 V	1.2 V		0.95				
		$I_{OH} = -6$ mA		1.4 V	1.4 V				1.05		
		$I_{OH} = -8$ mA		1.65 V	1.65 V				1.2		
		$I_{OH} = -9$ mA		2.3 V	2.3 V				1.75		
		$I_{OH} = -12$ mA		3 V	3 V				2.3		
V_{OL}		$I_{OL} = 100$ µA	$V_I = V_{IL}$	1.2 V to 3.6 V	1.2 V to 3.6 V					0.2	V
		$I_{OL} = 3$ mA		1.2 V	1.2 V		0.15				
		$I_{OL} = 6$ mA		1.4 V	1.4 V					0.35	
		$I_{OL} = 8$ mA		1.65 V	1.65 V					0.45	
		$I_{OL} = 9$ mA		2.3 V	2.3 V					0.55	
		$I_{OL} = 12$ mA		3 V	3 V					0.7	
I_I	DIR input	$V_I = V_{CCA}$ or GND		1.2 V to 3.6 V	1.2 V to 3.6 V	±0.025		±0.25		±1	µA
I_{BHL}[3]		$V_I = 0.42$ V		1.2 V	1.2 V	25					µA
		$V_I = 0.49$ V		1.4 V	1.4 V				15		
		$V_I = 0.58$ V		1.65 V	1.65 V				25		
		$V_I = 0.7$ V		2.3 V	2.3 V				45		
		$V_I = 0.8$ V		3.3 V	3.3 V				100		
I_{BHH}[4]		$V_I = 0.78$ V		1.2 V	1.2 V	−25					µA
		$V_I = 0.91$ V		1.4 V	1.4 V				−15		
		$V_I = 1.07$ V		1.65 V	1.65 V				−25		
		$V_I = 1.6$ V		2.3 V	2.3 V				−45		
		$V_I = 2$ V		3.3 V	3.3 V				−100		
I_{BHLO}[5]		$V_I = 0$ to V_{CCI}		1.2 V	1.2 V	50					µA
				1.6 V	1.6 V				125		
				1.95 V	1.95 V				200		
				2.7 V	2.7 V				300		
				3.6 V	3.6 V				500		
I_{BHHO}[6]		$V_I = 0$ to V_{CCI}		1.2 V	1.2 V	−50					µA
				1.6 V	1.6 V				−125		
				1.95 V	1.95 V				−200		
				2.7 V	2.7 V				−300		
				3.6 V	3.6 V				−500		

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.
(3) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.
(4) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.
(5) An external driver must source at least I_{BHLO} to switch this node from low to high.
(6) An external driver must sink at least I_{BHHO} to switch this node from high to low.

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Electrical Characteristics[(1)(2)]

over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	$T_A = 25°C$			−55°C to 125°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
I_{off}	A port	V_I or V_O = 0 to 3.6 V		0 V	0 V to 3.6 V		±0.1	±1		±13	μA
	B port			0 V to 3.6 V	0 V		±0.1	±1		±13	
I_{OZ}[(3)]	A or B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND	$\overline{OE} = V_{IH}$	3.6 V	3.6 V		±0.5	±2.5		±5	μA
	B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND	$\overline{OE}$ = don't care	0 V	3.6 V					±14	
	A port			3.6 V	0 V					±5	
I_{CCA}		$V_I = V_{CCI}$ or GND, $I_O = 0$		1.2 V to 3.6 V	1.2 V to 3.6 V					8	μA
				0 V	3.6 V					−2	
				3.6 V	0 V					8	
I_{CCB}		$V_I = V_{CCI}$ or GND, $I_O = 0$		1.2 V to 3.6 V	1.2 V to 3.6 V					8	μA
				0 V	3.6 V					8	
				3.6 V	0 V					−2	
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND, $I_O = 0$		1.2 V to 3.6 V	1.2 V to 3.6 V					16	μA
C_i	Control inputs	V_I = 3.3 V or GND		3.3 V	3.3 V		3.5			4.5	pF
C_{io}	A or B port	V_O = 3.3 V or GND		3.3 V	3.3 V		6			7	pF

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 1.2 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V	V_{CCB} = 1.8 V ± 0.15 V	V_{CCB} = 2.5 V ± 0.2 V	V_{CCB} = 3.3 V ± 0.3 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
t_{PLH}	A	B	3.4	2.9	2.7	2.6	2.8	ns
t_{PHL}			3.4	2.9	2.7	2.6	2.8	
t_{PLH}	B	A	3.6	3.1	2.8	2.6	2.6	ns
t_{PHL}			3.6	3.1	2.8	2.6	2.6	
t_{PZH}	$\overline{OE}$	A	5.6	4.7	4.3	3.9	3.7	ns
t_{PZL}			5.6	4.7	4.3	3.9	3.7	
t_{PZH}	$\overline{OE}$	B	5	4.3	3.9	3.6	3.6	ns
t_{PZL}			5	4.3	3.9	3.6	3.6	
t_{PHZ}	$\overline{OE}$	A	6.2	5.2	5.2	4.3	4.8	ns
t_{PLZ}			6.2	5.2	5.2	4.3	4.8	
t_{PHZ}	$\overline{OE}$	B	5.9	5.1	5	4.7	5.5	ns
t_{PLZ}			5.9	5.1	5	4.7	5.5	

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Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3.2	0.3	10.3	0.3	9.2	0.4	8.2	0.4	8.2	ns
t_{PHL}			3.2	0.3	10.3	0.3	9.2	0.4	8.2	0.4	8.2	
t_{PLH}	B	A	3.3	0.7	10.3	0.5	10	0.4	9.7	0.3	9.6	ns
t_{PHL}			3.3	0.7	10.3	0.5	10	0.4	9.7	0.3	13.6	
t_{PZH}	$\overline{OE}$	A	4.9	1.4	13.6	1.1	13.5	0.7	13.4	0.4	13.4	ns
t_{PZL}			4.9	1.4	13.6	1.1	13.5	0.7	13.4	0.4	13.4	
t_{PZH}	$\overline{OE}$	B	4.5	1.4	14.6	1.1	11.7	0.9	9.8	0.9	9.6	ns
t_{PZL}			4.5	1.4	14.6	1.1	11.7	0.9	9.8	0.9	9.6	
t_{PHZ}	$\overline{OE}$	A	5.6	1.8	14.2	1.5	14.2	1.3	14.2	1.6	14.2	ns
t_{PLZ}			5.6	1.8	14.2	1.5	14.2	1.3	14.2	1.6	14.2	
t_{PHZ}	$\overline{OE}$	B	5.2	1.9	14.3	1.9	13.1	1.4	11.4	1.2	11.6	ns
t_{PLZ}			5.2	1.9	14.3	1.9	13.1	1.4	11.4	1.2	11.6	

Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.9	0.1	10	0.1	8.9	0.1	7.9	0.3	7.9	ns
t_{PHL}			2.9	0.1	10	0.1	8.9	0.1	7.9	0.3	7.9	
t_{PLH}	B	A	3	0.6	9.3	0.5	8.9	0.3	8.6	0.3	8.5	ns
t_{PHL}			3	0.6	9.3	0.5	8.9	0.3	8.6	0.3	8.5	
t_{PZH}	$\overline{OE}$	A	4.4	1	13.4	1	11.3	0.6	11.3	0.4	11.2	ns
t_{PZL}			4.4	1	13.4	1	11.3	0.6	11.3	0.4	11.2	
t_{PZH}	$\overline{OE}$	B	4.1	1.2	14.4	1	12.4	0.8	9.3	0.8	8.6	ns
t_{PZL}			4.1	1.2	14.4	1	12.4	0.8	9.3	0.8	8.6	
t_{PHZ}	$\overline{OE}$	A	5.4	1.6	12.6	1.8	12.7	1.3	12.7	1.6	12.7	ns
t_{PLZ}			5.4	1.6	12.6	1.8	12.7	1.3	12.7	1.6	12.7	
t_{PHZ}	$\overline{OE}$	B	5	1.7	13.9	1.6	12.7	1.2	10.9	1	10.9	ns
t_{PLZ}			5	1.7	13.9	1.6	12.7	1.2	10.9	1	10.9	

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Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA} = 2.5$ V ± 0.2 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V TYP	V_{CCB} = 1.5 V ± 0.1 V MIN	MAX	V_{CCB} = 1.8 V ± 0.15 V MIN	MAX	V_{CCB} = 2.5 V ± 0.2 V MIN	MAX	V_{CCB} = 3.3 V ± 0.3 V MIN	MAX	UNIT
t_{PLH}	A	B	2.8	0.1	9.7	0.1	8.6	0.2	7.5	0.1	7.6	ns
t_{PHL}	A	B	2.8	0.1	9.7	0.1	8.6	0.2	7.5	0.1	7.6	ns
t_{PLH}	B	A	2.7	0.6	8.2	0.4	7.9	0.2	7.4	0.2	7.3	ns
t_{PHL}	B	A	2.7	0.6	8.2	0.4	7.9	0.2	7.4	0.2	7.3	ns
t_{PZH}	$\overline{OE}$	A	4	0.7	10.5	0.7	9.2	0.6	8.8	0.4	8.8	ns
t_{PZL}	$\overline{OE}$	A	4	0.7	10.5	0.7	9.2	0.6	8.8	0.4	8.8	ns
t_{PZH}	$\overline{OE}$	B	3.8	0.9	14.8	0.8	12	0.6	9.8	0.6	9	ns
t_{PZL}	$\overline{OE}$	B	3.8	0.9	14.8	0.8	12	0.6	9.8	0.6	9	ns
t_{PHZ}	$\overline{OE}$	A	4.7	1	12.4	1	12.4	1	10.2	1	10.6	ns
t_{PLZ}	$\overline{OE}$	A	4.7	1	12.4	1	12.4	1	10.2	1	10.6	ns
t_{PHZ}	$\overline{OE}$	B	4.5	1.5	13.4	1.3	12.2	1.1	10.2	0.9	9.2	ns
t_{PLZ}	$\overline{OE}$	B	4.5	1.5	12.8	1.3	12.2	1.1	10.2	0.9	9.2	ns

Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA} = 3.3$ V ± 0.3 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V TYP	V_{CCB} = 1.5 V ± 0.1 V MIN	MAX	V_{CCB} = 1.8 V ± 0.15 V MIN	MAX	V_{CCB} = 2.5 V ± 0.2 V MIN	MAX	V_{CCB} = 3.3 V ± 0.3 V MIN	MAX	UNIT
t_{PLH}	A	B	2.9	0.1	9.6	0.1	8.5	0.1	7.3	0.1	6.9	ns
t_{PHL}	A	B	2.9	0.1	9.6	0.1	8.5	0.1	7.3	0.1	6.9	ns
t_{PLH}	B	A	2.6	0.6	8.2	0.4	7.4	0.2	7	0.1	6.8	ns
t_{PHL}	B	A	2.6	0.6	8.2	0.4	7.4	0.2	7	0.1	6.8	ns
t_{PZH}	$\overline{OE}$	A	3.8	0.6	12.7	0.6	9.2	0.6	7.8	0.4	7.8	ns
t_{PZL}	$\overline{OE}$	A	3.8	0.6	12.7	0.6	9.2	0.6	7.8	0.4	7.8	ns
t_{PZH}	$\overline{OE}$	B	3.7	0.8	14.7	0.6	11.8	0.5	9.7	0.5	8.8	ns
t_{PZL}	$\overline{OE}$	B	3.7	0.8	14.7	0.6	11.8	0.5	9.7	0.5	8.8	ns
t_{PHZ}	$\overline{OE}$	A	4.8	0.7	13.3	0.7	12.3	0.7	9.6	0.7	10.6	ns
t_{PLZ}	$\overline{OE}$	A	4.8	0.7	13.3	0.7	12.3	0.7	9.6	0.7	10.6	ns
t_{PHZ}	$\overline{OE}$	B	5.3	1.4	13.3	1.2	12.1	1	10.4	0.8	10.2	ns
t_{PLZ}	$\overline{OE}$	B	5.3	1.4	13.3	1.2	12.1	1	10.4	0.8	10.2	ns

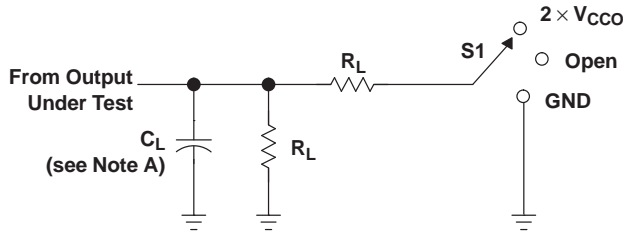Product Folder Link(s): *SN74AVCH4T245-EP*

Operating Characteristics

$T_A = 25°C$

PARAMETER			TEST CONDITIONS	$V_{CCA} = V_{CCB} = 1.2$ V	$V_{CCA} = V_{CCB} = 1.5$ V	$V_{CCA} = V_{CCB} = 1.8$ V	$V_{CCA} = V_{CCB} = 2.5$ V	$V_{CCA} = V_{CCB} = 3.3$ V	UNIT
				TYP	TYP	TYP	TYP	TYP	
C_{pdA}[1]	A to B	Outputs enabled	$C_L = 0$, f = 10 MHz, $t_r = t_f = 1$ ns	1	1	1	1.5	2	pF
		Outputs disabled		1	1	1	1	1	
	B to A	Outputs enabled		12	12.5	13	14	15	
		Outputs disabled		1	1	1	1	1	
C_{pdB}[1]	A to B	Outputs enabled	$C_L = 0$, f = 10 MHz, $t_r = t_f = 1$ ns	12	12.5	13	14	15	pF
		Outputs disabled		1	1	1	1	1	
	B to A	Outputs enabled		1	1	1	1	2	
		Outputs disabled		1	1	1	1	1	

(1) Power dissipation capacitance per transceiver

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SN74AVCH4T245-EP

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PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V
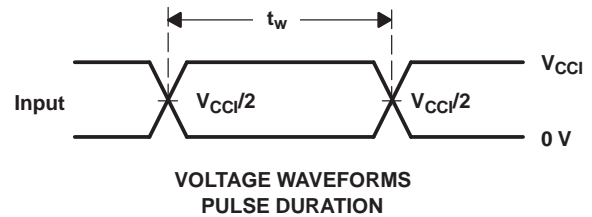
VOLTAGE WAVEFORMS
PULSE DURATION
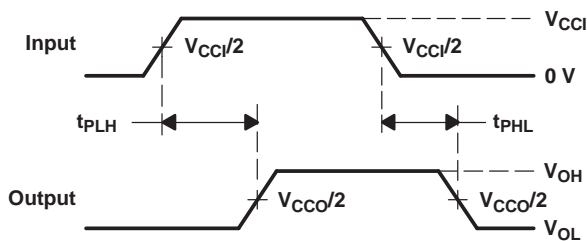
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
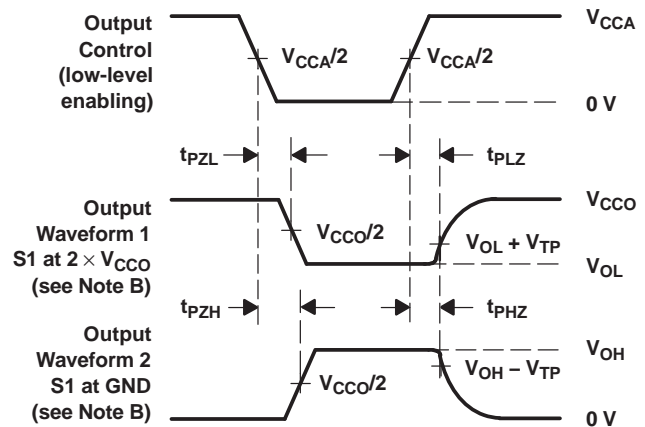
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns,
   dv/dt ≥1 V/ns.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 F. t_{PZL} and t_{PZH} are the same as t_{en}.
 G. t_{PLH} and t_{PHL} are the same as t_{pd}.
 H. V_{CCI} is the V_{CC} associated with the input port.
 I. V_{CCO} is the V_{CC} associated with the output port.

Figure 1. Load Circuit and Voltage Waveforms

Product Folder Link(s): *SN74AVCH4T245-EP*

PACKAGE OPTION ADDENDUM

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CAVCH4T245MRSVREP	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	SODM	Samples
V62/09618-01XE	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	SODM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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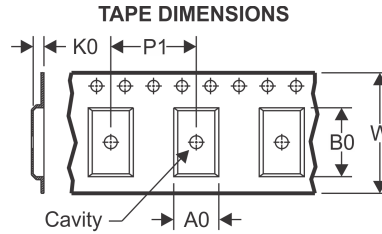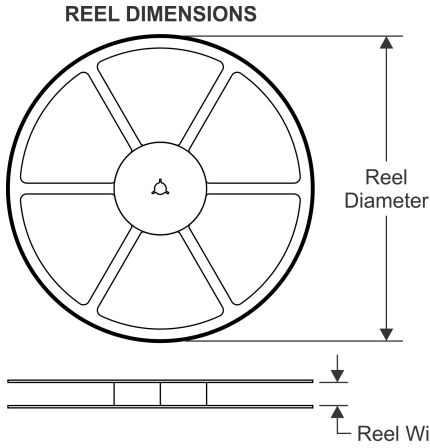
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NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

Cavity

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

User Direction of Feed

Pocket Quadrants
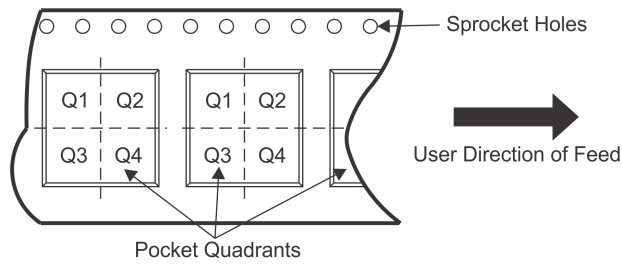
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CAVCH4T245MRSVREP	UQFN	RSV	16	3000	180.0	12.4	2.1	2.9	0.75	4.0	12.0	Q1

Pack Materials-Page 1

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TAPE AND REEL BOX DIMENSIONS
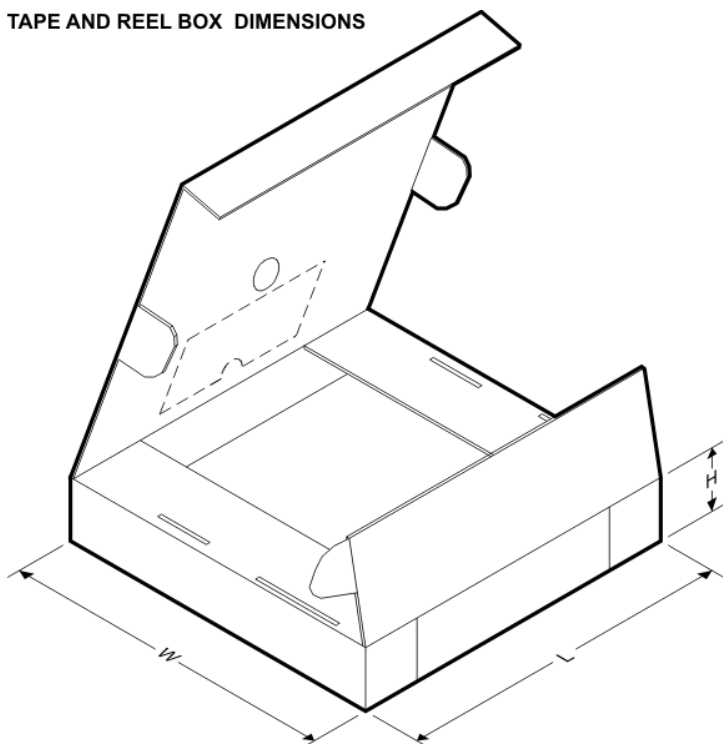
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CAVCH4T245MRSVREP	UQFN	RSV	16	3000	203.0	203.0	35.0

MECHANICAL DATA

RSV (R−PUQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD
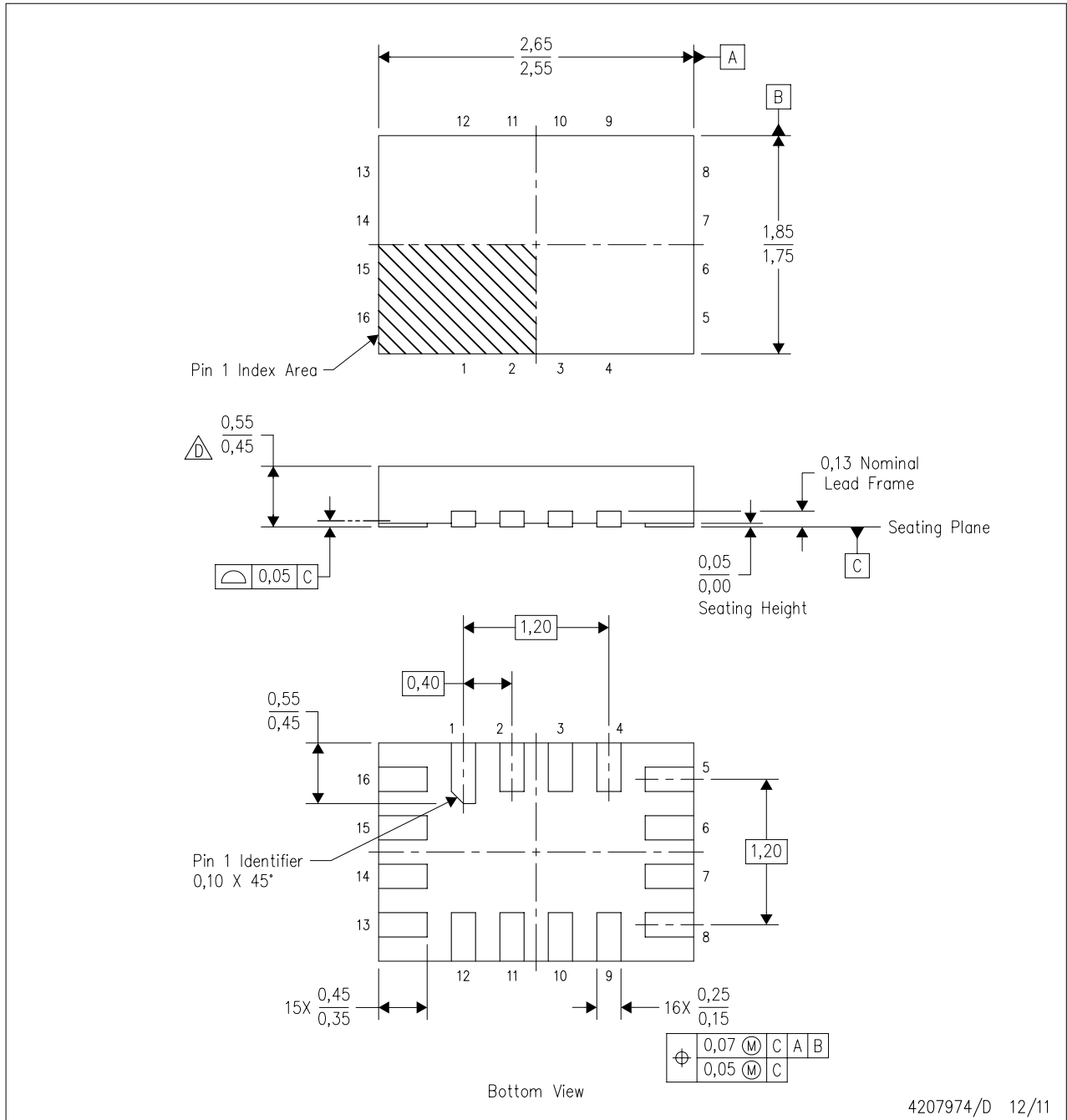
4207974/D 12/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No−Lead) package configuration.
D. This package complies to JEDEC MO−288 variation UFHE, except minimum package thickness.

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LAND PATTERN DATA

RSV (R–PUQFN–N16)   PLASTIC QUAD FLATPACK NO–LEAD

Example Board Layout

3,00
1,70
0,40
2,20
0,40 0,90
0,75
0,65
Pin 1 ID
0,20

Example Stencil Design
0.125mm Stencil Thickness
(Note F&G)

3,00
1,70
0,40
2,20
0,40 0,90
0,75
0,65
Pin 1 ID
0,20

Non Solder Mask Defined Pad

0,05
all around

Example
Solder Mask Opening
(Note D)

Example
Pad Geometry
(Note C)

0,10

4208244/C 02/13
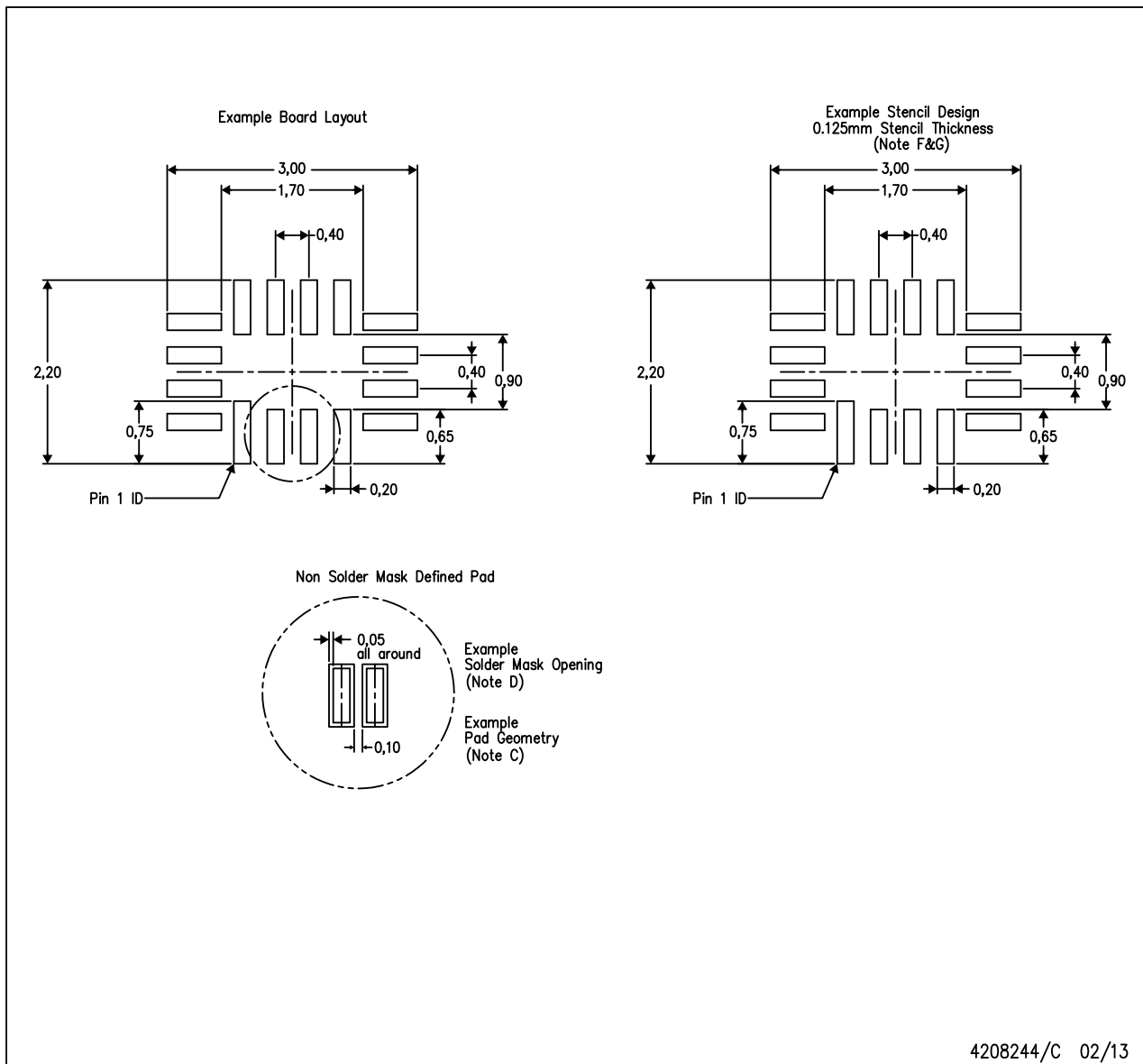
NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC–7351 is recommended for alternate designs.
         D.   Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
         E.   Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
         F.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
         G.   Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions
              if stencil manufacturing process allows for sufficient release at smaller opening.

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