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## STL80N4LLF3

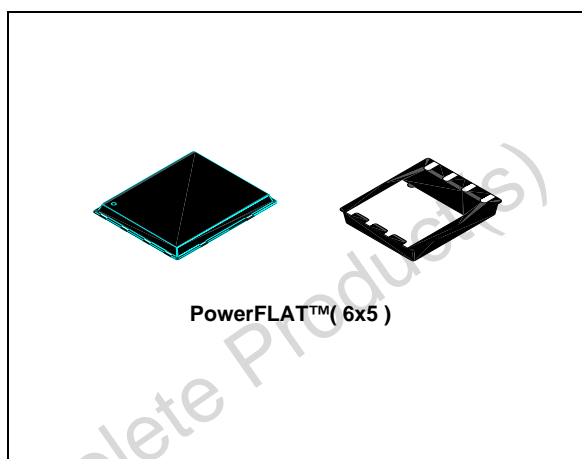
N-channel 40V - 0.0042Ω - 80A - PowerFLAT™ (6x5)  
 STripFET™ Power MOSFET for DC-DC conversion

### General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STL80N4LLF3	40V	<0.005Ω	20A <sup>(1)</sup>

1. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu, t<10 sec

- Improved die-to-footprint ratio
- Very low profile package (1mm Max)
- Very low thermal resistance
- Conduction losses reduced
- Switching losses reduced



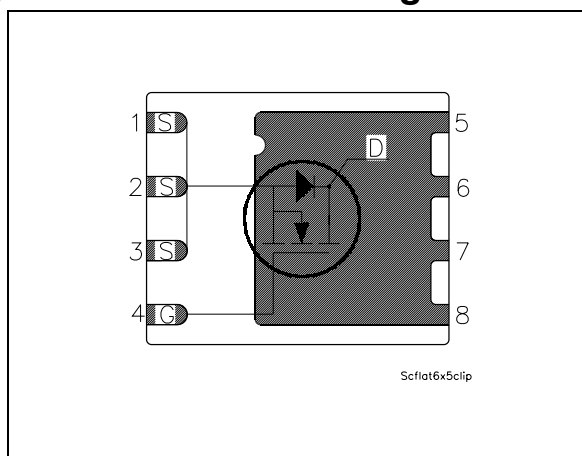
### Description

This series of product utilizes the latest advanced design rules of ST's proprietary STripFET™ Technology. The resulting Transistor is optimized for low on-Resistance and minimal gate charge. The chip-scaled PowerFLAT™ package allows a significant board space saving, still boosting the performance.

### Applications

- Switching application

### Internal schematic diagram



### Order codes

Part number	Marking	Package	Packaging
STL80N4LLF3	L80N4LLF3	PowerFLAT™ (6x5)	Tape & reel

## Contents

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Obsolete Product(s) - Obsolete Product(s)

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	40	V
$V_{GS}$	Gate- source voltage	$\pm 16$	V
$V_{GS}^{(1)}$	Gate- source voltage	$\pm 18$	V
$I_D^{(2)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	80	A
$I_D^{(2)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	50	A
$I_D^{(3)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	20	A
$I_{DM}^{(4)}$	Drain current (pulsed)	80	A
$P_{TOT}^{(2)}$	Total dissipation at $T_C = 25^\circ\text{C}$	80	W
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25^\circ\text{C}$	4	W
	Derating factor <sup>(3)</sup>	0.03	W/°C
$T_{stg}$ $T_j$	Storage temperature Operating junction temperature	-55 to 150	°C

1. Guaranteed for test time  $\leq 15\text{ms}$
2. The value is rated according Rthj-c
3. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu, t < 10 sec
4. Pulse width limited by safe operating area

**Table 2. Thermal resistance**

Symbol	Parameter	Value	Unit
Rthj-c	Thermal resistance junction-case max	1.56	°C/W
Rthj-pcb <sup>(1)</sup>	Thermal operating junction-pcb max	31.2	°C/W

1. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu, t < 10 sec

Electrical characteristics

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## 2 Electrical characteristics

(T<sub>CASE</sub> = 25°C unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	40			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max rating V <sub>DS</sub> = Max rating @ 125 °C			10 100	μA μA
I <sub>GSS</sub>	Gate-body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 16V			±200	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1			V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 10 A V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 10 A		0.0042 0.005	0.005 0.007	Ω Ω

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		2530		pF
C <sub>oss</sub>	Output capacitance			574		pF
C <sub>rss</sub>	Reverse transfer capacitance			29		pF
R <sub>G</sub>	Gate input resistance	f=1 MHz Gate DC Bias = 0 Test signal level = 20mV open drain	1	3	5	Ω
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 32V, I <sub>D</sub> = 20 A, V <sub>GS</sub> = 4.5V (see Figure 13)		21.5	28	nC
Q <sub>gs</sub>	Gate-source charge			6.9		nC
Q <sub>gd</sub>	Gate-drain charge			8.2		nC

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**Electrical characteristics**
**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 20V, I_D = 10A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ <i>(see Figure 15)</i>		17		ns
$t_r$	Rise time			25		ns
$t_{d(off)}$	Turn-off delay time			62		ns
$t_f$	Fall time			9		ns

**Table 6. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				20	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				80	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 20 A, V_{GS} = 0$			1.2	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 20A, V_{DD} = 20V$ $di/dt = 100A/\mu s$ $T_j = 150^\circ C$ <i>(see Figure 14)</i>		43		ns
$Q_{rr}$	Reverse recovery charge			64		nC
$I_{RRM}$	Reverse recovery current			3		A

1. Pulse width limited by safe operating area

 2. Pulsed: Pulse duration = 300 $\mu s$ , duty cycle 1.5%

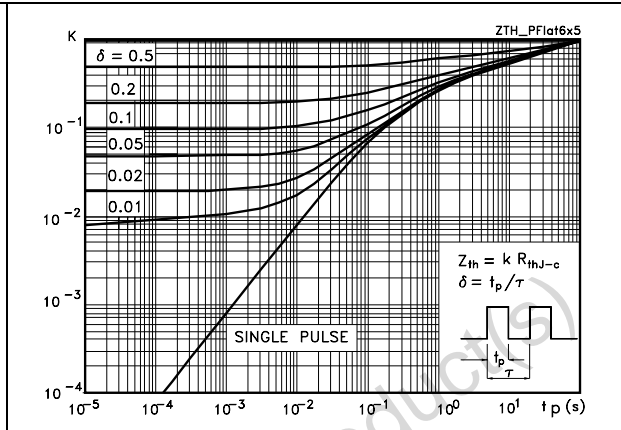
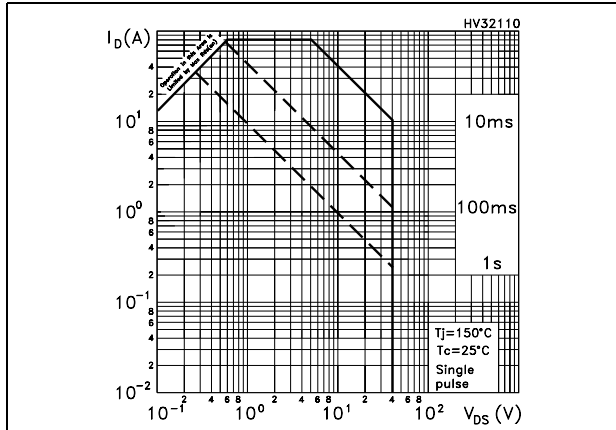
**Electrical characteristics**

**STL80N4LLF3**

**2.1 Electrical characteristics (curves)**

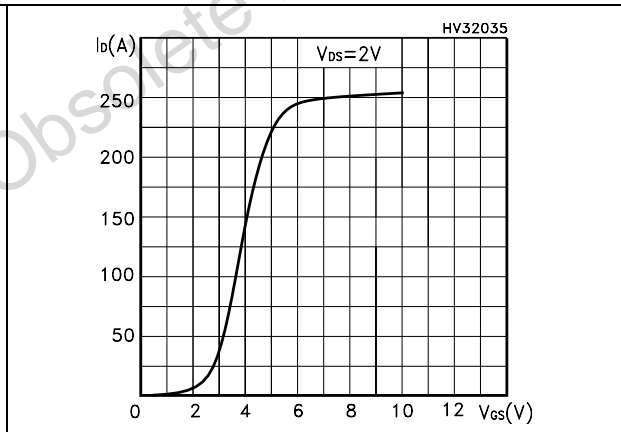
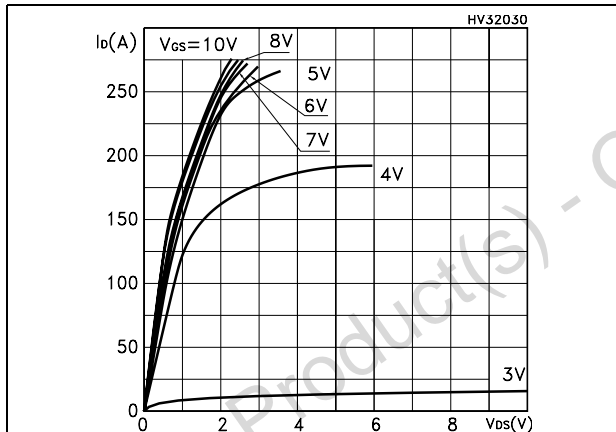
**Figure 1. Safe operating area**

**Figure 2. Thermal impedance**



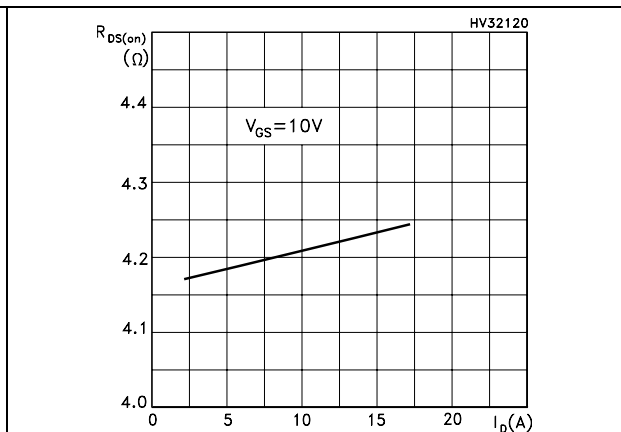
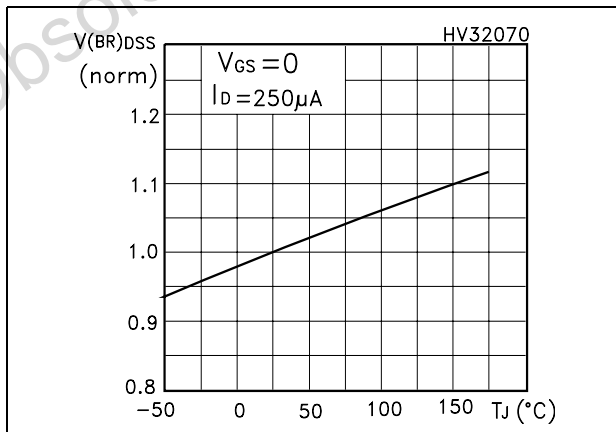
**Figure 3. Output characteristics**

**Figure 4. Transfer characteristics**



**Figure 5. Normalized  $B_{V_{DS}}$  vs temperature**

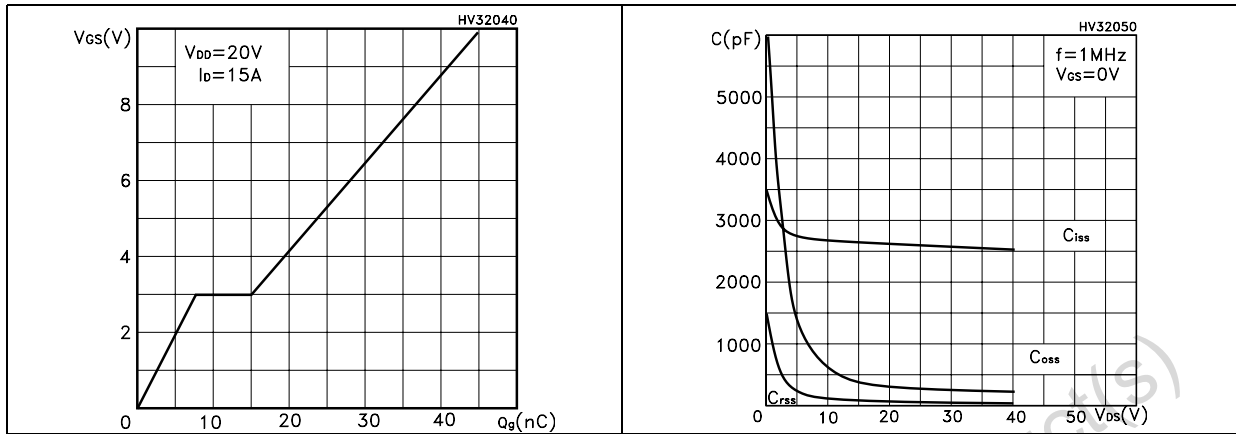
**Figure 6. Static drain-source on resistance**



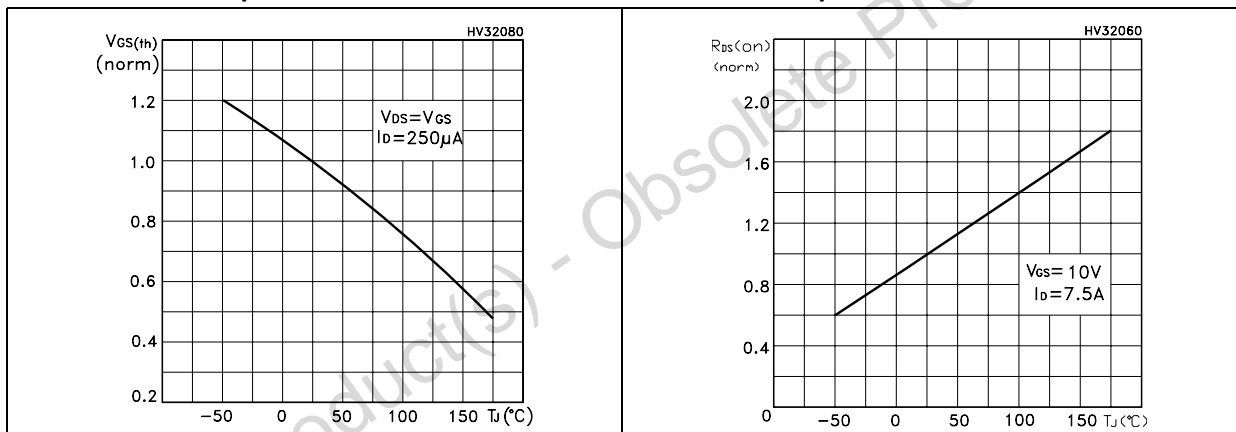
**STL80N4LLF3**

**Electrical characteristics**

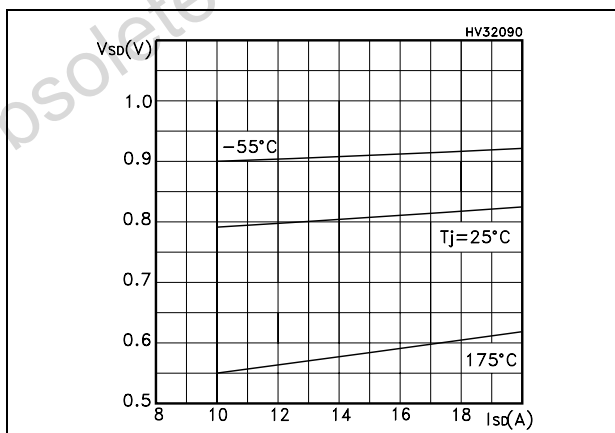
**Figure 7. Gate charge vs gate-source voltage** **Figure 8. Capacitance variations**



**Figure 9. Normalized gate threshold voltage vs temperature** **Figure 10. Normalized on resistance vs temperature**



**Figure 11. Source-drain diode forward characteristics**



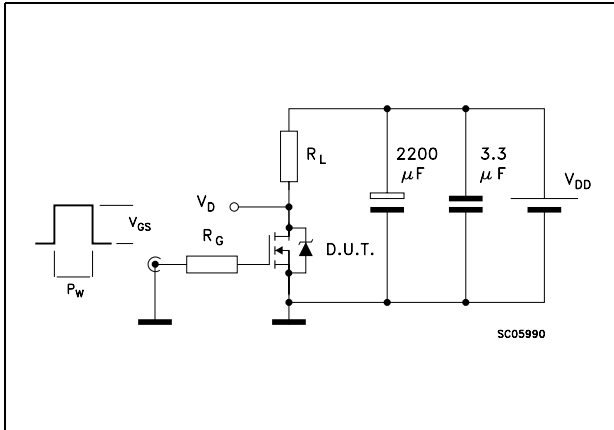


Test circuit

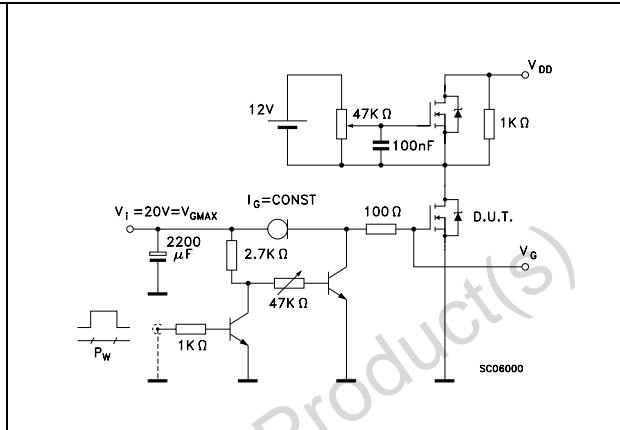
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**3 Test circuit**

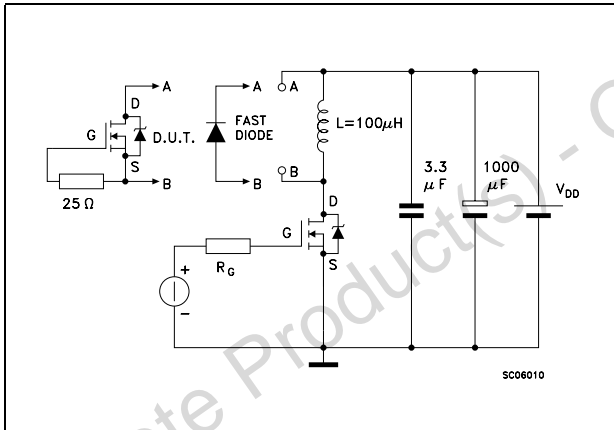
**Figure 12. Switching times test circuit for resistive load**



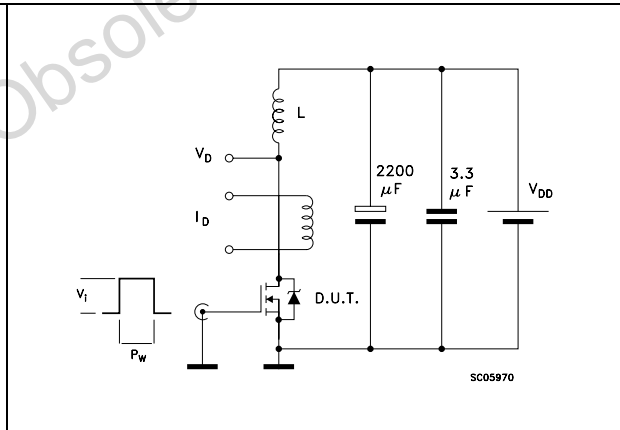
**Figure 13. Gate charge test circuit**



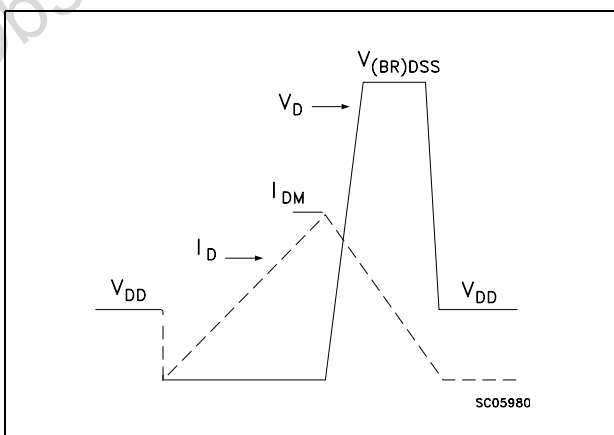
**Figure 14. Test circuit for inductive load switching and diode recovery times**



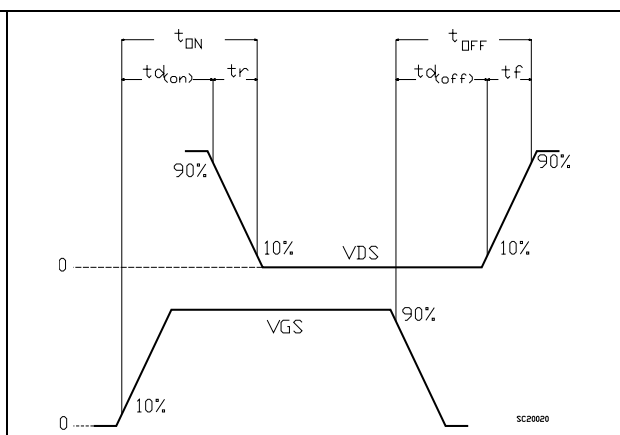
**Figure 15. Unclamped inductive load test circuit**



**Figure 16. Unclamped inductive waveform**



**Figure 17. Switching time waveform**



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

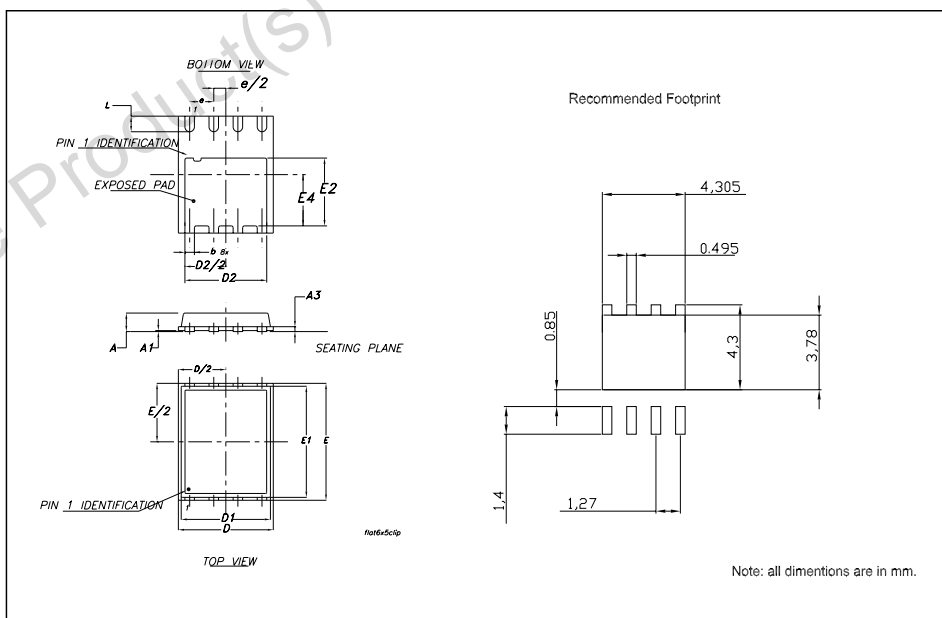
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**Package mechanical data**

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**PowerFLAT™ (6x5) MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.80	0.83	0.93	0.031	0.032	0.036
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.007	
b	0.35	0.40	0.47	0.013	0.015	0.018
D		5.00			0.196	
D1		4.75			0.187	
D2	4.15	4.20	4.25	0.163	0.165	0.167
E		6.00			0.236	
E1		5.75			0.226	
E2	3.43	3.48	3.53	0.135	0.137	0.139
E4	2.58	2.63	2.68		0.103	0.105
e		1.27			0.050	
L	0.70	0.80	0.90	0.027	0.031	0.035



## 5 Revision history

Table 7. Revision history

Date	Revision	Changes
13-May-2005	1	First release.
20-Jun-2005	2	Updated mechanical data
22-Jun-2005	3	New $R_G$ value on <a href="#">Table 6</a>
04-Jan-2006	4	New footprint
06-Jun-2006	5	Complete version
04-Sep-2006	6	New template, no content change
22-Nov-2006	7	Corrected part number

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## STL80N4LLF3

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