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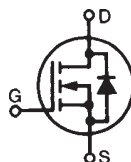
[IXYS Corporation](#)

[IXFL32N120P](#)

For any questions, you can email us directly:

sales@integrated-circuit.com

**Polar™ HiPerFET™
Power MOSFET**
IXFL32N120P
(Electrically Isolated Tab)

 N-Channel Enhancement Mode
 Avalanche Rated
 Fast Intrinsic Diode


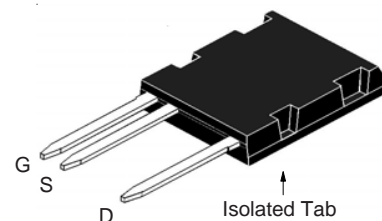
$$V_{DSS} = 1200V$$

$$I_{D25} = 24A$$

$$R_{DS(on)} \leq 340m\Omega$$

$$t_{rr} \leq 300ns$$

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ C$ to $150^\circ C$	1200	V
V_{DGR}	$T_J = 25^\circ C$ to $150^\circ C$, $R_{GS} = 1M\Omega$	1200	V
V_{GSS}	Continuous	± 30	V
V_{GSM}	Transient	± 40	V
I_{D25}	$T_C = 25^\circ C$	24	A
I_{DM}	$T_C = 25^\circ C$, Pulse Width Limited by T_{JM}	100	A
I_A	$T_C = 25^\circ C$	16	A
E_{AS}	$T_C = 25^\circ C$	2	J
dv/dt	$I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ C$	20	V/ns
P_D	$T_C = 25^\circ C$	520	W
T_J		-55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		-55 ... +150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ C$
T_{SOLD}	Plastic Body for 10s	260	$^\circ C$
V_{ISOL}	50/60 Hz, RMS, 1 minute	2500	V~
	$I_{ISOL} \leq 1mA$ $t = 1s$	3000	V~
F_C	Mounting Force	40..120/4.5..27	N/lb.
Weight		8	g

ISOPLUS i5-Pak™

 G = Gate D = Drain
 S = Source

Features

- Silicon Chip on Direct-Copper-Bond Substrate
 - High Power Dissipation
 - Isolated Mounting Surface
 - 2500V Electrical Isolation
- Avalanche Rated
- Fast Intrinsic Diode

Advantages

- Easy Assembly
- Space Savings
- High Power Density

Applications

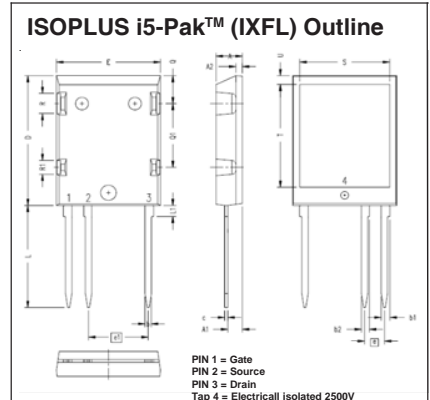
- Switch-Mode and Resonant-Mode Power Supplies
- DC-DC Converters
- Laser Drivers
- AC and DC Motor Drives
- Robotics and Servo Controls

Symbol	Test Conditions ($T_J = 25^\circ C$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = 3mA$	1200		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 1mA$	3.5		6.5 V
I_{GSS}	$V_{GS} = \pm 30V$, $V_{DS} = 0V$			± 300 nA
I_{DSS}	$V_{DS} = V_{DSS}$, $V_{GS} = 0V$ Note 2, $T_J = 125^\circ C$			50 μA 5 mA
$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 16A$, Note 1			340 m Ω

IXYS

IXFL32N120P

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 20\text{V}, I_D = 16\text{A}$, Note 1	17	29	S
C_{iss}	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$		21	nF
C_{oss}			1105	pF
C_{rss}			77	pF
R_{Gi}	Gate input resistance		0.84	Ω
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 16\text{A}$ $R_G = 1\Omega$ (External)		70	ns
t_r			62	ns
$t_{d(off)}$			88	ns
t_f			51	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 16\text{A}$		360	nC
Q_{gs}			130	nC
Q_{gd}			160	nC
R_{thJC}				0.24 $^\circ\text{C/W}$
R_{thCS}		0.15		$^\circ\text{C/W}$



SYM	INCHES		MILLIMETER	
	MIN	MAX	MIN	MAX
A	0.190	0.205	4.83	5.21
A1	0.102	0.118	2.59	3.00
A2	0.046	0.055	1.17	1.40
b	0.045	0.055	1.14	1.40
b1	0.063	0.072	1.60	1.83
b2	0.058	0.068	1.47	1.73
c	0.020	0.029	0.51	0.74
D	1.020	1.040	25.91	26.42
E	0.770	0.799	19.56	20.29
e	0.150 BSC		3.81 BSC	
e1	0.450 BSC		11.43 BSC	
L	0.780	0.820	19.81	20.83
L1	0.080	0.102	2.03	2.59
Q	0.210	0.235	5.33	5.97
Q1	0.490	0.513	12.45	13.03
R	0.150	0.180	3.81	4.57
R1	0.100	0.130	2.54	3.30
S	0.668	0.690	16.97	17.53
T	0.801	0.821	20.34	20.85
U	0.065	0.080	1.65	2.03

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{V}$			32 A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			128 A
V_{SD}	$I_F = I_S, V_{GS} = 0\text{V}$, Note 1			1.5 V
t_{rr}	$I_F = 25\text{A}, -di/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}, V_{GS} = 0\text{V}$			300 ns
Q_{RM}			1.9	μC
I_{RM}			15.0	A

Notes:

1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.
2. Part must be heatsunk for high-temp I_{ces} measurement.

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

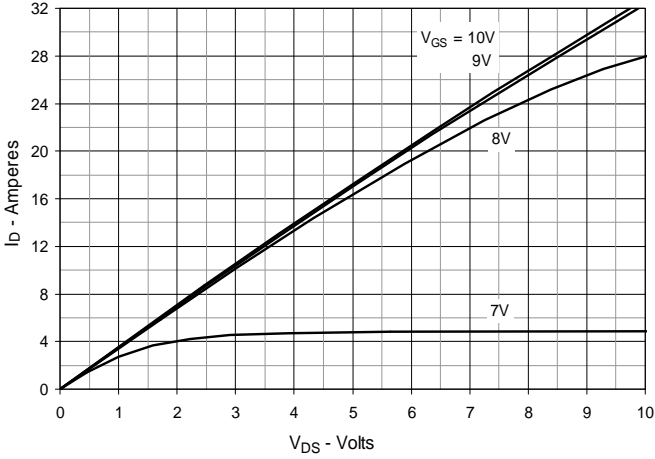


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

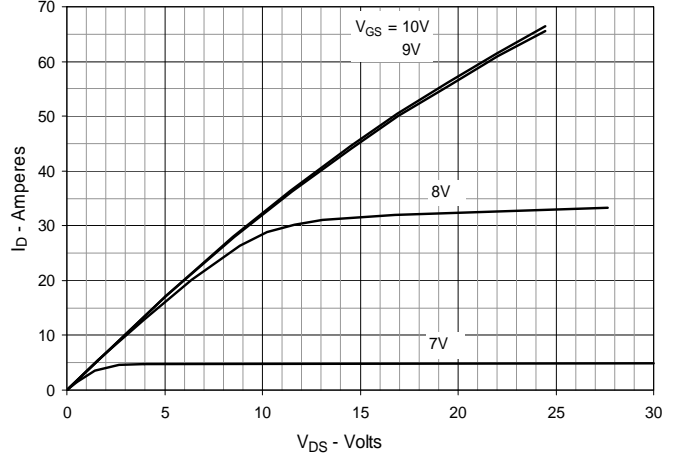


Fig. 3. Output Characteristics $T_J = 125^\circ\text{C}$

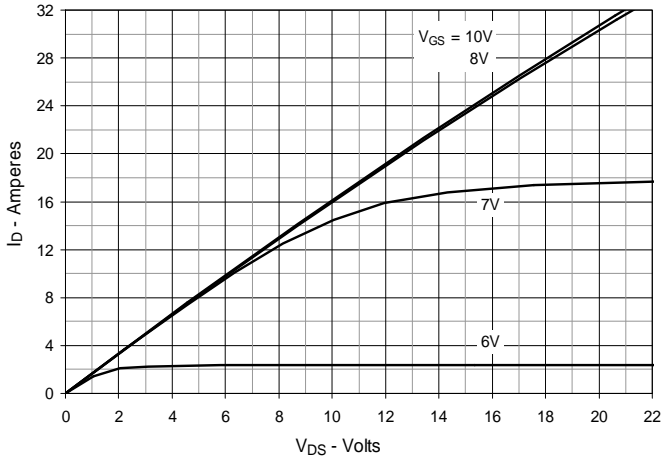


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 16\text{A}$ Value vs. Junction Temperature

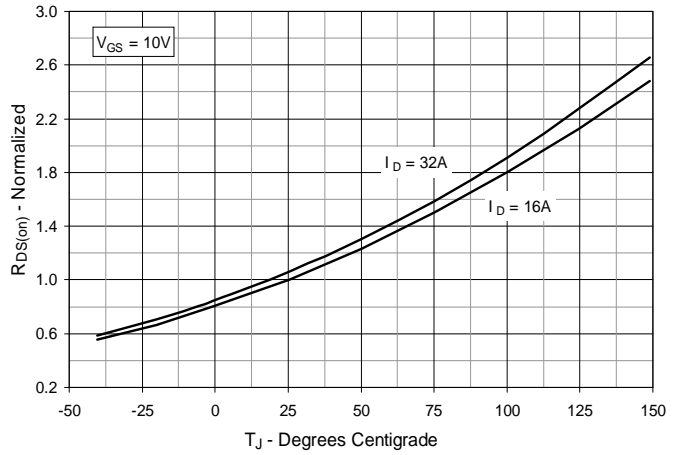


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 16\text{A}$ Value vs. Drain Current

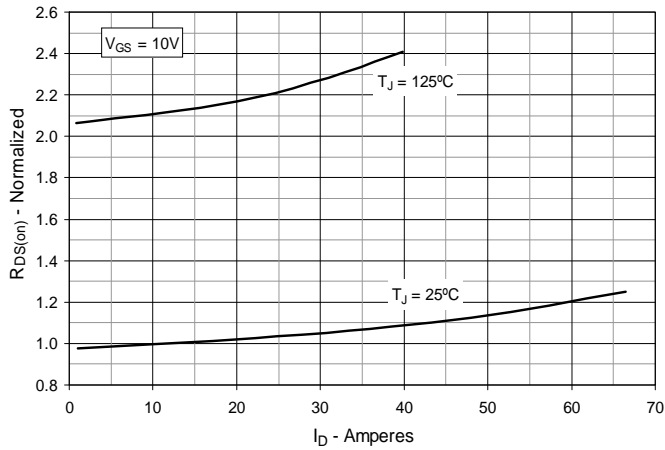


Fig. 6. Maximum Drain Current vs. Case Temperature

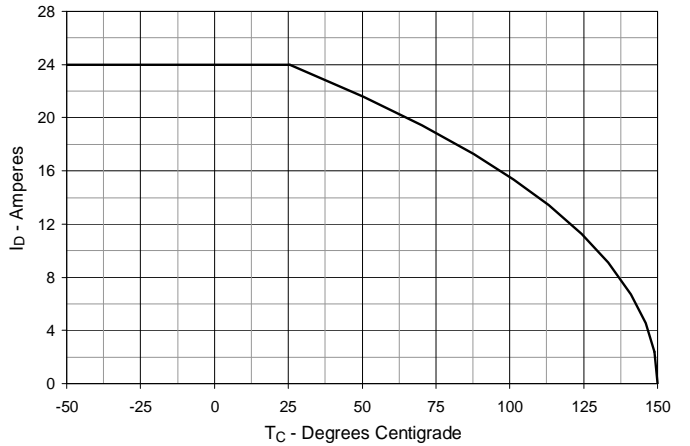


Fig. 7. Input Admittance

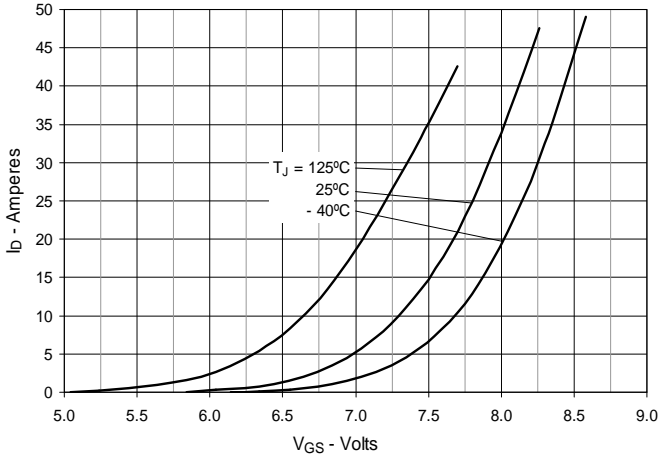


Fig. 8. Transconductance

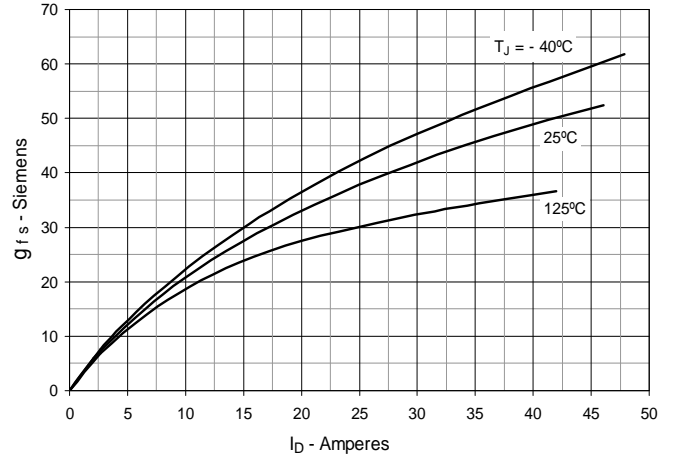


Fig. 9. Forward Voltage Drop of Intrinsic Diode

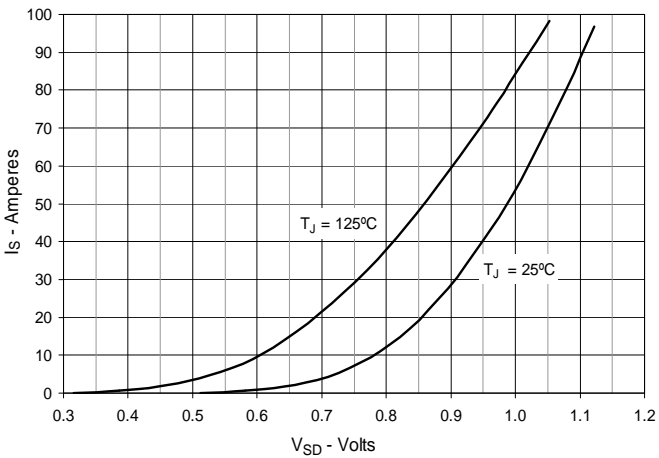


Fig. 10. Gate Charge

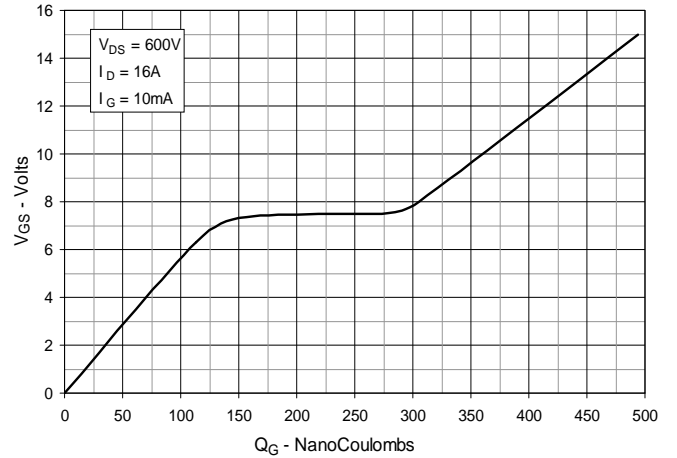


Fig. 11. Capacitance

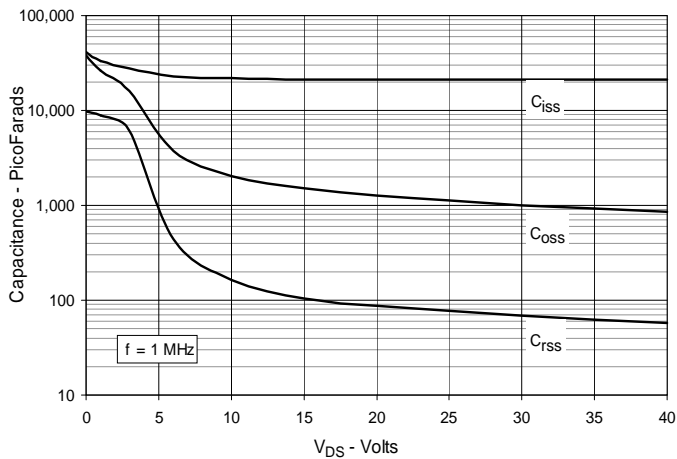


Fig. 12. Forward-Bias Safe Operating Area

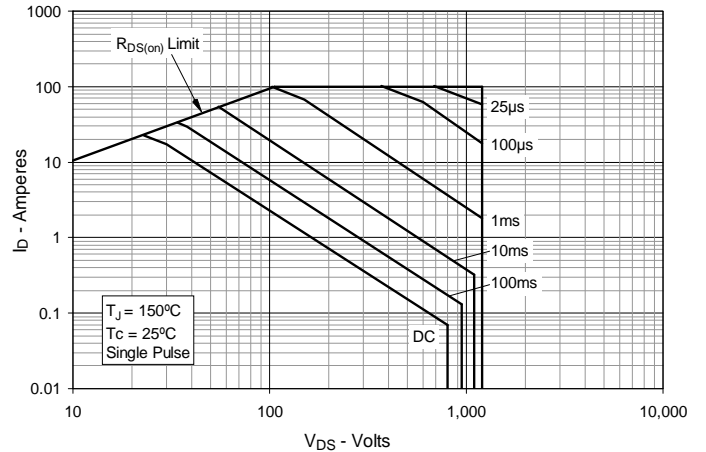


Fig. 13. Maximum Transient Thermal Impedance

