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Integrated Device Technology (IDT)
IDT5V995PFGI

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3.3V PROGRAMMABLE SKEW PLL CLOCK DRIVER TURBOCLOCK™ II

IDT5V995

FEATURES:

- **Ref input is 5V tolerant**
- **4 pairs of programmable skew outputs**
- **Low skew: 185ps same pair, 250ps all outputs**
- **Selectable positive or negative edge synchronization: Excellent for DSP applications**
- **Synchronous output enable**
- **Input frequency: 2MHz to 200MHz**
- **Output frequency: 6MHz to 200MHz**
- **3-level inputs for skew and PLL range control**
- **3-level inputs for feedback divide selection multiply / divide ratios of (1-6, 8, 10, 12) / (2, 4)**
- **PLL bypass for DC testing**
- **External feedback, internal loop filter**
- **12mA balanced drive outputs**
- **Low Jitter: <100ps cycle-to-cycle**
- **Power-down mode**
- **Lock indicator**
- **Available in TQFP package**

DESCRIPTION:

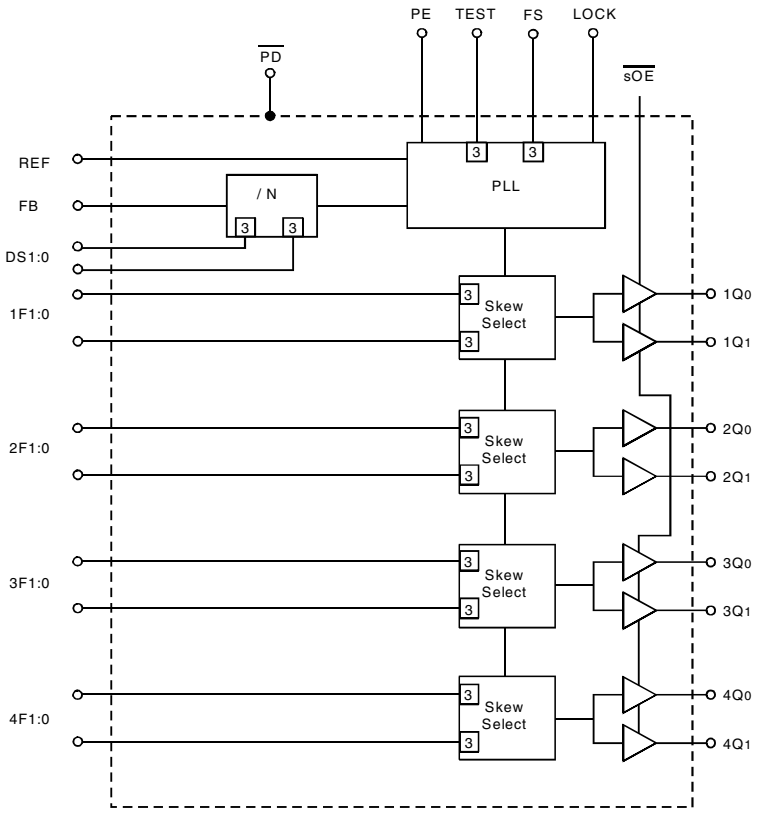
The IDT5V995 is a high fanout 3.3V PLL based clock driver intended for high performance computing and data-communications applications. A key feature of the programmable skew is the ability of outputs to lead or lag the REF input signal. The IDT5V995 has eight programmable skew outputs in four banks of 2. Skew is controlled by 3-level input signals that may be hard-wired to appropriate HIGH-MID-LOW levels.

The feedback input allows divide-by-functionality from 1 to 12 through the use of the DS[1:0] inputs. This provides the user with frequency multiplication from 1 to 12 without using divided outputs for feedback.

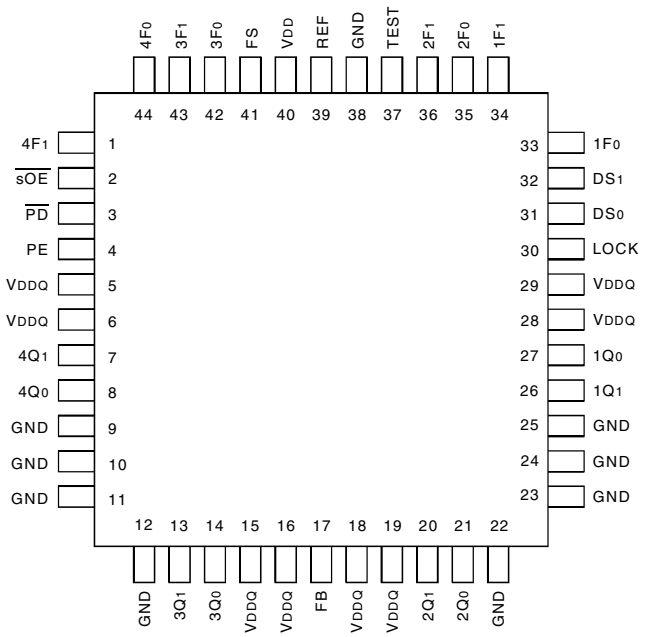
When the $\overline{sOE}$ pin is held low, all the outputs are synchronously enabled. However, if $\overline{sOE}$ is held high, all the outputs except 2Q0 and 2Q1 are synchronously disabled. The LOCK output asserts to indicate when Phase Lock has been achieved.

Furthermore, when PE is held high, all the outputs are synchronized with the positive edge of the REF clock input. When PE is held low, all the outputs are synchronized with the negative edge of REF. The IDT5V995 has LVTTL outputs with 12mA balanced drive outputs.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TQFP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description		Max	Unit
V_{DDQ}, V_{DD}	Supply Voltage to Ground		–0.5 to +4.6	V
V_I	DC Input Voltage		–0.5 to V_{DD}+0.5	V
	REF Input Voltage		–0.5 to +5.5	V
	Maximum Power Dissipation	T_A = 85°C	0.7	W
		T_A = 55°C	1.1	
T_{STG}	Storage Temperature Range		–65 to +150	°C

NOTE:
1. Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

CAPACITANCE (T_A = +25°C, f = 1MHz, V_{IN} = 0V)

Parameter	Description	Typ.	Max.	Unit
C_{IN}	Input Capacitance	5	7	pF

NOTE:
1. Capacitance applies to all inputs except TEST, FS, nF[1:0], and DS[1:0].

PIN DESCRIPTION

Pin Name	Type	Description
REF	IN	Reference Clock Input
FB	IN	Feedback Input
TEST(1)	IN	When MID or HIGH, disables PLL (except for conditions of Note 1). REF goes to all outputs. Skew Selections (See Control Summary Table) remain in effect. Set LOW for normal operation.
$\overline{sOE}$(1)	IN	Synchronous Output Enable. When HIGH, it stops clock outputs (except 2Q0 and 2Q1) in a LOW state (for PE = H) - 2Q0 and 2Q1 may be used as the feedback signal to maintain phase lock. When TEST is held at MID level and $\overline{sOE}$ is HIGH, the nF[1:0] pins act as output disable controls for individual banks when nF[1:0] = LL. Set $\overline{sOE}$ LOW for normal operation (has internal pull-down).
PE	IN	Selectable positive or negative edge control. When LOW/HIGH the outputs are synchronized with the negative/positive edge of the reference clock (has internal pull-up).
nF[1:0]	IN	3-level inputs for selecting 1 of 9 skew taps or frequency functions
FS	IN	Selects appropriate oscillator circuit based on anticipated frequency range. (See Programmable Skew Range.)
nQ[1:0]	OUT	Four banks of two outputs with programmable skew
DS[1:0]	IN	3-level inputs for feedback divider selection
$\overline{PD}$	IN	Power down control. Shuts off entire chip when LOW (has internal pull-up).
LOCK	OUT	PLL lock indication signal. HIGH indicates lock. LOW indicates that the PLL is not locked and outputs may not be synchronized to the inputs. (For more information on application specific use of the LOCK pin, please see AN237.)
V_{DDQ}	PWR	Power supply for output buffers
V_{DD}	PWR	Power supply for phase locked loop, lock output, and other internal circuitry
GND	PWR	Ground

NOTE:
1. When TEST = MID and $\overline{sOE}$ = HIGH, PLL remains active with nF[1:0] = LL functioning as an output disable control for individual output banks. Skew selections remain in effect unless nF[1:0] = LL.

PROGRAMMABLE SKEW

Output skew with respect to the REF input is adjustable to compensate for PCB trace delays, backplane propagation delays or to accommodate requirements for special timing relationships between clocked components. Skew is selectable as a multiple of a time unit (t_U) which ranges from 625ps to 1.3ns (see Programmable Skew Range and Resolution Table). There are nine skew configurations available for each output pair. These configurations are chosen by the $nF_{1:0}$ control pins. In order to minimize the number of control pins, 3-level inputs (HIGH-MID-LOW) are used, they are intended for but not restricted to hard-wiring. Undriven 3-level inputs default to the MID level. Where programmable skew is not a requirement, the control pins can be left open for the zero skew default setting. The Control Summary Table shows how to select specific skew taps by using the $nF_{1:0}$ control pins.

EXTERNAL FEEDBACK

By providing external feedback, the IDT5V995 gives users flexibility with regard to skew adjustment. The FB signal is compared with the input REF signal at the phase detector in order to drive the VCO. Phase differences cause the VCO of the PLL to adjust upwards or downwards accordingly.

An internal loop filter moderates the response of the VCO to the phase detector. The loop filter transfer function has been chosen to provide minimal jitter (or frequency variation) while still providing accurate responses to input frequency changes.

PROGRAMMABLE SKEW RANGE AND RESOLUTION TABLE

	FS = LOW	FS = MID	FS = HIGH	Comments
Timing Unit Calculation (t_U)	1/(32 x F_{NOM})	1/(16 x F_{NOM})	1/(8 x F_{NOM})	
VCO Frequency Range (F_{NOM})(1,2)	24 to 50MHz	48 to 100MHz	96 to 200MHz	
Skew Adjustment Range(3) Max Adjustment:	±7.8125ns	±7.8125ns	±7.8125ns	ns
	±67.5°	±135°	±270°	Phase Degrees
	±18.75%	±37.5%	±75%	% of Cycle Time
Example 1, F_{NOM} = 25MHz	t_U = 1.25ns	—	—	
Example 2, F_{NOM} = 37.5MHz	t_U = 0.833ns	—	—	
Example 3, F_{NOM} = 50MHz	t_U = 0.625ns	t_U = 1.25ns	—	
Example 4, F_{NOM} = 75MHz	—	t_U = 0.833ns	—	
Example 5, F_{NOM} = 100MHz	—	t_U = 0.625ns	t_U = 1.25ns	
Example 6, F_{NOM} = 150MHz	—	—	t_U = 0.833ns	
Example 7, F_{NOM} = 200MHz	—	—	t_U = 0.625ns	

NOTES:

1. The device may be operated outside recommended frequency ranges without damage, but functional operation is not guaranteed.
2. The level to be set on FS is determined by the nominal operating frequency of the VCO and Time Unit Generator. The VCO frequency always appears at $1Q_{1:0}$, $2Q_{1:0}$, and the higher outputs when they are operated in their undivided modes. The frequency appearing at the REF and FB inputs will be F_{NOM} when the output connected to FB is undivided and $DS_{[1:0]}$ = MM. The frequency of the REF and FB inputs will be F_{NOM} /2 or F_{NOM} /4 when the part is configured for frequency multiplication by using a divided output as the FB input and setting $DS_{[1:0]}$ = MM. Using the $DS_{[1:0]}$ inputs allows a different method for frequency multiplication (see Divide Selection Table).
3. Skew adjustment range assumes that a zero skew output is used for feedback. If a skewed Q output is used for feedback, then adjustment range will be greater. For example if a $4t_U$ skewed output is used for feedback, all other outputs will be skewed $-4t_U$ in addition to whatever skew value is programmed for those outputs. 'Max adjustment' range applies to output pairs 3 and 4 where ± $6t_U$ skew adjustment is possible and at the lowest F_{NOM} value.

DIVIDE SELECTION TABLE

DS [1:0]	FB Divide-by-n	Permitted Output Divide-by-n connected to FB(1)
LL	2	1 or 2
LM	3	1
LH	4	1, 2, or 4
ML	5	1 or 2
MM	1	1, 2, or 4
MH	6	1 or 2
HL	8	1 or 2
HM	10	1
HH	12	1

NOTE:
1. Permissible output division ratios connected to FB. The frequency of the REF input will be F_{NOM}/N when the part is configured for frequency multiplication by using an undivided output for FB and setting DS[1:0] to N (N = 1-6, 8, 10, 12).

CONTROL SUMMARY TABLE FOR FEEDBACK SIGNALS

nF1:0	Skew (Pair #1, #2)	Skew (Pair #3)	Skew (Pair #4)
LL(1)	–4tU	Divide by 2	Divide by 2
LM	–3tU	–6tU	–6tU
LH	–2tU	–4tU	–4tU
ML	–1tU	–2tU	–2tU
MM	Zero Skew	Zero Skew	Zero Skew
MH	1tU	2tU	2tU
HL	2tU	4tU	4tU
HM	3tU	6tU	6tU
HH	4tU	Divide by 4	Inverted(2)

NOTES:
1. LL disables outputs if TEST = MID and $\overline{sOE}$ = HIGH.
2. When pair #4 is set to HH (inverted), $\overline{sOE}$ disables pair #4 HIGH when PE = HIGH, $\overline{sOE}$ disables pair #4 LOW when PE = LOW.

RECOMMENDED OPERATING RANGE

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}/V_{DDQ}	Power Supply Voltage	3	3.3	3.6	V
T_A	Ambient Operating Temperature	-40	+25	+85	° C

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions		Min.	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH (REF, FB Inputs Only)		2	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW (REF, FB Inputs Only)		—	0.8	V
V_{IHH}	Input HIGH Voltage(1)	3-Level Inputs Only		V_{DD}—0.6	—	V
V_{IMM}	Input MID Voltage(1)	3-Level Inputs Only		V_{DD}/2—0.3	V_{DD}/2+0.3	V
V_{ILL}	Input LOW Voltage(1)	3-Level Inputs Only		—	0.6	V
I_{IN}	Input Leakage Current (REF, FB Inputs Only)	V_{IN} = V_{DD} or GND V_{DD} = Max.		—5	+5	µA
I_3	3-Level Input DC Current (TEST, FS, $nF_{[1:0]}$, $DS_{[1:0]}$)	V_{IN} = V_{DD}	HIGH Level	—	+200	µA
		V_{IN} = V_{DD}/2	MID Level	—50	+50	
		V_{IN} = GND	LOW Level	—200	—	
I_{PU}	Input Pull-Up Current (PE, $\overline{PD}$)	V_{DD} = Max., V_{IN} = GND		—25	—	µA
I_{PD}	Input Pull-Down Current ($\overline{sOE}$)	V_{DD} = Max., V_{IN} = V_{DD}		—	+100	µA
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = —2mA (LOCK Output)		2.4	—	V
		V_{DDQ} = Min., I_{OH} = —12mA ($nQ_{[1:0]}$ Outputs)		2.4	—	
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 2mA (LOCK Output)		—	0.4	V
		V_{DDQ} = Min., I_{OL} = 12mA ($nQ_{[1:0]}$ Outputs)		—	0.4	

NOTE:

1. These inputs are normally wired to V_{DD}, GND, or unconnected. Internal termination resistors bias unconnected inputs to V_{DD}/2. If these inputs are switched, the function and timing of the outputs may be glitched, and the PLL may require an additional t_{LOCK} time before all datasheet limits are achieved.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions(1)	Typ.(2)	Max.	Unit
I_{DDQ}	Quiescent Power Supply Current	V_{DD} = Max., TEST = MID, REF = LOW, PE = LOW, $\overline{sOE}$ = LOW, $\overline{PD}$ = HIGH FS = MID, All outputs unloaded	20	30	mA
I_{DDPD}	Power Down Current	V_{DD} = Max., $\overline{PD}$ = LOW, $\overline{SOE}$ = LOW PE = HIGH, TEST = HIGH, FS = HIGH $nF_{[1:0]}$ = HH, $DS_{[1:0]}$ = HH	—	25	µA
ΔI_{DD}	Power Supply Current per Input HIGH (REF and FB inputs only)	V_{IN} = 3V, V_{DD} = Max., $\overline{PD}$ = LOW, TEST = HIGH	1	30	µA
I_{DDD}	Dynamic Power Supply Current per Output	FS = L	190	290	µA/MHz
		FS = M	150	230	
		FS = H	130	200	
I_{TOT}	Total Power Supply Current	FS = L , F_{VCO} = 50MHz, C_L = 0pF	56	—	mA
		FS = M , F_{VCO} = 100MHz, C_L = 0pF	80	—	
		FS = H, F_{VCO} = 200MHz, C_L = 0pF	125	—	

NOTES:

1. Measurements are for divide-by-1 outputs, $nF_{[1:0]}$ = MM, and $DS_{[1:0]}$ = MM.
2. For nominal voltage and temperature.

INPUT TIMING REQUIREMENTS

Symbol	Description[1]		Min.	Max.	Unit
t_R, t_F	Maximum input rise and fall times, 0.8V to 2V		—	10	ns/V
t_{PWC}	Input clock pulse, HIGH or LOW		2	—	ns
D_H	Input duty cycle		10	90	%
F_{REF}	Reference clock input frequency	FS = LOW	2	50	MHz
		FS = MID	4	100	
		FS = HIGH	8	200	

NOTE:

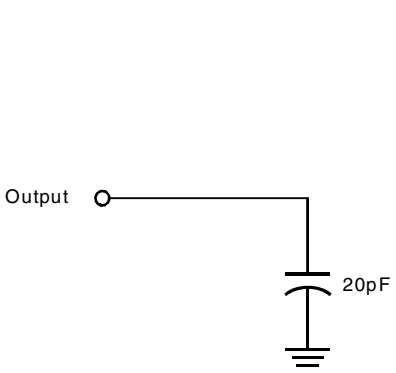
1. Where pulse width implied by D_H is less than t_{PWC} limit, t_{PWC} limit applies.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

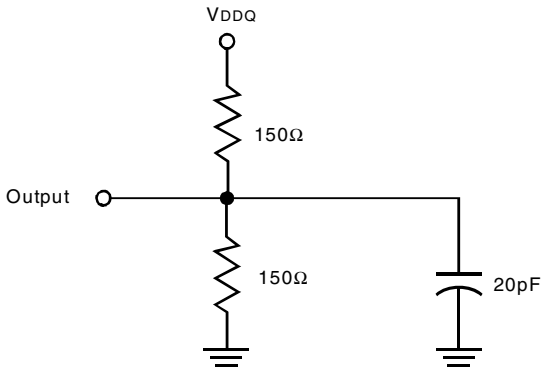
Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{NOM}	VCO Frequency Range	See Programmable Skew Range and Resolution Table			
t_{RPWH}	REF Pulse Width HIGH(1)	2	—	—	ns
t_{RPWL}	REF Pulse Width LOW(1)	2	—	—	ns
t_U	Programmable Skew Time Unit	See Control Summary Table			
t_{SKEWPR}	Zero Output Matched-Pair Skew (xQ_0, xQ_1)(2,3)	—	50	185	ps
t_{SKEW0}	Zero Output Skew (All Outputs)(4)	—	0.1	0.25	ns
t_{SKEW1}	Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs)(5)	—	0.1	0.25	ns
t_{SKEW2}	Output Skew (Rise-Fall, Nominal-Inverted, Divided-Divided)(5)	—	0.2	0.5	ns
t_{SKEW3}	Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs)(5)	—	0.15	0.5	ns
t_{SKEW4}	Output Skew (Rise-Fall, Nominal-Divided, Divided-Inverted)(2)	—	0.3	0.9	ns
t_{DEV}	Device-to-Device Skew(2,6)	—	—	0.75	ns
$(\phi)_{1-3}$	Static Phase Offset (FS = L, M, H) (FB Divide-by-n = 1, 2, 3)(7)	—0.25	—	0.25	ns
$(\phi)_H$	Static Phase Offset (FS = H)(7)	—0.25	—	0.25	ns
$t_{(\phi)M}$	Static Phase Offset (FS = M)(7)	—0.5	—	0.5	ns
$t_{(\phi)L1-6}$	Static Phase Offset (FS = L) (FB Divide-by-n = 1, 2, 3, 4, 5, 6)(7)	—0.7	—	0.7	ns
$t_{(\phi)L8-12}$	Static Phase Offset (FS = L) (FB Divide-by-n = 8, 10, 12)(7)	—1	—	1	ns
t_{ODCV}	Output Duty Cycle Variation from 50%	—1	0	1	ns
t_{PWH}	Output HIGH Time Deviation from 50%(8)	—	—	1.5	ns
t_{PWL}	Output LOW Time Deviation from 50%(9)	—	—	2	ns
t_{ORISE}	Output Rise Time	0.15	0.7	1.5	ns
t_{OFALL}	Output Fall Time	0.15	0.7	1.5	ns
t_{LOCK}	PLL Lock Time(10,11)	—	—	0.5	ms
t_{CCJH}	Cycle-to-Cycle Output Jitter (peak-to-peak) (divide by 1 output frequency, FS = H, FB divide-by-n=1,2)	—	—	100	ps
t_{CCJHA}	Cycle-to-Cycle Output Jitter (peak-to-peak) (divide by 1 output frequency, FS = H, FB divide-by-n=any)	—	—	150	
t_{CCJM}	Cycle-to-Cycle Output Jitter (peak-to-peak) (divide by 1 output frequency, FS = M)	—	—	150	
t_{CCJL}	Cycle-to-Cycle Output Jitter (peak-to-peak) (divide by 1 output frequency, FS = L, F_{REF} > 3MHz)	—	—	200	
t_{CCJLA}	Cycle-to-Cycle Output Jitter (peak-to-peak) (divide by 1 output frequency, FS = L, F_{REF} < 3MHz)	—	—	300	

NOTES:
1. Refer to Input Timing Requirements table for more detail.
2. Skew is the time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with the specified load.
3. t_{SKEWPR} is the skew between a pair of outputs (xQ0 and xQ1) when all eight outputs are selected for $0t_U$.
4. $t_{SK(0)}$ is the skew between outputs when they are selected for $0t_U$.
5. There are 3 classes of outputs: Nominal (multiple of t_U delay), Inverted (4Q0 and 4Q1 only with 4F0 = 4F1 = HIGH), and Divided (3Qx and 4Qx only in Divide-by-2 or Divide-by-4 mode). Test condition: nF0:1=MM is set on unused outputs.
6. t_{DEV} is the output-to-output skew between any two devices operating under the same conditions (V_{DDQ}, V_{DD}, ambient temperature, air flow, etc.)
7. $t\phi$ is measured with REF input rise and fall times (from 0.8V to 2V) of 0.5ns. Measured from 1.5V on REF to 1.5V on FB.
8. Measured at 2V.
9. Measured at 0.8V.
10. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{DD}/V_{DDQ} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.
11. Lock detector may be unreliable for input frequencies less than approximately 4MHz, or for input signals which contain significant jitter.

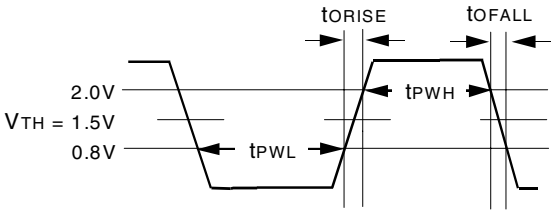
AC TEST LOADS AND WAVEFORMS



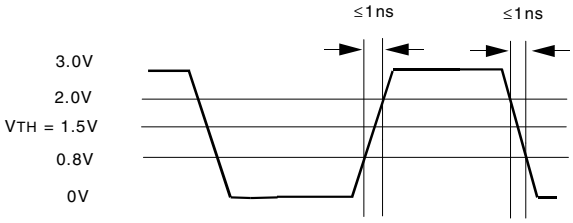
For LOCK output



For all other outputs

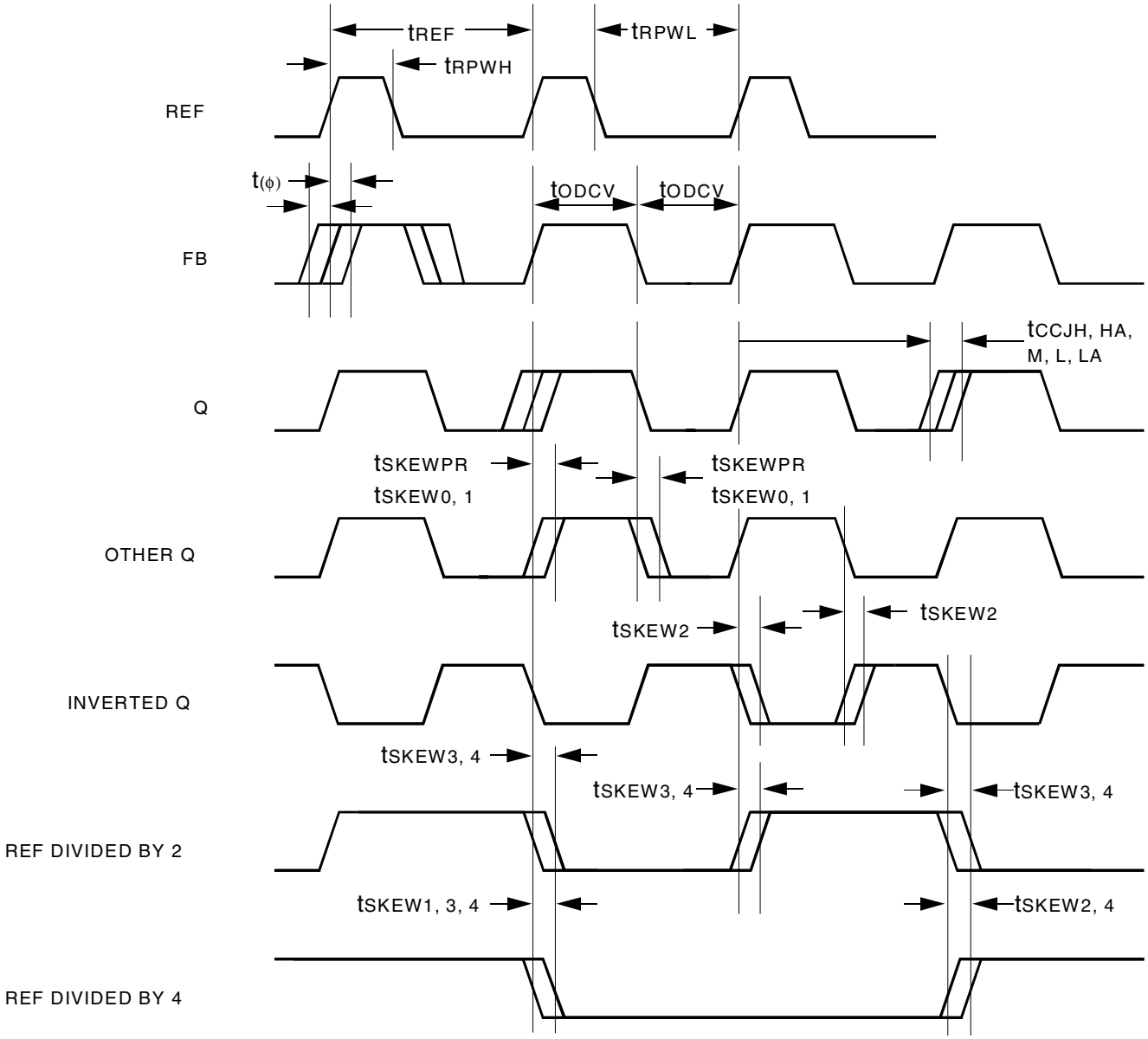


LVTTL Output Waveform



LVTTL Input Test Waveform

AC TIMING DIAGRAM



NOTES:

PE: The AC Timing Diagram applies to PE=V_{DD}. For PE=GND, the negative edge of FB aligns with the negative edge of REF, divided outputs change on the negative edge of REF, and the positive edges of the divide-by-2 and the divide-by-4 signals align.

Skew: The time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with 20pF and terminated with 75Ω to $V_{DDQ}/2$.

t_{SKEWPR}: The skew between a pair of outputs (xQ_0 and xQ_1) when all eight outputs are selected for $0t_U$.

t_{SKEW0}: The skew between outputs when they are selected for $0t_U$.

t_{DEV}: The output-to-output skew between any two devices operating under the same conditions (V_{DDQ}, V_{DD}, ambient temperature, air flow, etc.)

t_{ODCV}: The deviation of the output from a 50% duty cycle. Output pulse width variations are included in t_{SKEW2} and t_{SKEW4} specifications.

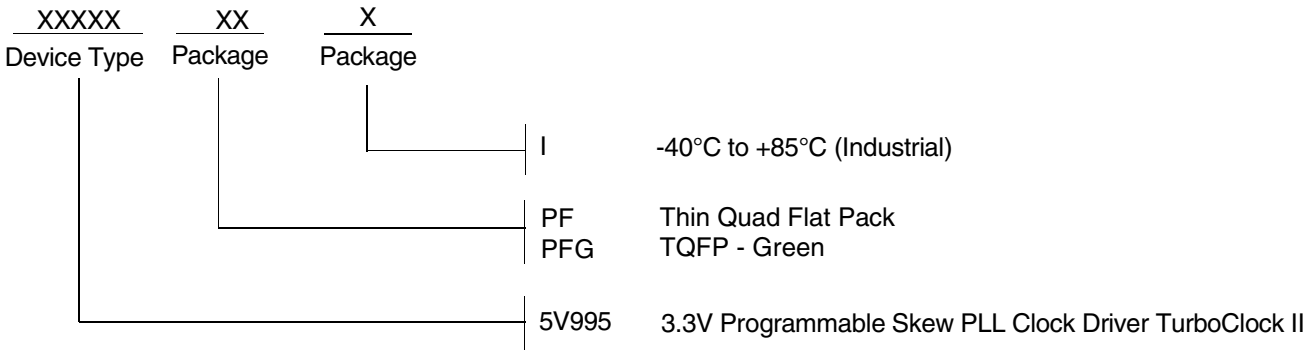
t_{PWH} is measured at 2V.

t_{PWL} is measured at 0.8V.

t_{ORISE} and t_{OFALL} are measured between 0.8V and 2V.

t_{LOCK}: The time that is required before synchronization is achieved. This specification is valid only after V_{DD}/V_{DDQ} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

ORDERING INFORMATION



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