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NXP Semiconductors/Freescale Semiconductor, Inc. BTA202X-600D,127

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Datasheet of BTA202X-600D,127 - TRIAC SENS GATE 600V 2A TO220-3 Contact us: sales@integrated-circuit.com Website: www.integrated-circuit.com



Product data sheet

1. General description

Planar passivated high commutation three quadrant triac in a SOT186A (TO-220F) "full pack" plastic package. The "series D" triac balances the requirements of commutation performance and gate sensitivity. This "very sensitive gate" "series D" is intended for interfacing with low power drivers including microcontrollers.

2. Features and benefits

- 3Q technology for improved noise immunity
- Direct interfacing with low power drivers and microcontrollers
- Good immunity to false turn-on by dV/dt
- High commutation capability with very sensitive gate
- High voltage capability
- Isolated mounting base package
- Planar technology for voltage ruggedness and reliability
- Triggering in three quadrants only
- Very sensitive gate for easy logic level triggering

3. Applications

- General purpose motor controls
- Large and small appliances (White Goods)
- Loads such as contactors, circuit breakers, valves, dispensers and door locks
- Lower-power highly inductive, resistive and safety loads

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DRM}	repetitive peak off- state voltage		-	-	600	V
I _{TSM}	non-repetitive peak on- state current	full sine wave; $T_{j(init)} = 25 \text{ °C}$; $t_p = 20 \text{ ms}$; Fig. 4; Fig. 5	-	-	14	A
I _{T(RMS)}	RMS on-state current	full sine wave; $T_h \le 110 ^{\circ}\text{C}$; Fig. 1; Fig. 2; Fig. 3	-	-	2	A
Static chara	cteristics					,
I _{GT}	gate trigger current	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ G+;$ $T_j = 25 \text{ °C}; Fig. 7$	0.25	-	5	mA







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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ G-;$ $T_j = 25 \text{ °C}; Fig. 7$	0.25	-	5	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; \text{ T2- G-};$ $T_j = 25 \text{ °C}; \underline{\text{Fig. 7}}$	0.25	-	5	mA

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	mb	T2——T1
2	T2	main terminal 2		sym051
3	G	gate		,
mb	n.c.	mounting base; isolated		
			TO-220F (SOT186A)	

6. Ordering information

Table 3. Ordering information

rance or tracking in								
Type number	Package	ge						
	Name	Description	Version					
BTA202X-600D	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A					

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7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	600	V
I _{T(RMS)}	RMS on-state current	full sine wave; T _h ≤ 110 °C; <u>Fig. 1;</u> <u>Fig. 2; Fig. 3</u>	-	2	Α
I _{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25 ^{\circ}C$; $t_p = 20 \text{ms}$; Fig. 4; Fig. 5	-	14	A
		full sine wave; $T_{j(init)} = 25 ^{\circ}\text{C}$; $t_p = 16.7 \text{ms}$	-	15.4	A
I ² t	I2t for fusing	t _p = 10 ms; SIN	-	0.98	A ² s
dI _T /dt	rate of rise of on-state current	$I_T = 1.5 \text{ A}$; $I_G = 0.2 \text{ A}$; $dI_G/dt = 0.2 \text{ A}/\mu\text{s}$	-	100	A/µs
I _{GM}	peak gate current		-	2	Α
P_GM	peak gate power		-	5	W
P _{G(AV)}	average gate power	over any 20 ms period	-	0.5	W
T _{stg}	storage temperature		-40	150	°C
Tj	junction temperature		-	125	°C

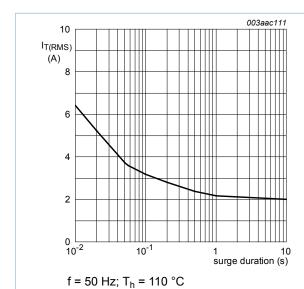


Fig. 1. RMS on-state current as a function of surge duration; maximum values

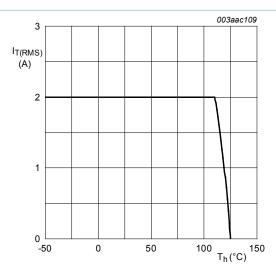


Fig. 2. RMS on-state current as a function of heatsink temperature; maximum values

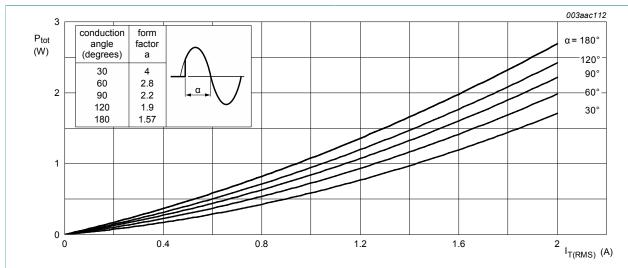
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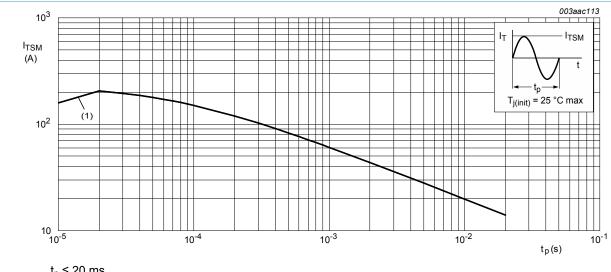
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 α = conduction angle

a = form factor = $I_{T(RMS)} / I_{T(AV)}$

Total power dissipation as a function of RMS on-state current; maximum values



 $t_p \le 20 \text{ ms}$

(1) dI_T/dt limit

Non-repetitive peak on-state current as a function of pulse width; maximum values Fig. 4.

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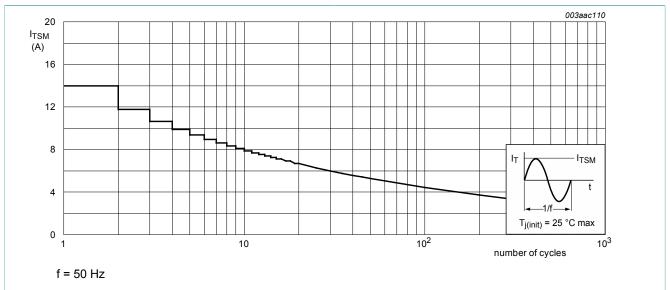


Fig. 5. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

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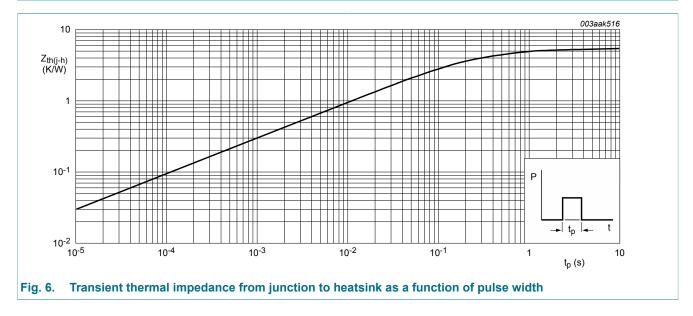
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8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-h)}	thermal resistance from junction to heatsink	full cycle; with heatsink compound; Fig. 6	-	-	5.5	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	-	55	-	K/W



9. Isolation characteristics

Table 6. Isolation characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{isol(RMS)}	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; 50 Hz \leq f \leq 60 Hz; RH \leq 65 %; T _h = 25 °C	-	-	2500	V
C _{isol}	isolation capacitance	from main terminal 2 to external heatsink; f = 1 MHz	-	10	-	pF

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static char	acteristics		1			
I _{GT}	gate trigger current	$V_D = 12 \text{ V; } I_T = 0.1 \text{ A; } T2+ \text{ G+;}$ $T_j = 25 \text{ °C; } Fig. 7$	0.25	-	5	mA
		$V_D = 12 \text{ V; } I_T = 0.1 \text{ A; } T2 + \text{G-;}$ $T_j = 25 \text{ °C; } Fig. 7$	0.25	-	5	mA
		$V_D = 12 \text{ V; } I_T = 0.1 \text{ A; } T2-\text{ G-;}$ $T_j = 25 \text{ °C; } Fig. 7$	0.25	-	5	mA
IL	latching current	$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; T2+ G+;$ $T_j = 25 \text{ °C}; Fig. 8$	-	-	5	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; T2+ G-;$ $T_j = 25 \text{ °C}; Fig. 8$	-	-	10	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; \text{ T2- G-};$ $T_j = 25 ^{\circ}\text{C}; \text{ Fig. 8}$	-	-	5	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 9</u>	-	-	5	mA
V _T	on-state voltage	I _T = 3 A; T _j = 25 °C; <u>Fig. 10</u>	-	1.63	2	V
V_{GT}	gate trigger voltage	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_j = 25 ^{\circ}\text{C};$ Fig. 11	-	0.7	1	V
		V _D = 400 V; I _T = 0.1 A; T _j = 125 °C; Fig. 11	0.2	0.3	-	V
I _D	off-state current	V _D = 600 V; T _j = 125 °C	-	0.1	0.5	mA
Dynamic c	haracteristics		1			
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 402 V; T_j = 125 °C; R_{GT1} = 220 Ω ; (V_{DM} = 67% of V_{DRM}); exponential waveform	-	350	-	V/µs
dl _{com} /dt	rate of change of commutating current	V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 2 A; dV_{com}/dt = 20 V/ μ s; (snubberless condition); gate open circuit	1	-	-	A/ms
		V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 2 A; dV_{com}/dt = 10 V/ μ s; gate open circuit	1.2	-	-	A/ms



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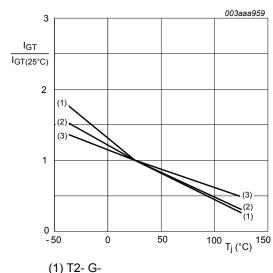
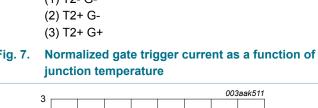


Fig. 7. junction temperature



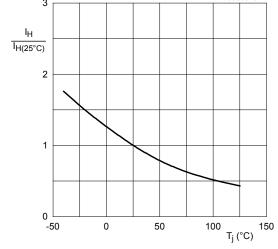


Fig. 9. Normalized holding current as a function of junction temperature

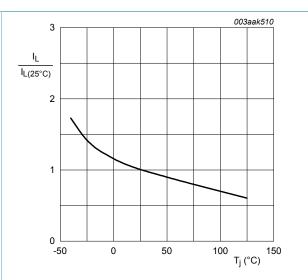
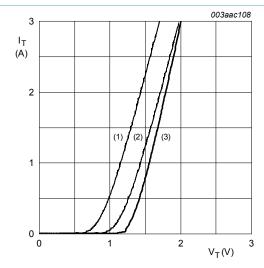


Fig. 8. Normalized latching current as a function of junction temperature



- $V_0 = 0.9 \text{ V}; R_s = 0.267 \Omega$
- (1) T_i = 125 °C; typical values
- (2) T_i = 125 °C; maximum values
- (3) T_i = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

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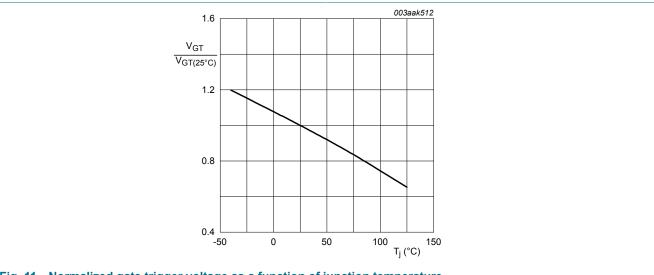


Fig. 11. Normalized gate trigger voltage as a function of junction temperature



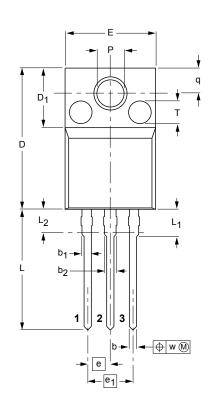
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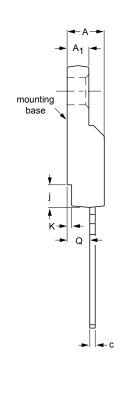
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11. Package outline

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 'full pack'

SOT186A





0 5 10 mm Luuruuluuruul scale

DIMENSIONS (mm are the original dimensions)

UNIT	Α	A ₁	b	b ₁	b ₂	С	D	D ₁	E	е	e ₁	j	K	L	L ₁	L ₂ ⁽¹⁾ max.	Р	Q	q	T ⁽²⁾	w
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	1.4 1.0	0.7 0.4	15.8 15.2	6.5 6.3	10.3 9.7	2.54	5.08	2.7 1.7	0.6 0.4	14.4 13.5	3.30 2.79	3	3.2 3.0	2.6 2.3	3.0 2.6	2.5	0.4

Notes

- 1. Terminal dimensions within this zone are uncontrolled.
- 2. Both recesses are # 2.5 × 0.8 max. depth

IEC JEDE	C JEITA	PROJE	ECTION ISSUE DATE
3-lead TO-	220F		-02-04-09 06-02-14
		3-lead TO-220F	

Fig. 12. Package outline TO-220F (SOT186A)

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