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# STP5N120

## N-channel 1200 V, 2.7 $\Omega$ , 4.7 A TO-220 Zener-protected SuperMESH™ Power MOSFET

### Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>W</sub>
STP5N120	1200 V	< 3.5 $\Omega$	4.7 A	160 W

- 100% avalanche tested
- Extremely high dv/dt capability
- ESD improved capability
- New high voltage benchmark
- Gate charge minimized

### Application

- Switching applications

### Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage Power MOSFETs.

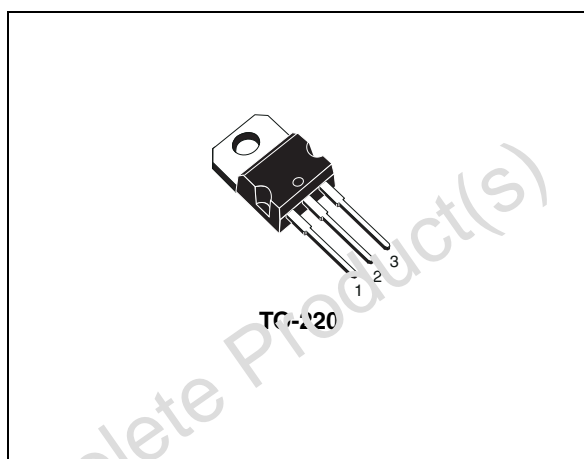


Figure 1. Internal schematic diagram

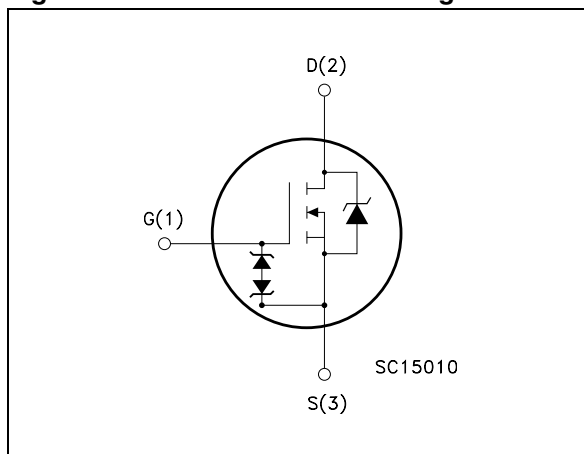


Table 1. Device summary

Order code	Marking	Package	Packaging
STP5N120	5N120	TO-220	Tube

## Contents

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Obsolete Product(s) - Obsolete Product(s)

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	1200	V
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	4.7	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	3	A
$I_{DM}^{(1)}$	Drain current (pulsed)	18.8	A
	Derating factor	1.28	W/ $^\circ\text{C}$
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	160	W
$V_{ESD(G-S)}$	Gate source ESD (HBM-C = 100 pF, R = 1.5 k $\Omega$ )	4000	V
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4	V/ns
$T_j$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area
2.  $I_{SD} \leq 4.7\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq 80\% V_{(BF, DSS)}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.78	$^\circ\text{C}/\text{W}$
$R_{thj-amb}^{(1)}$	Thermal resistance junction-amb max	62.5	$^\circ\text{C}/\text{W}$
$T_l$	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

1. When mounted on 1inch<sup>2</sup> FR-4 board, 2 oz Cu

**Table 4. Avalanche characteristics**

Symbol	Parameter	Max value	Unit
$I_{AS}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	4.7	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AS}$ , $V_{DD} = 50\text{ V}$ )	400	mJ

**Electrical characteristics**
**STP5N120**

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}, V_{GS} = 0$	1200			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating}, T_c = 125\text{ }^{\circ}\text{C}$			1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}, I_D = 2.3\text{ A}$		2.7	3.5	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{ V}, I_D = 2.3\text{ A}$		5.8		S
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$		2004		pF
$C_{oss}$	Output capacitance			139		pF
$C_{rss}$	Reverse transfer capacitance			19		pF
$C_{oss\ eq.}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0\text{ to }960\text{ V}$		89		pF
$R_g$	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$		2.2		$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 960\text{ V}, I_D = 4.7\text{ A}$		57		nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 10\text{ V}$		10		nC
$Q_{gd}$	Gate-drain charge	(see <a href="#">Figure 15</a> )		31		nC

1. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

2.  $C_{oss\ eq.}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 600\text{ V}, I_D = 2.3\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see <a href="#">Figure 17</a> )		18		ns	
$t_r$	Rise time			9		ns	
$t_{d(off)}$	Turn-off delay time				42		ns
$t_f$	Fall time				30		ns

**STP5N120**
**Electrical characteristics**
**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		4.7	mA
$I_{SDM}$	Source-drain current (pulsed)		-		18.8	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 4.7\text{ A}, V_{GS} = 0$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 4.7\text{ A}, V_{DD} = 60\text{ V}$	-	760		ns
$Q_{rr}$	Reverse recovery charge	$di/dt = 100\text{ A}/\mu\text{s}$ ,	-	5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see <a href="#">Figure 16</a> )		14		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 4.7\text{ A}, V_{DD} = 60\text{ V}$	-	880		ns
$Q_{rr}$	Reverse recovery charge	$di/dt = 100\text{ A}/\mu\text{s}$ ,	-	7		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	$T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 16</a> )		160		A

 1. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

**Table 9. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$BV_{GSO}$	Gate-source breakdown voltage	$I_{gs} \pm 1\text{ mA}$ , (open drain)	30			V

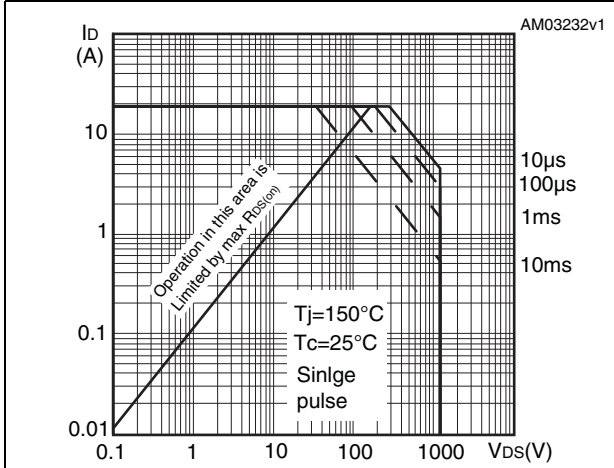
The built-in-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

**Electrical characteristics**

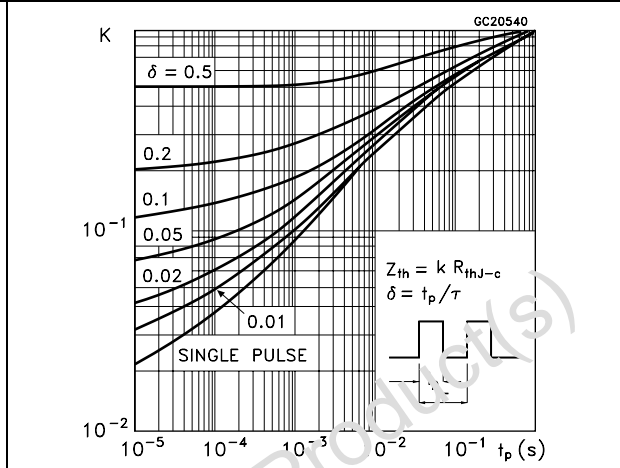
**STP5N120**

**2.1 Electrical characteristics (curves)**

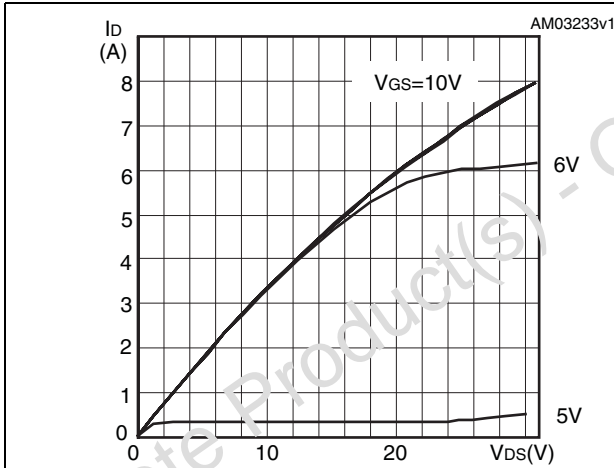
**Figure 2. Safe operating area**



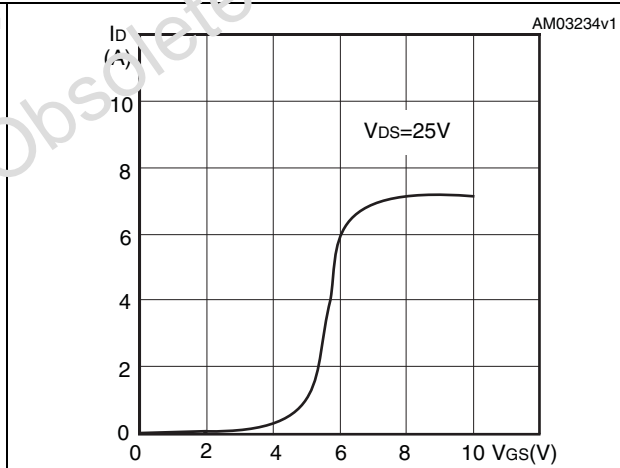
**Figure 3. Thermal impedance**



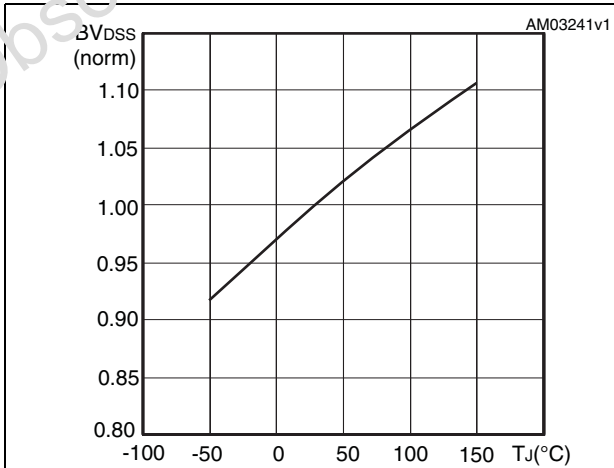
**Figure 4. Output characteristics**



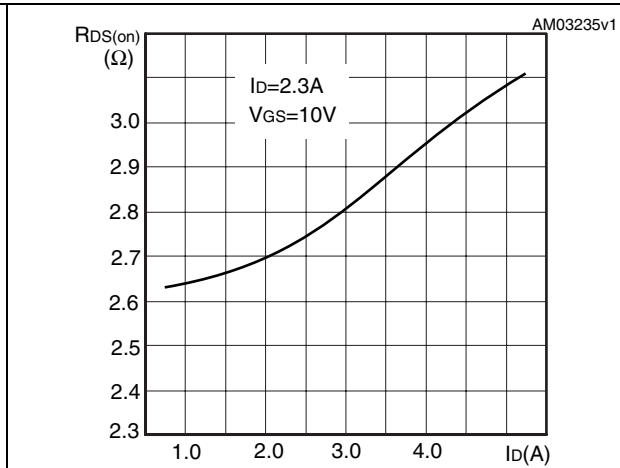
**Figure 5. Transfer characteristics**



**Figure 6. Normalized  $B_{V_{DSS}}$  vs temperature**



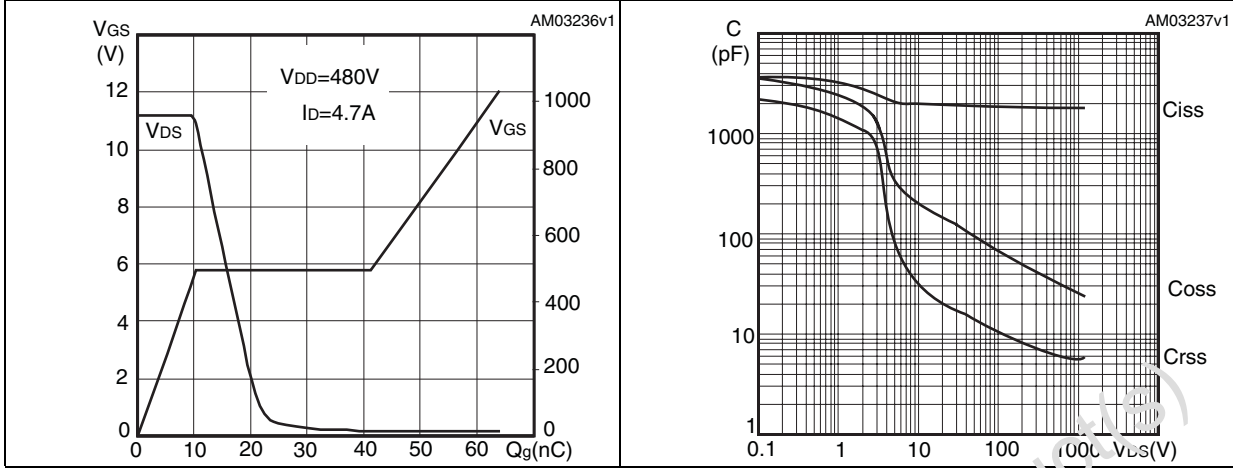
**Figure 7. Static drain-source on resistance**



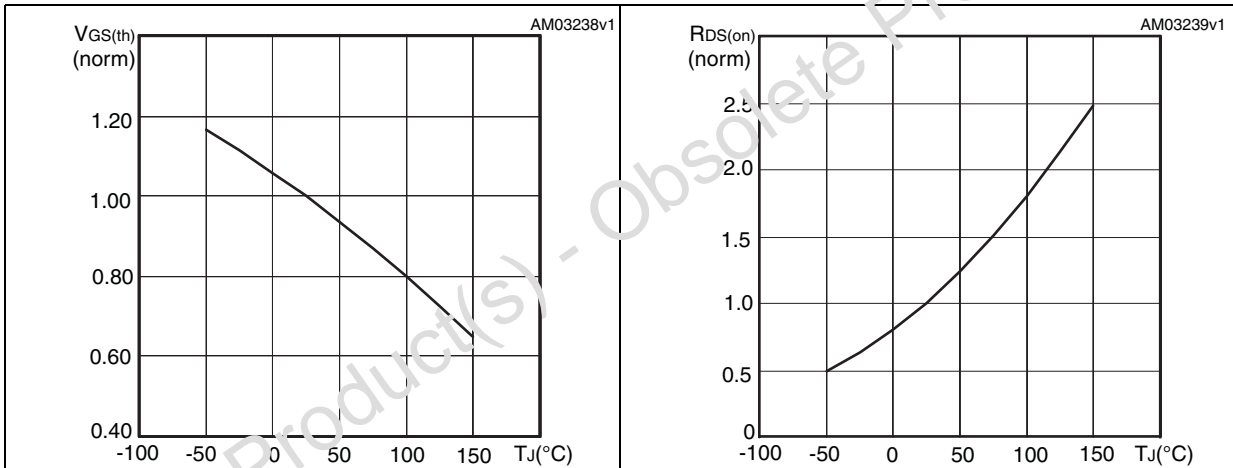
**STP5N120**

**Electrical characteristics**

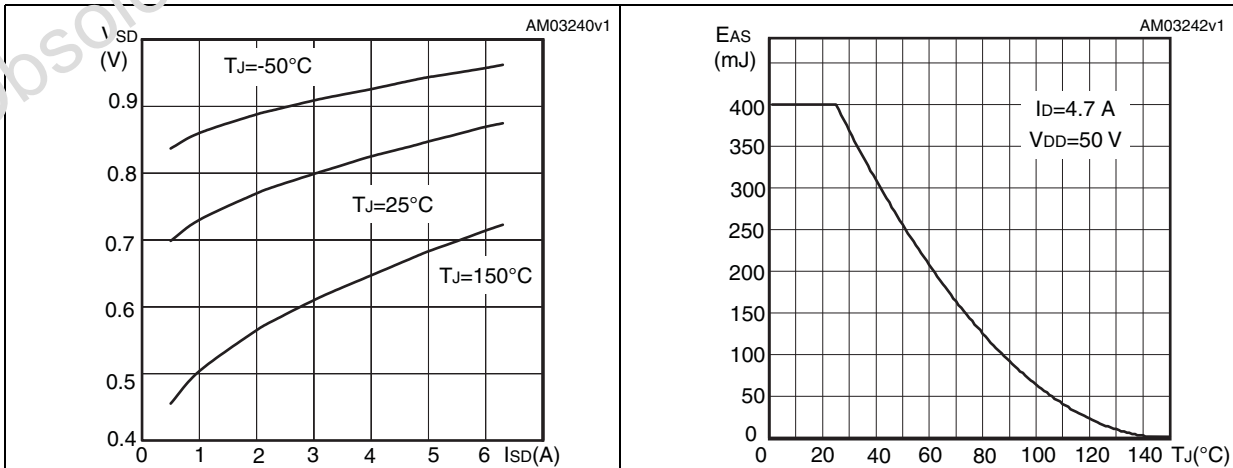
**Figure 8. Gate charge vs gate-source voltage** **Figure 9. Capacitance variations**



**Figure 10. Normalized gate threshold voltage vs temperature** **Figure 11. Normalized on resistance vs temperature**



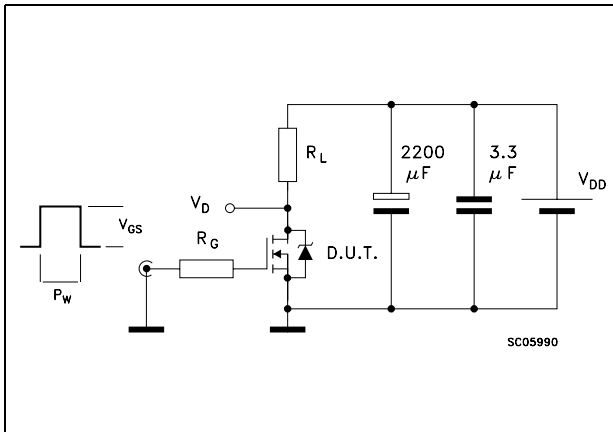
**Figure 12. Source-drain diode forward characteristics** **Figure 13. Maximum avalanche energy vs temperature**



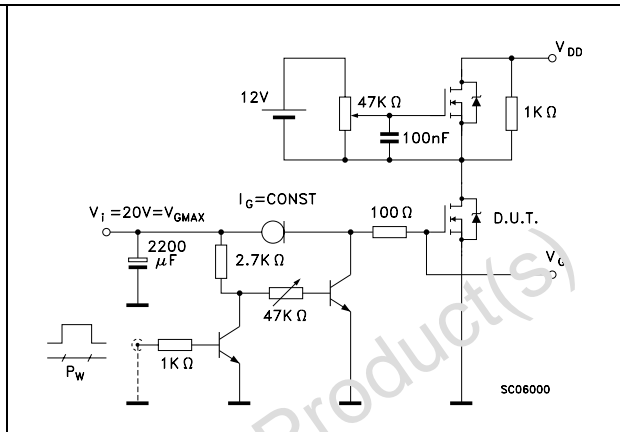


### 3 Test circuits

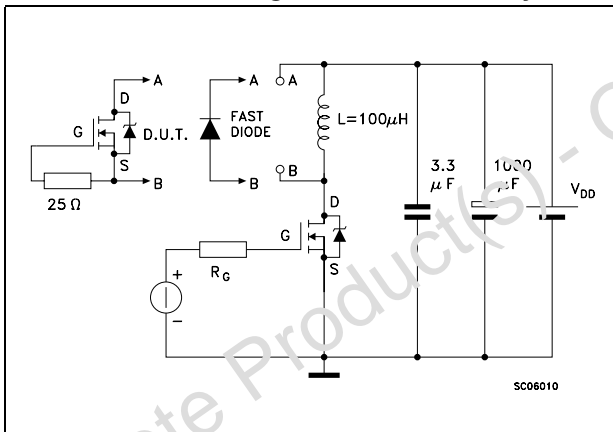
**Figure 14. Switching times test circuit for resistive load**



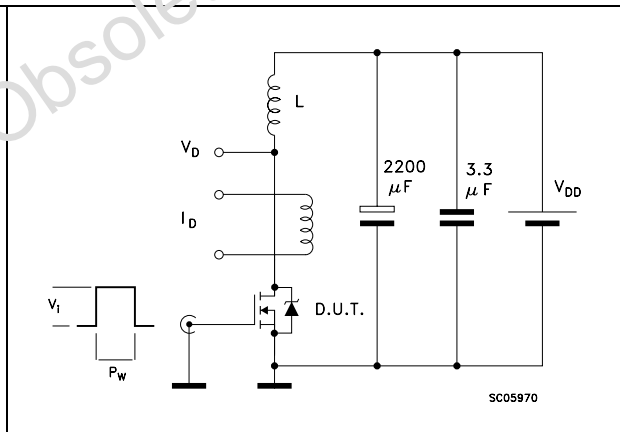
**Figure 15. Gate charge test circuit**



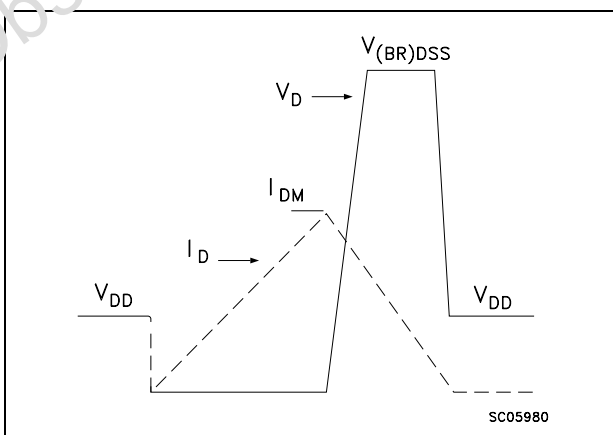
**Figure 16. Test circuit for inductive load switching and diode recovery times**



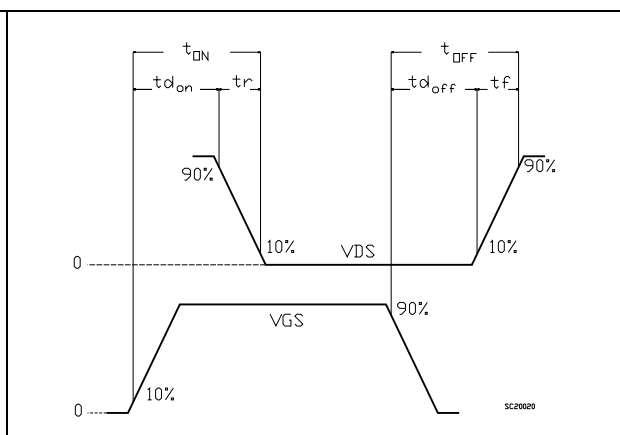
**Figure 17. Unclamped inductive load test circuit**



**Figure 18. Unclamped inductive waveform**



**Figure 19. Switching time waveform**



## 4 Package mechanical data

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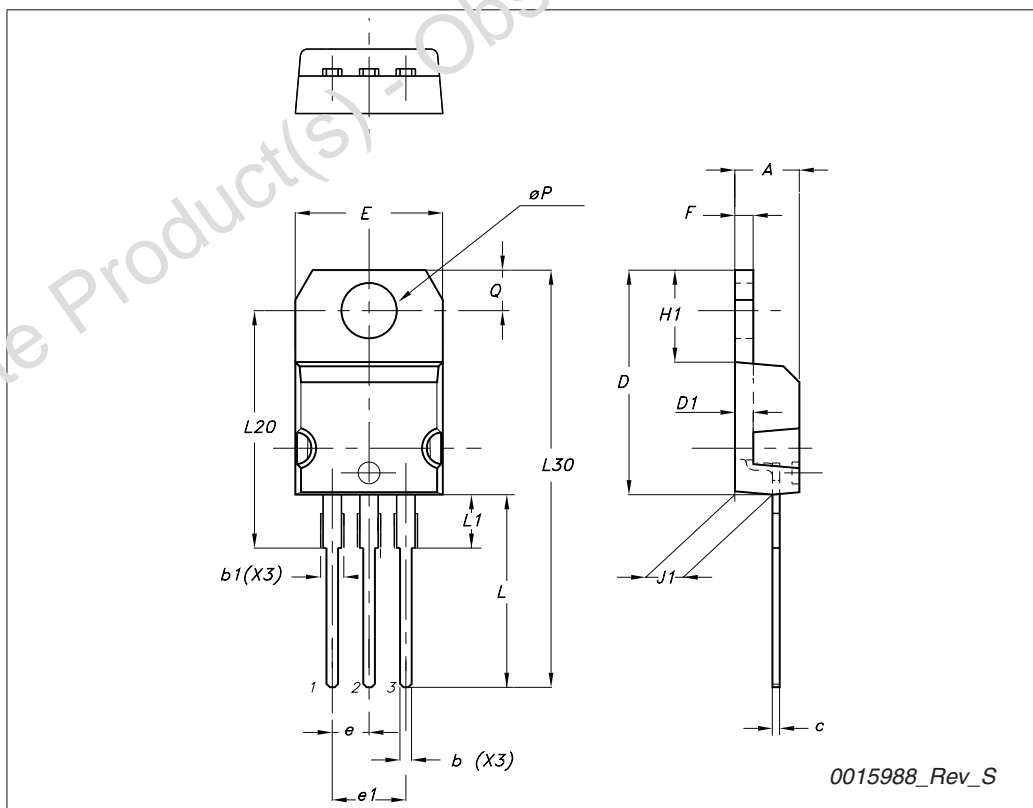
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Package mechanical data

STP5N120

TO-220 type A mechanical data

Dim	mm		
	Min	Typ	Max
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		13.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95



## 5 Revision history

Table 10. Revision history

Date	Revision	Changes
21-May-2007	1	First release
02-Nov-2009	2	Document status promoted from preliminary data to datasheet. Updated mechanical data.

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