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# STL15N3LLH5

N-channel 30 V, 0.0045 Ω, 15 A, PowerFLAT™ (3.3 x 3.3)  
 STripFET™ V Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub>
STL15N3LLH5	30 V	< 0.0054 Ω	15 A <sup>(1)</sup>

1. The value is rated according R<sub>thj-pcb</sub>

- R<sub>DS(on)</sub> \* Q<sub>g</sub> industry benchmark
- Extremely low on-resistance R<sub>DS(on)</sub>
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses

## Applications

- Switching applications

## Description

This product utilizes the 5<sup>th</sup> generation of design rules of ST's proprietary STripFET™ technology. The lowest available R<sub>DS(on)</sub>\*Q<sub>g</sub>, in this chip scale package, makes this device suitable for the most demanding DC-DC converter applications, where high power density is to be achieved.

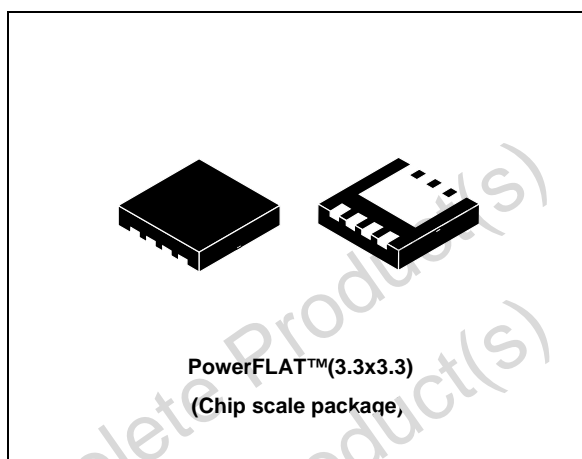


Figure 1. Internal schematic diagram

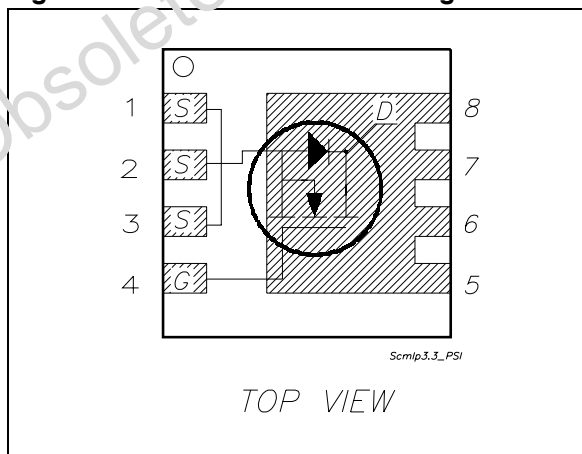


Table 1. Device summary

Order code	Marking	Package	Packaging
STL15N3LLH5	15N3L	PowerFLAT™ (3.3 x 3.3)	Tape and reel

## Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
2.1	Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuits</b> .....	<b>8</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>9</b>
<b>5</b>	<b>Revision history</b> .....	<b>11</b>

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	30	V
$V_{GS}$	Gate-source voltage	$\pm 22$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	15	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	9.3	A
$I_{DM}^{(2)}$	Drain current (pulsed)	60	A
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	50	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	2	W
	Derating factor	0.4	W/ $^\circ\text{C}$
$T_J$ $T_{stg}$	Operating junction temperature storage temperature	-55 to 150	$^\circ\text{C}$

1. The value is rated according  $R_{thj-pcb}$
2. Pulse width limited by safe operating area.
3. The vaule is rated according  $R_{thj-c}$

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (drain)	2.5	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	42.8	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(2)}$	Thermal resistance junction-pcb	63.5	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10\text{sec}$
2. Steady state

Electrical characteristics

STL15N3LLH5

## 2 Electrical characteristics

(T<sub>CASE</sub>=25°C unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	30			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max rating, V <sub>DS</sub> = Max rating @125 °C			1 10	μA μA
I <sub>GSS</sub>	Gate body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 22 V			±100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1		2.5	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7.5 A V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 7.5 A		0.0045 0.006	0.0054 0.007	Ω Ω

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0		1500		pF
C <sub>oss</sub>	Output capacitance			295		pF
C <sub>rss</sub>	Reverse transfer capacitance			39		pF
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 15 A		12		nC
Q <sub>gs</sub>	Gate-source charge	V <sub>GS</sub> = 4.5 V		4		nC
Q <sub>gd</sub>	Gate-drain charge	(see Figure 14)		4.7		nC
R <sub>G</sub>	Gate input resistance	f = 1 MHz Gate DC Bias = 0 Test signal level = 20 mV Open drain	0.5	1.5	2.5	Ω

STL15N3LLH5

Electrical characteristics

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15\text{ V}$ , $I_D=7.5\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=4.5\text{ V}$ <i>(see Figure 13)</i>		9.3		ns
$t_r$	Rise time			14.5		ns
$t_{d(off)}$	Turn-off delay time			22.7		ns
$t_f$	Fall time			4.5		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				15	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				60	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=15\text{ A}$ , $V_{GS}=0$			1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD}=15\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}=20\text{ V}$ , $T_j=150\text{ }^\circ\text{C}$ <i>(see Figure 18)</i>		25		ns
$Q_{rr}$	Reverse recovery charge			17.5		nC
$I_{RRM}$	Reverse recovery current			1.4		A

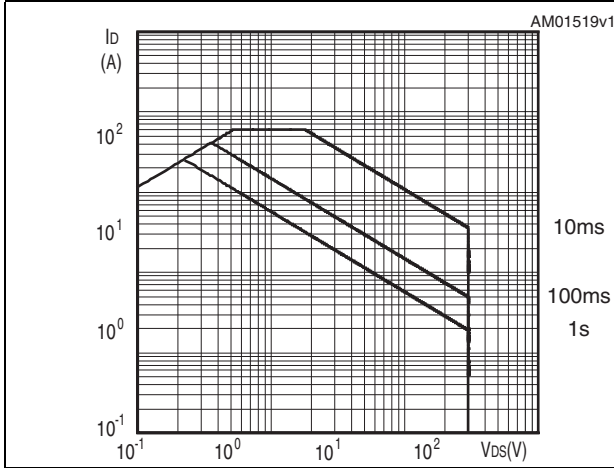
1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

**Electrical characteristics**

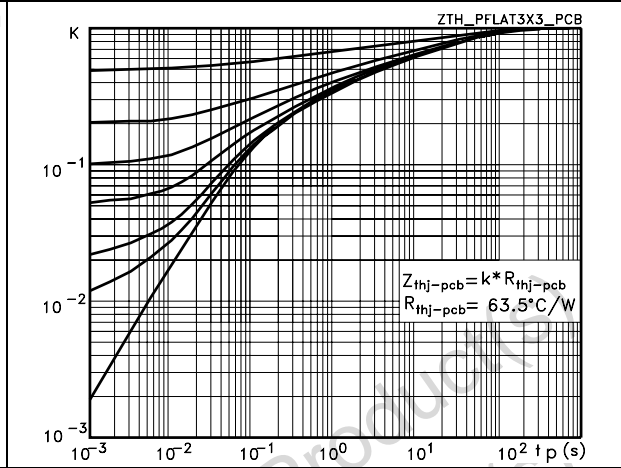
**STL15N3LLH5**

**2.1 Electrical characteristics (curves)**

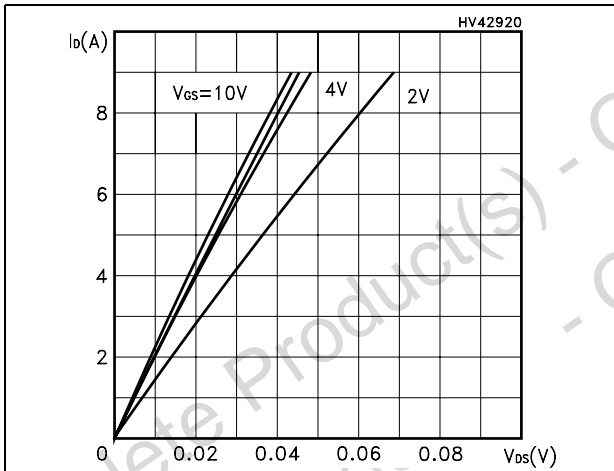
**Figure 2. Safe operating area**



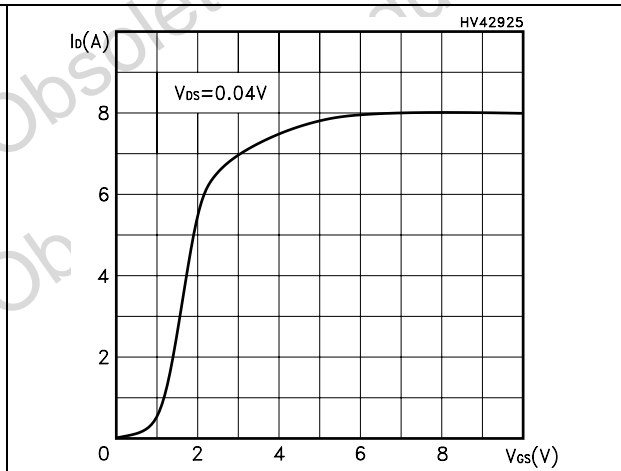
**Figure 3. Thermal impedance**



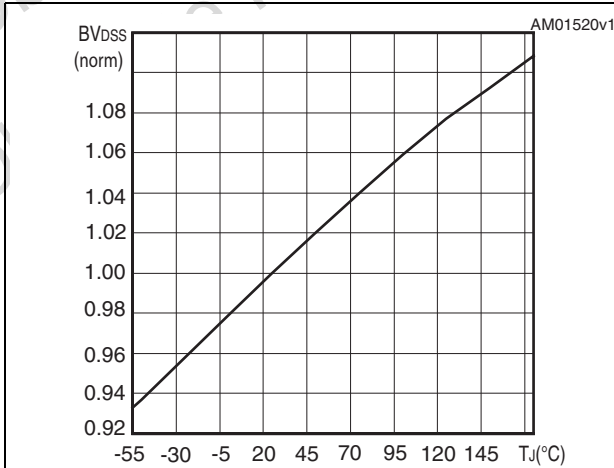
**Figure 4. Output characteristics**



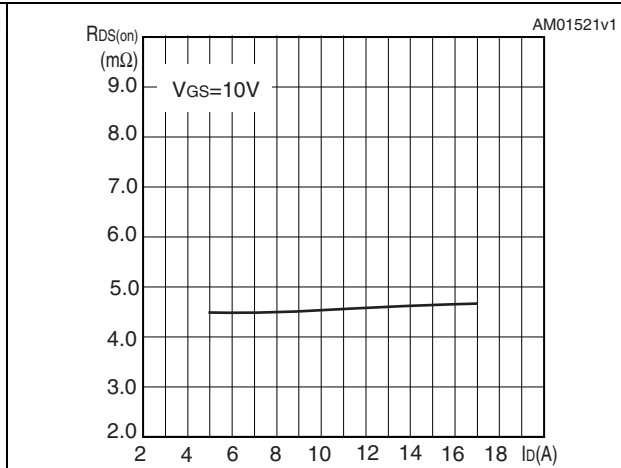
**Figure 5. Transfer characteristics**



**Figure 6. Normalized BV<sub>DSS</sub> vs temperature**



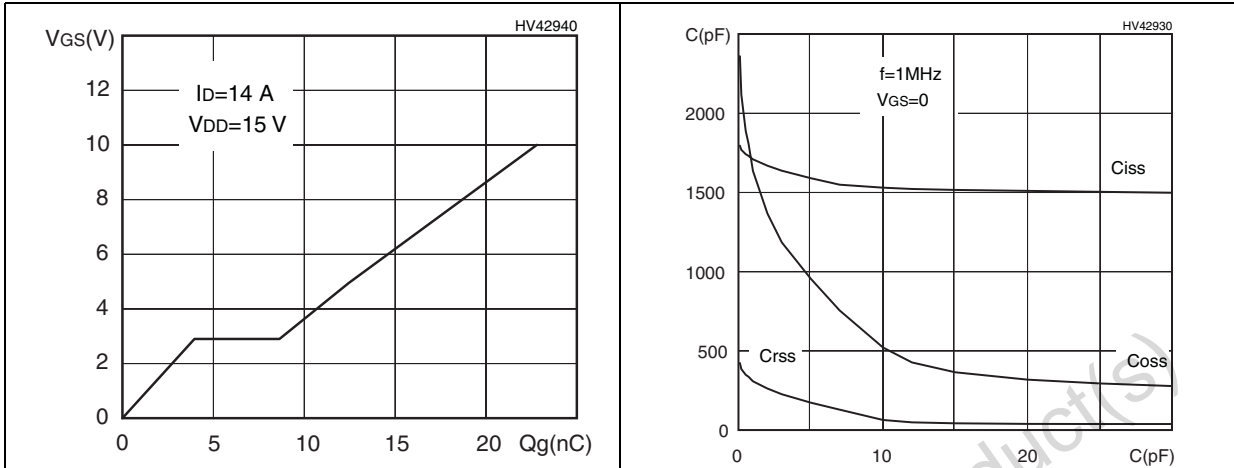
**Figure 7. Static drain-source on resistance**



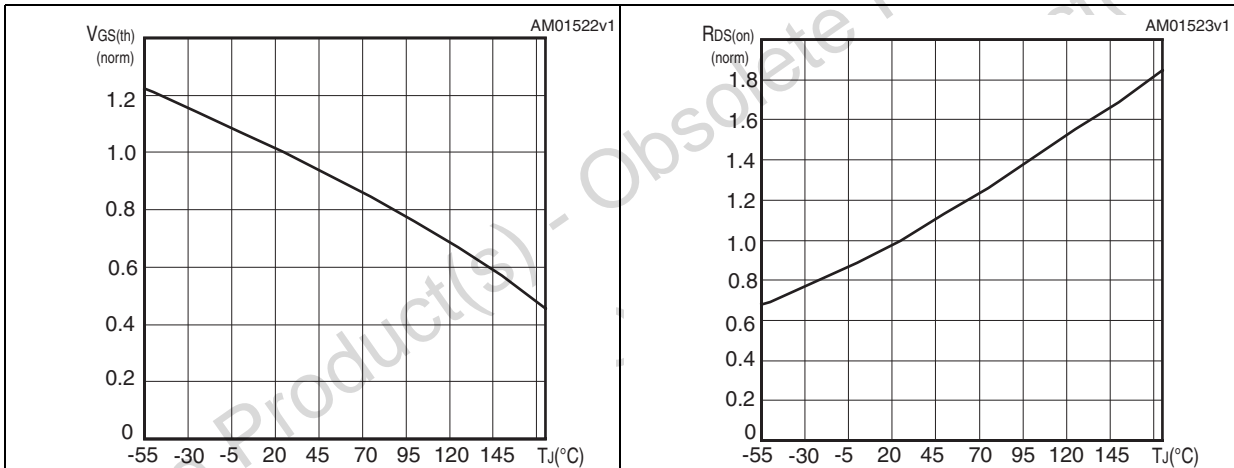
**STL15N3LLH5**

**Electrical characteristics**

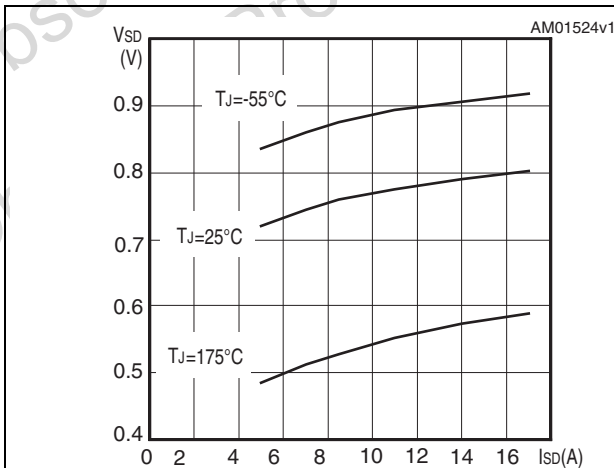
**Figure 8. Gate charge vs gate-source voltage** **Figure 9. Capacitance variations**



**Figure 10. Normalized gate threshold voltage vs temperature** **Figure 11. Normalized on resistance vs temperature**



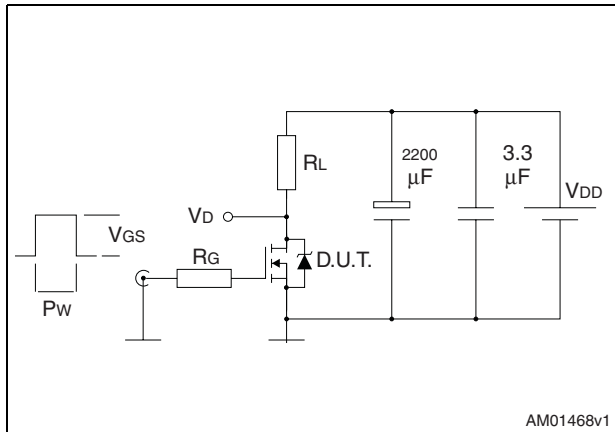
**Figure 12. Source-drain diode forward characteristics**



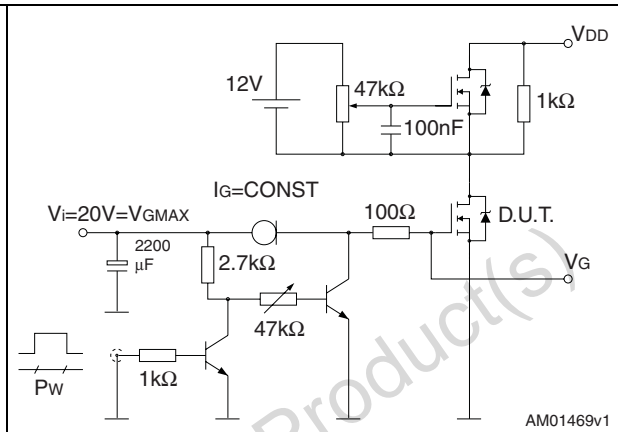


### 3 Test circuits

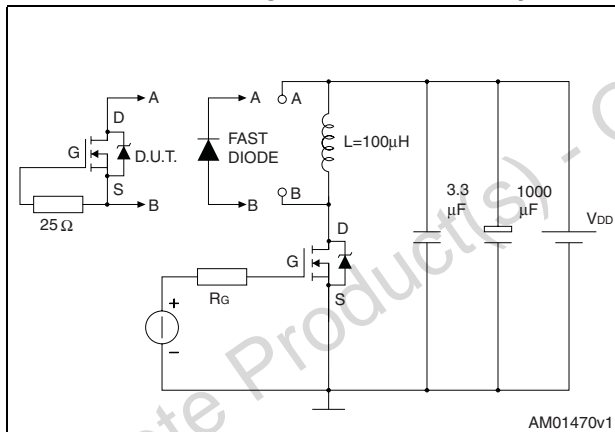
**Figure 13. Switching times test circuit for resistive load**



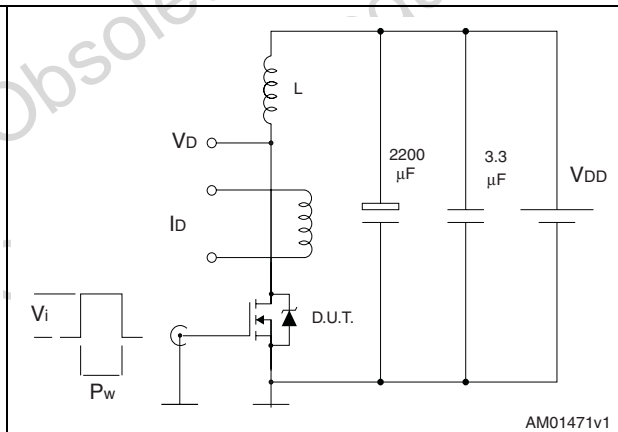
**Figure 14. Gate charge test circuit**



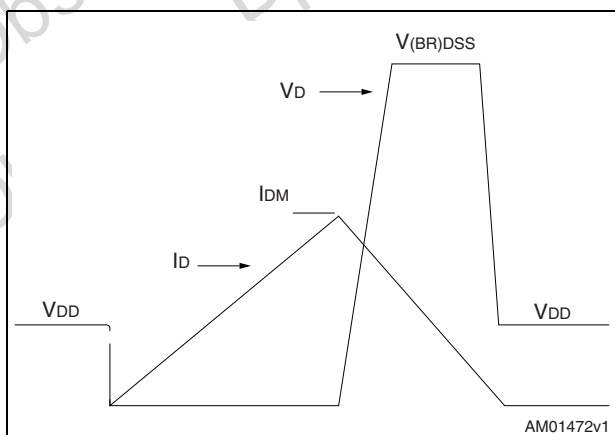
**Figure 15. Test circuit for inductive load switching and diode recovery times**



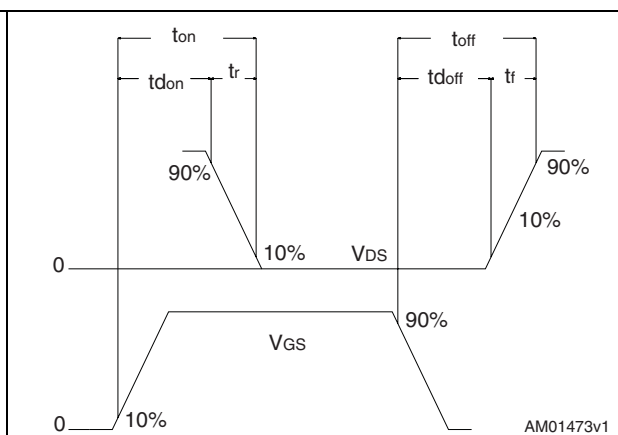
**Figure 16. Unclamped inductive load test circuit**



**Figure 17. Unclamped inductive waveform**



**Figure 18. Switching time waveform**



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

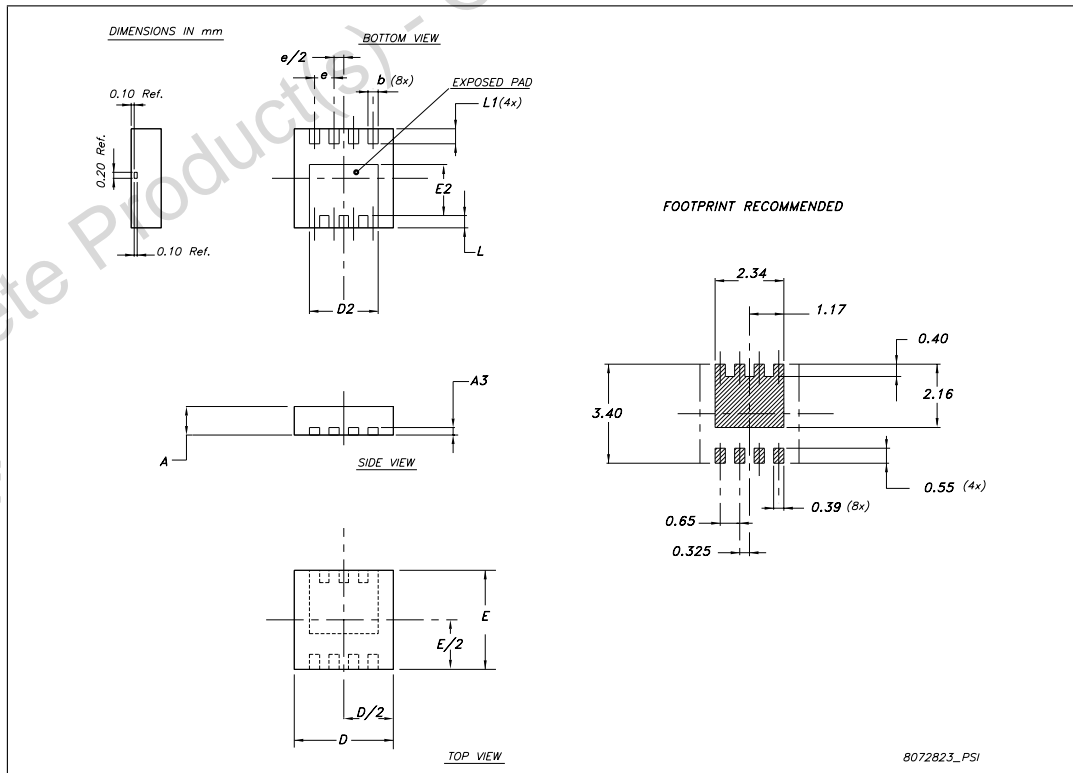
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**Package mechanical data**

**STL15N3LLH5**

**PowerFLAT™ ( 3.3 x 3.3) mechanical data**

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	0.950		1.000	0.037		0.039
A3		0.200			0.008	
b	0.29	0.34	0.39	0.011	0.013	0.015
D	3.200	3.300	3.400	0.126	0.123	0.134
D2	2.24	2.29	2.34	0.088	0.090	0.092
E	2.20	3.30	3.40	0.086	0.123	0.1338
E2	1.660	1.710	1.760	0.065	0.067	0.069
e		0.650			0.025	
L		0.40			0.0157	
L1	0.45	0.50	0.55	0.017	0.0196	0.021



## 5 Revision history

Table 8. Document revision history

Date	Revision	Changes
25-Aug-2008	1	First release
04-Nov-2008	2	Document status promoted from preliminary data to datasheet.

Obsolete Product(s) - Obsolete Product(s)  
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