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Fairchild Semiconductor
FDPF10N50FT

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November 2013

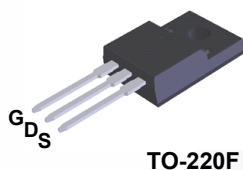# FDPF10N50FT
N-Channel UniFET™ FRFET® MOSFET
500 V, 9 A, 850 mΩ

Features

- $R_{DS(on)}$ = 710 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 4.5 A
- Low Gate Charge (Typ. 18 nC)
- Low C_{rss} (Typ. 10 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- RoHS Compliant

Applications

- LCD/LED/PDP TV
- Lighting
- Uninterruptible Power Supply

Description

UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. The body diode's reverse recovery performance of UniFET FRFET® MOSFET has been enhanced by lifetime control. Its t_{rr} is less than 100nsec and the reverse dv/dt immunity is 15V/ns while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore, it can remove additional component and improve system reliability in certain applications in which the performance of MOSFET's body diode is significant. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

TO-220F
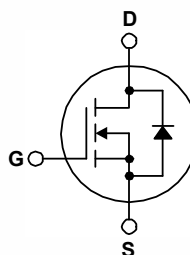
MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter			FDPF10N50FT	Unit
V_{DSS}	Drain to Source Voltage			500	V
V_{GSS}	Gate to Source Voltage			±30	V
I_D	Drain Current	- Continuous (T_C = 25°C)		9*	A
		- Continuous (T_C = 100°C)		5.4*	
I_{DM}	Drain Current	- Pulsed	(Note 1)	36*	A
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	364	mJ
I_{AR}	Avalanche Current		(Note 1)	9	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	12.5	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	20	V/ns
P_D	Power Dissipation	(T_C = 25°C)		42	W
		- Derate Above 25°C		0.33	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds			300	°C

*Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	FDPF10N50FT	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDPF10N50FT	FDPF10N50FT	TO-220F	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu A$, $V_{GS} = 0\ V$, $T_J = 25^oC$	500	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu A$, Referenced to 25^oC	-	0.5	-	V/^oC
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500\ V$, $V_{GS} = 0\ V$	-	-	10	μA
		$V_{DS} = 400\ V$, $T_C = 125^oC$	-	-	100	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30\ V$, $V_{DS} = 0\ V$	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu A$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ V$, $I_D = 4.5\ A$	-	0.71	0.85	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20\ V$, $I_D = 4.5\ A$	-	8.5	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25\ V$, $V_{GS} = 0\ V$, $f = 1\ MHz$	-	880	1170	pF
C_{oss}	Output Capacitance		-	120	160	pF
C_{rss}	Reverse Transfer Capacitance		-	10	15	pF
Q_g	Total Gate Charge at 10V	$V_{DS} = 400\ V$, $I_D = 10\ A$, $V_{GS} = 10\ V$	-	18	24	nC
Q_{gs}	Gate to Source Gate Charge		-	5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note 4)	-	7.5	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\ V$, $I_D = 10\ A$, $V_{GS} = 10\ V$, $R_G = 25\ \Omega$	-	20	50	ns
t_r	Turn-On Rise Time		-	40	90	ns
$t_{d(off)}$	Turn-Off Delay Time		-	45	100	ns
t_f	Turn-Off Fall Time	(Note 4)	-	30	70	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	9	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	60	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\ V$, $I_{SD} = 9\ A$	-	-	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\ V$, $I_{SD} = 9\ A$, $dI_F/dt = 100\ A/\mu s$	-	95	-	ns
Q_{rr}	Reverse Recovery Charge		-	0.2	-	μC

Notes:
1: Repetitive rating: pulse-width limited by maximum junction temperature.
2: $L = 9\ mH$, $I_{AS} = 9\ A$, $V_{DD} = 50\ V$, $R_G = 25\ \Omega$, starting $T_J = 25°C$.
3: $I_{SD} \leq 8\ A$, di/dt $\leq 200\ A/\mu s$, $V_{DD} \leq BV_{DSS}$, starting $T_J = 25°C$.
4: Essentially independent of operating temperature typical characteristics.

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Typical Performance Characteristics

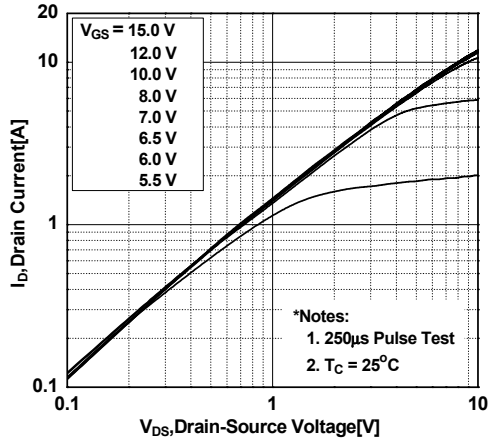### Figure 1. On-Region Characteristics

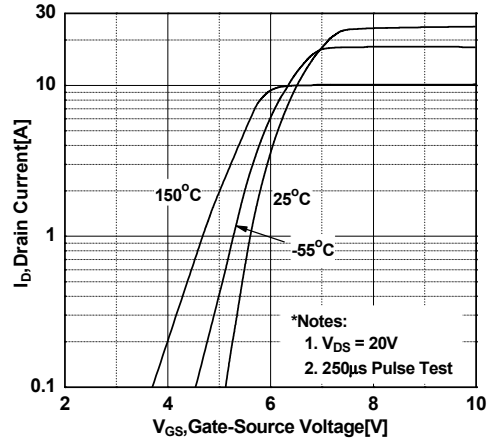### Figure 2. Transfer Characteristics

Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage
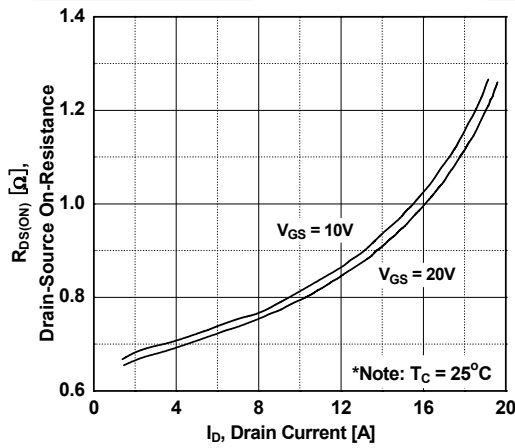

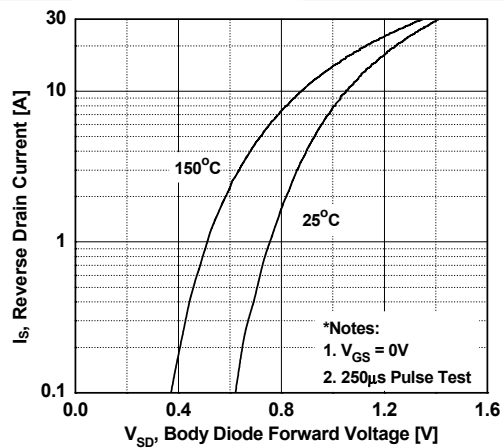### Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature
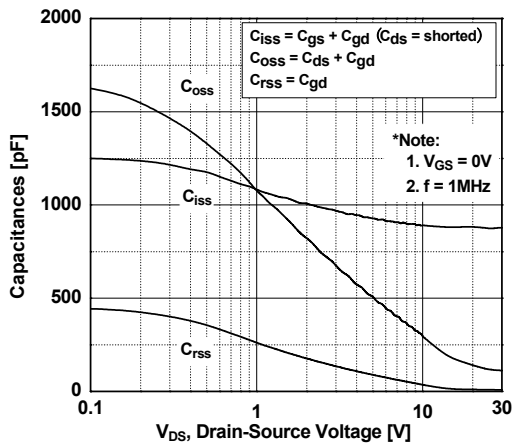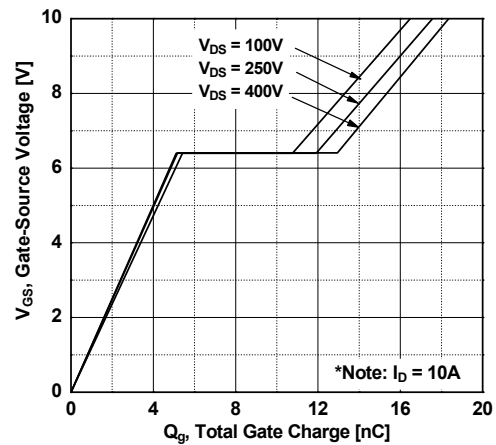

Figure 5. Capacitance Characteristics

Figure 6. Gate Charge Characteristics

FDPF10N50FT — N-Channel UniFET™ FRFET® MOSFET

Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

*Notes:
1. V_{GS} = 0V
2. I_D = 250µA
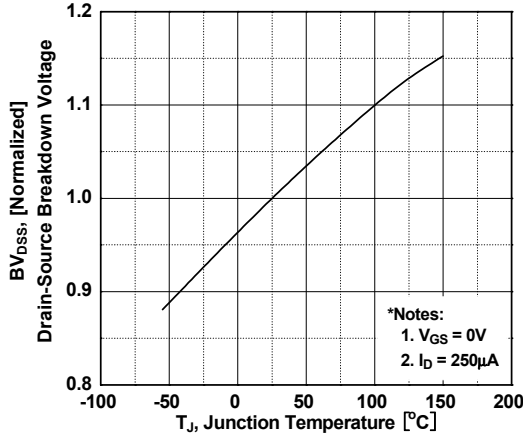
Figure 8. Maximum Safe Operating Area

20µs
100µs
1ms
10ms
DC

Operation in This Area is Limited by $R_{DS(on)}$

*Notes:
1. T_C = 25°C
2. T_J = 150°C
3. Single Pulse
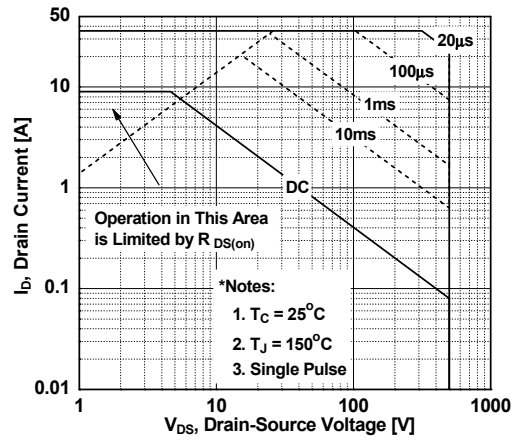
Figure 9. Maximum Drain Current vs. Case Temperature
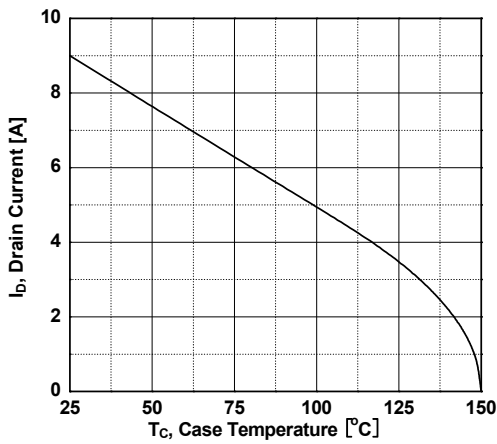
Figure 10. Transient Thermal Response Curve

0.5
0.2
0.1
0.05
0.02
0.01
Single pulse

P_{DM}
t_1
t_2

*Notes:
1. $Z_{\theta JC}(t)$ = 3.0°C/W Max.
2. Duty Factor, D= t_1/t_2
3. $T_{JM} - T_C = P_{DM} * Z_{\theta JC}(t)$
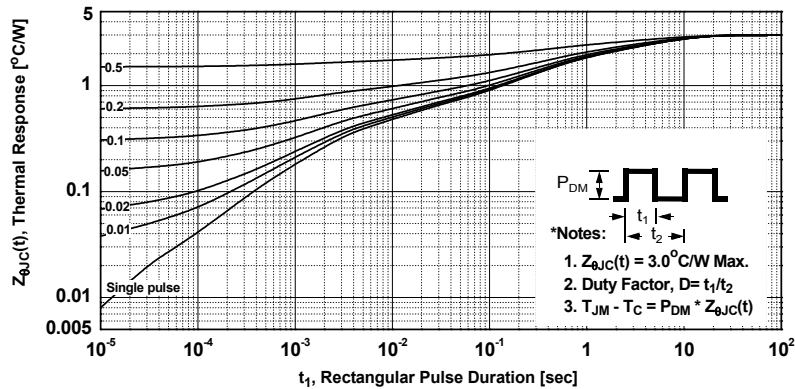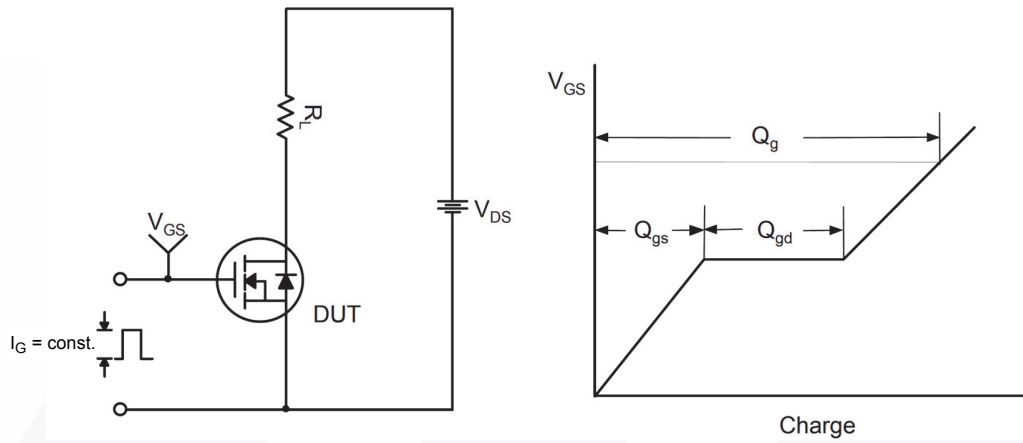
Figure 11. Gate Charge Test Circuit & Waveform
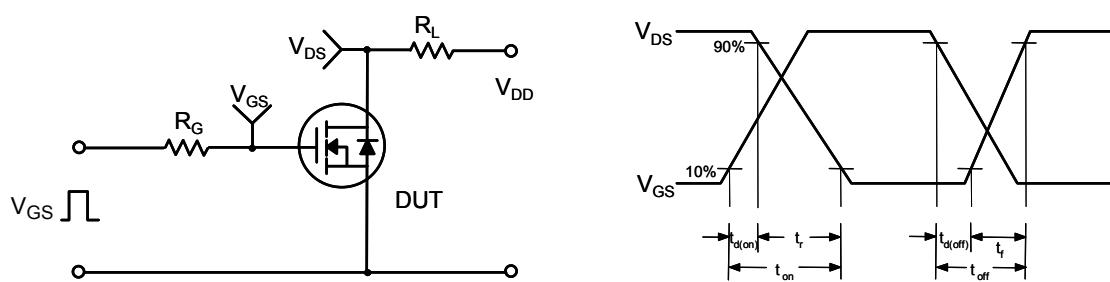
Figure 12. Resistive Switching Test Circuit & Waveforms

$$E_{AS} = \frac{1}{2} L I_{AS}^2$$
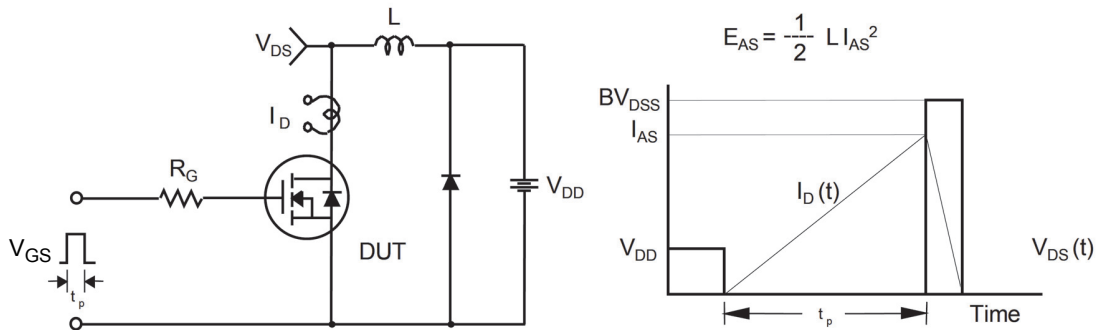
Figure 13. Unclamped Inductive Switching Test Circuit & Waveforms

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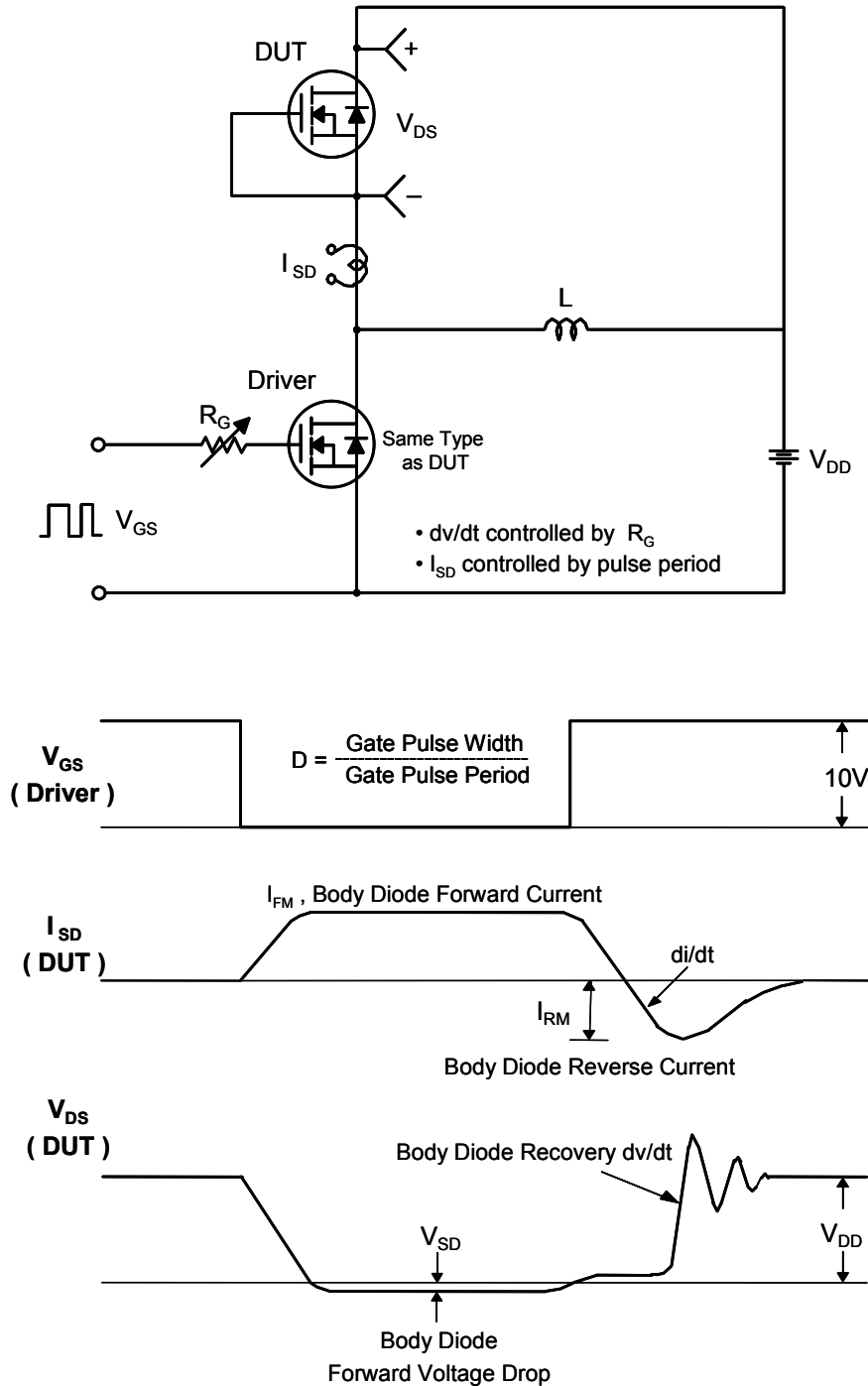
Figure 14. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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Mechanical Dimensions
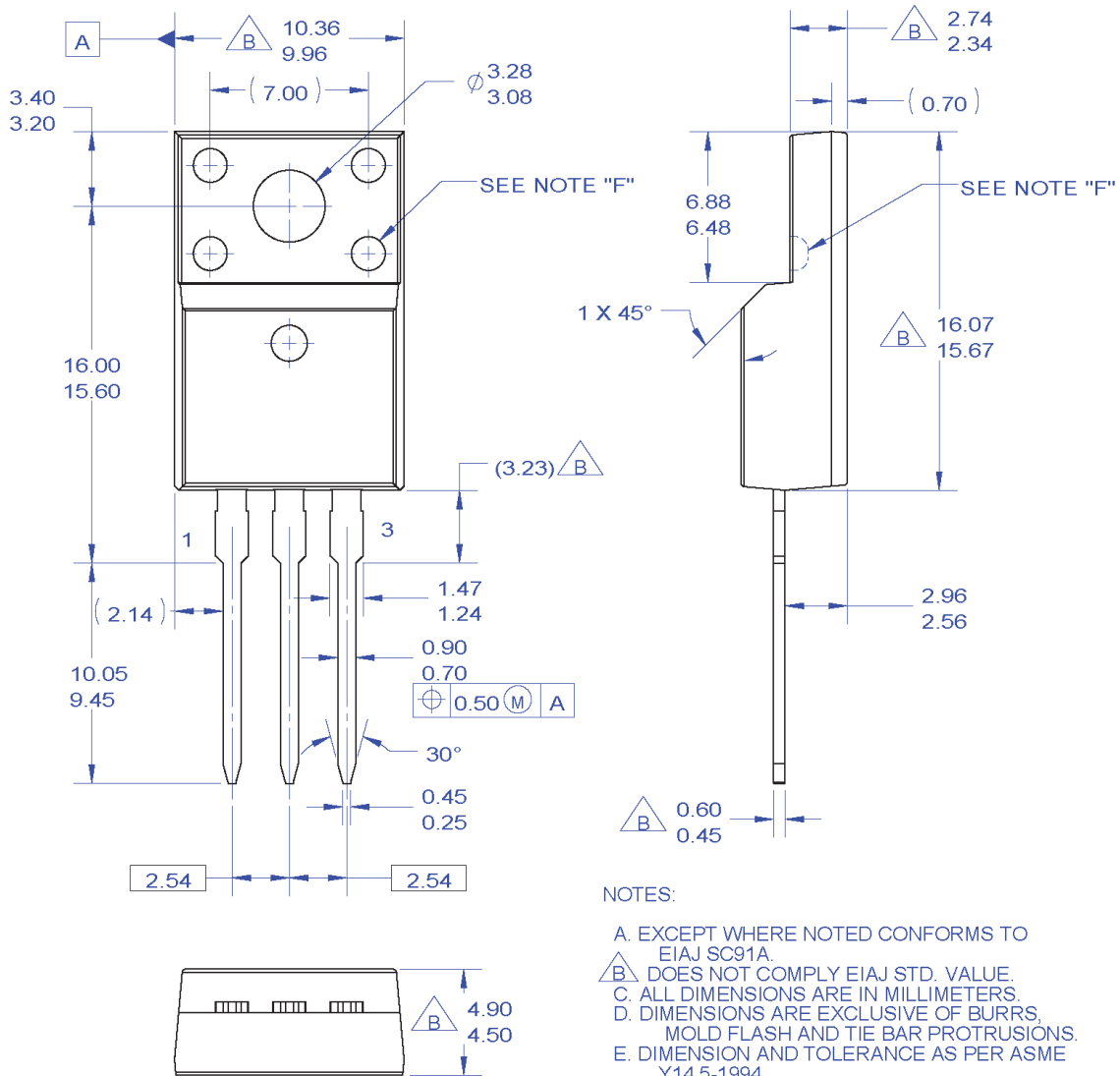
NOTES:

A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
B. DOES NOT COMPLY EIAJ STD. VALUE.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
F. OPTION 1 - WITH SUPPORT PIN HOLE.
   OPTION 2 - NO SUPPORT PIN HOLE.
G. DRAWING FILE NAME: TO220M03REV3

Figure 15. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead

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FPS™		SyncFET™	XS™

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I66