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Maxim Integrated
MAX17108ETI+

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RELIABILITY REPORT

FOR

MAX17108ETI+

PLASTIC ENCAPSULATED DEVICES

May 4, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
Ken Wendel
Quality Assurance
Director, Reliability Engineering

Conclusion

The MAX17108ETI+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX17108 includes a 10-channel high-voltage level-shifting scan driver and a VCOM amplifier. The device is optimized for thin-film transistor (TFT) liquid-crystal display (LCD) applications. The high-voltage level-shifting scan driver can swing from +38V to -12V and can swiftly drive capacitive loads. There are two positive supply inputs, which provide flexibility for system design. The operational amplifier features rail-to-rail output, high short-circuit output current, fast slew rate, and wide bandwidth. The MAX17108 is available in a 28-pin, 5mm x 5mm, lead-free thin QFN package with a maximum thickness of 0.8mm for thin LCD panels.

II. Manufacturing Information

A. Description/Function:	10-Channel High-Voltage Scan Driver and VCOM Amplifier for TFT LCD Panels
B. Process:	S45URS
C. Number of Device Transistors:	2918
D. Fabrication Location:	Texas
E. Assembly Location:	UTL Thailand
F. Date of Initial Production:	October 21, 2008

III. Packaging Information

A. Package Type:	28-pin TQFN 5x5
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Au (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	47°C/W
K. Single Layer Theta Jc:	2.1°C/W
L. Multi Layer Theta Ja:	29°C/W
M. Multi Layer Theta Jc:	2.1°C/W

IV. Die Information

A. Dimensions:	60 X 128 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide
C. Interconnect:	Aluminum/0.5% Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 46 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 23.3 \times 10^{-9}$

$\lambda = 23.3$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the S45URS Process results in a FIT Rate of 0.9 @ 25C and 13.84 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The PF52 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500 V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100 mA, 1.5X VCCMax Overvoltage per JESD78.

Table 1
Reliability Evaluation Test Results

MAX17108ETI+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	47	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data