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SN761640DBTR

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DIGITAL TV TUNER IC

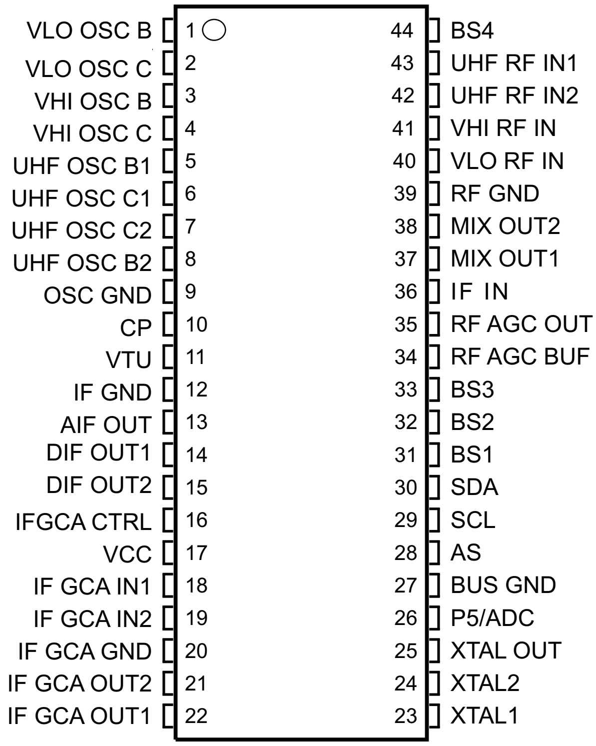
FEATURES

- **Integrated Mixer/Oscillator/PLL and IF GCA**
- **VHF-L, VHF-H, UHF 3-Band Local Oscillator**
- **RF AGC Detector Circuit**
- **I²C Bus Protocol
  Bidirectional Data Transmission**
- **High-Voltage Tuning Voltage Output**
- **Four NPN-Type Band Switch Drivers**
- **One Auxiliary Port/5-Level ADC**
- **Crystal Oscillator Output**
- **Programmable Reference Divider Ratio (24/28/32/64/80/128)**
- **IF GCA Enable/Disable Control**
- **Selectable digital IFOUT and Analog IFOUT**
- **Standby Mode**
- **5-V Power Supply**
- **44-Pin Thin Shrink Small-Outline Package (TSSOP)**

APPLICATIONS

- **Digital TVs**
- **Digital CATVs**
- **Set-Top Boxes**

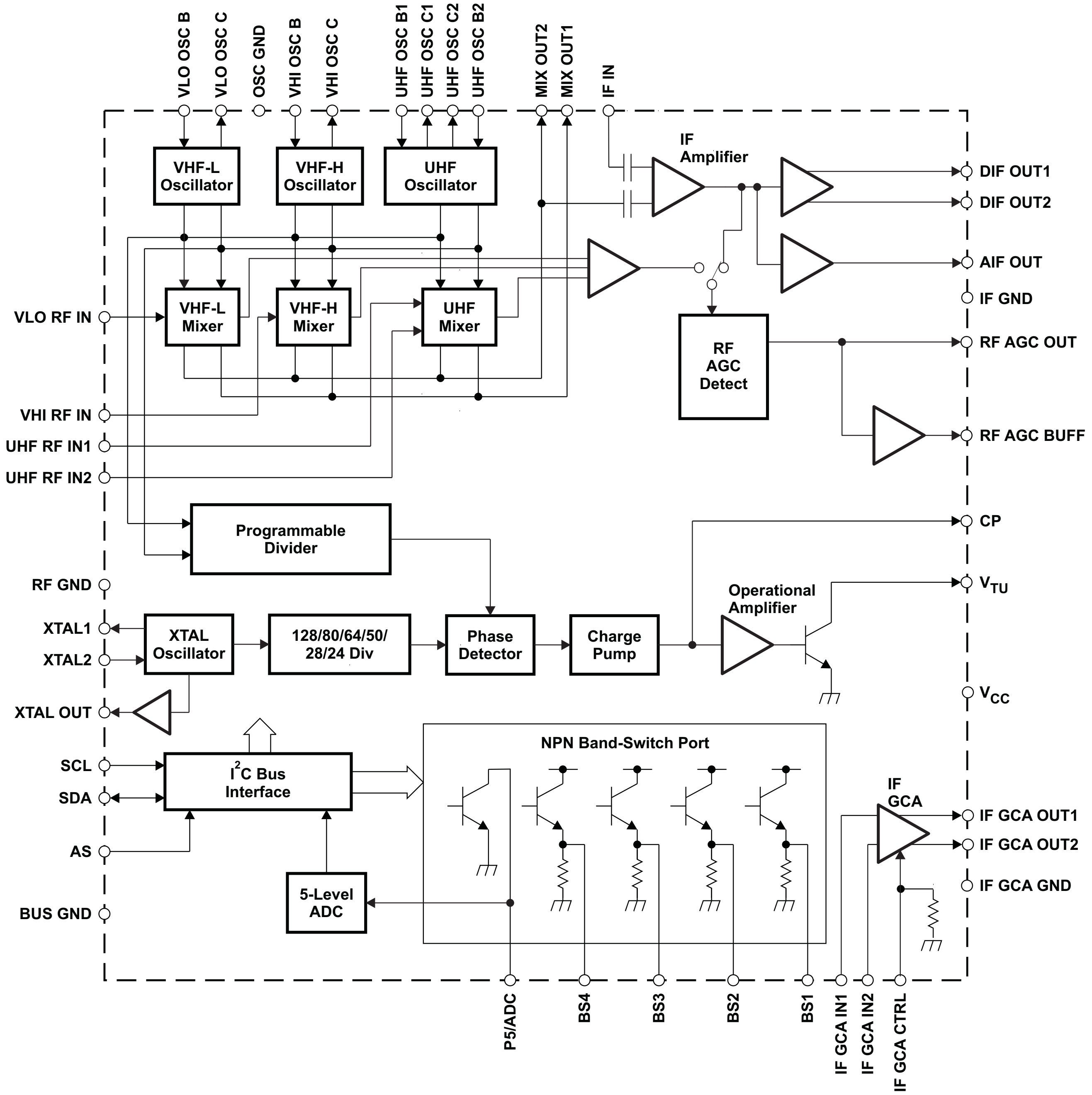
**DBT PACKAGE
(TOP VIEW)**



DESCRIPTION

The SN761640 is a low-phase-noise synthesized tuner IC designed for digital TV tuning systems. The circuit consists of a PLL synthesizer, three-band local oscillator and mixer, RF AGC detector circuit, and IF gain-controlled amplifier. The SN761640 is available in a small-outline package.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION	SCHEMATIC
NAME	NO.		
AIF OUT	13	IF amplifier output (analog)	Figure 8
AS	28	Address selection input	Figure 1
BS1	31	Band switch 1 output	Figure 2
BS2	32	Band switch 2 output	Figure 2
BS3	33	Band switch 3 output	Figure 2
BS4	44	Band switch 4 output	Figure 2
BUS GND	27	BUS ground	
CP	10	Charge-pump output	Figure 3
DIF OUT1	14	IF amplifier output 1	Figure 9
DIF OUT2	15	IF amplifier output 2	Figure 9
IF GCA CTRL	16	IF GCA CTRL voltage inout	Figure 4
IF GCA GND	20	IF GCA ground	
IF GCA IN1	18	IF GCA input 1	Figure 5
IF GCA IN2	19	IF GCA input 2	Figure 5
IF GCA OUT1	22	IF GCA output 1	Figure 6
IF GCA OUT2	21	IF GCA output 2	Figure 6
IF GND	12	IF ground	
IF IN	36	IF amplifier input	Figure 7
MIXOUT1	37	Mixer output 1	Figure 10
MIXOUT2	38	Mixer output 2	Figure 10
OSC GND	9	Oscillator ground	
P5/ADC	26	Port-5 output/ADC input	Figure 11
RF AGC BUF	34	RF AGC buffer output	Figure 12
RF AGC OUT	35	RF AGC output	Figure 13
RF GND	39	RF ground	
SCL	29	Serial clock input	Figure 14
SDA	30	Serial data input/output	Figure 15
UHF OSC B1	5	UHF oscillator base 1	Figure 16
UHF OSC B2	8	UHF oscillator base 2	Figure 16
UHF OSC C1	6	UHF oscillator collector 1	Figure 16
UHF OSC C2	7	UHF oscillator collector 2	Figure 16
UHF RF IN1	43	UHF RF input 1	Figure 17
UHF RF IN2	42	UHF RF input 2	Figure 17
V_{CC}	17	Supply voltage for mixer/oscillator/PLL: 5 V	
VHI OSC B	3	VHF-H oscillator base	Figure 18
VHI OSC C	4	VHF-H oscillator collector	Figure 18
VHI RF IN	41	VHF-H RF input	Figure 19
VLO OSC B	1	VHF-L oscillator base	Figure 20
VLO OSC C	2	VHF-L oscillator collector	Figure 20
VLO RF IN	40	VHF-L RF input	Figure 21
VTU	11	Tuning voltage amplifier output	Figure 3
XTAL1	23	4-MHz crystal oscillator output	Figure 22
XTAL2	24	4-MHz crystal oscillator input	Figure 22
XTALOUT	25	4-MHz crystal oscillator buffer output	Figure 23

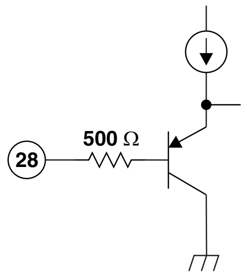


Figure 1. AS

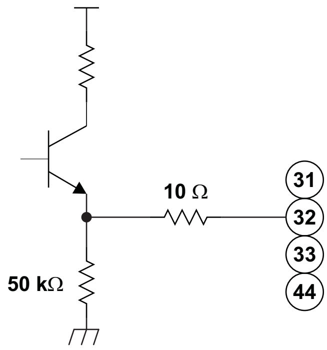


Figure 2. BS1, BS2, BS3, and BS4

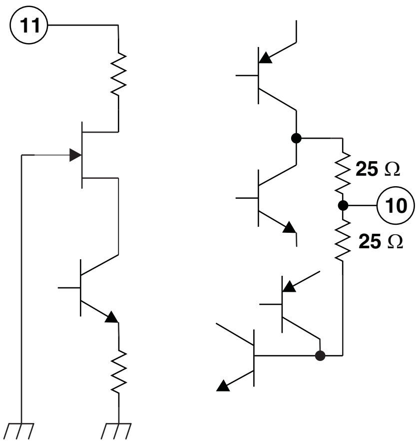


Figure 3. CP and VTU

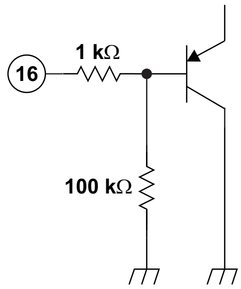


Figure 4. IF GCA CTRL

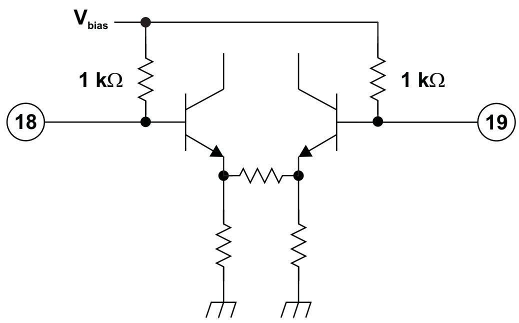


Figure 5. IF GCA IN1 and IF GCA IN2

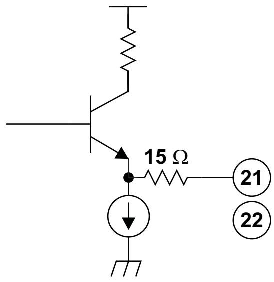


Figure 6. IF GCA OUT1 and IF GCA OUT2

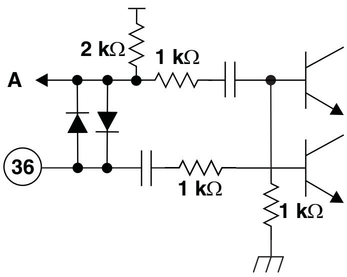


Figure 7. IF IN

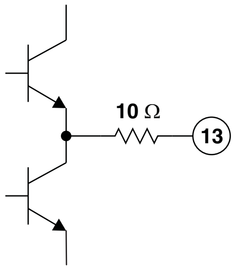


Figure 8. AIF OUT

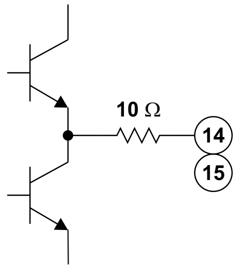


Figure 9. DIF OUT1 and DIF OUT2

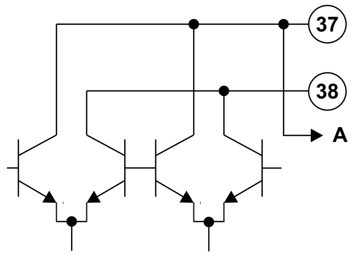


Figure 10. MIXOUT1 and MIXOUT2

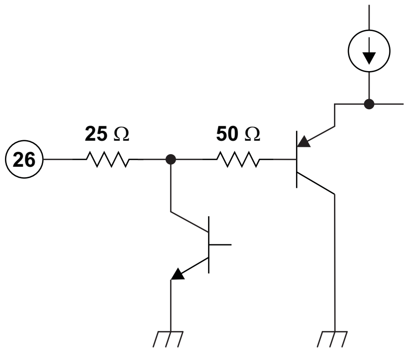


Figure 11. P5/ADC

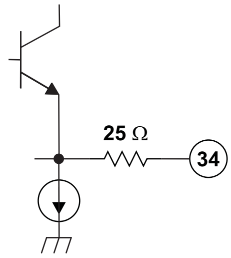


Figure 12. RF AGC BUF

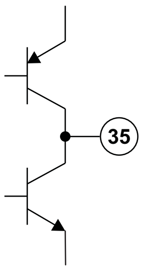


Figure 13. RF AGC OUT

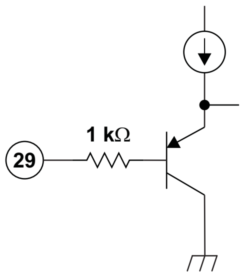


Figure 14. SCL

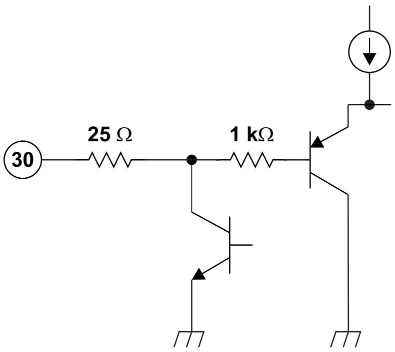


Figure 15. SDA

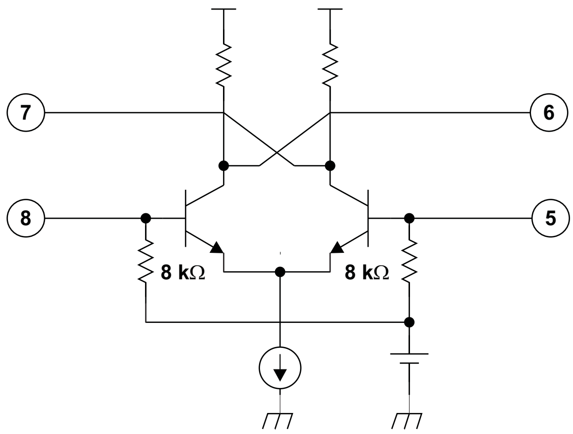


Figure 16. UHF OSC B1, UHF OSC B2, UHF OSC C1, and UHF OSC C2

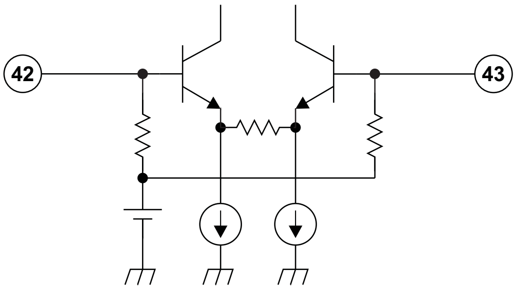


Figure 17. UHF RF IN1 and UHF RF IN2

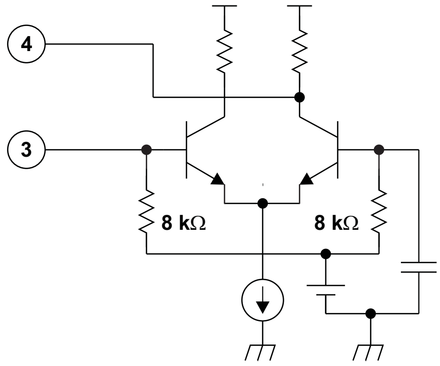


Figure 18. VHI OSC B and VHI OSC C

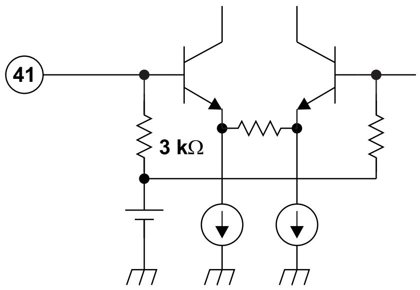


Figure 19. VHI RF IN

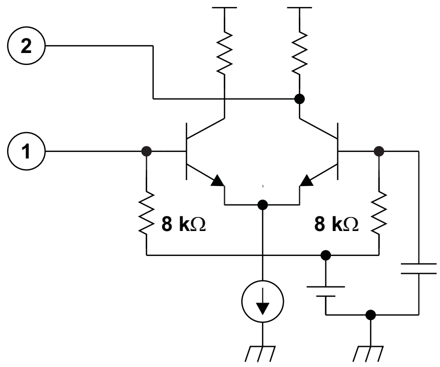


Figure 20. VLO OSC B and VLO OSC C

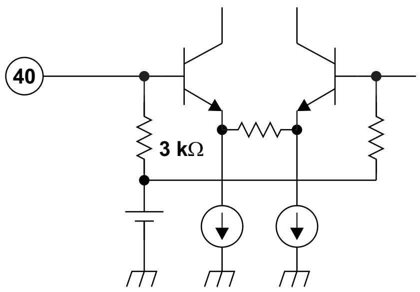


Figure 21. VLO RF IN

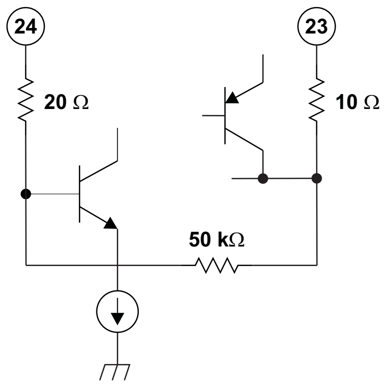


Figure 22. XTAL1 and XTAL2

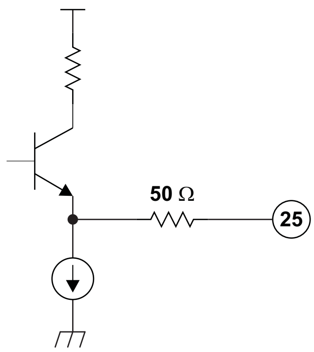


Figure 23. XTALOUT

ABSOLUTE MAXIMUM RATINGS(1)

over recommended operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range (2)	V_{CC}	–0.4	6.5	V
V_{GND}	Input voltage range 1 (2)	RF GND, OSC GND	–0.4	0.4	V
VTU	Input voltage range 2 (2)	VTU	–0.4	35	V
V_{IN}	Input voltage range 3 (2)	Other pins	–0.4	6.5	V
P_D	Continuous total dissipation (3)	$T_A \leq 25°C$		1438	mW
T_A	Operating free-air temperature range		–20	85	°C
T_{stg}	Storage temperature range		–65	150	°C
T_J	Maximum junction temperature			150	°C
$t_{SC(max)}$	Maximum short-circuit time	Each pin to V_{CC} or to GND		10	s

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to the IF GND of the circuit.
(3) Derating factor is 11.5 mW/°C for $T_A \geq 25°C$.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	V_{CC}	4.5	5	5.5	V
VTU	Tuning supply voltage	VTU		30	33	V
I_{BS}	Output current of band switch	BS1 – BS4, one band switch on			10	mA
I_{P5}	Output current of port 5	P5/ADC			–5	mA
T_A	Operating free-air temperature		–20		85	°C

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

IF IN1, MIXOUT1, and MIXOUT2 (pins 36–38) withstand 1.5 kV, and all other pins withstand 2 kV, according to the Human-Body Model (1.5 kΩ, 100 pF).

ELECTRICAL CHARACTERISTICS

Total Device and Serial Interface

V_{CC} = 4.5 V to 5.5 V, T_A = –20°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}1	Supply current 1	BS[1:4] = 0100, IFGCA disabled		90	120	mA
I_{CC}2	Supply current 2	BS[1:4] = 0100, IFGCA enabled		115	145	mA
I_{CC}3	Supply current 3	BS[1:4] = 0100, IFGCA enabled, I_{BS} = 10 mA		125	155	mA
$I_{CC-STBY}$	Standby supply current	BS[1:4] = 1100		9		mA
V_{IH}	High-level input voltage (SCL, SDA)		2.3			V
V_{IL}	Low-level input voltage (SCL, SDA)				1.05	V
I_{IH}	High-level input current (SCL, SDA)				10	µA
I_{IL}	Low-level input current (SCL, SDA)		–10			µA
V_{POR}	Power-on-reset supply voltage (threshold of supply voltage between reset and operation mode)		2.1	2.8	3.5	V
I²C Interface						
V_{ASH}	Address-select high-input voltage (AS)	V_{CC} = 5 V	4.5		5	V
V_{ASM1}	Address-select mid-input 1 voltage (AS)	V_{CC} = 5 V	2		3	V
V_{ASM2}	Address-select mid-input 2 voltage (AS)	V_{CC} = 5 V	1		1.5	V
V_{ASL}	Address-select low-input voltage (AS)	V_{CC} = 5 V			0.5	V
I_{ASH}	Address-select high-input current (AS)				50	µA
I_{ASL}	Address-select low-input current (AS)		–10			µA
V_{ADC}	ADC input voltage	See Table 10	0		V_{CC}	V
I_{ADH}	ADC high-level input current	V_{ADC} = V_{CC}			10	µA
I_{ADL}	ADC low-level input current	V_{ADC} = 0 V	–10			µA
V_{OL}	Low-level output voltage (SDA)	V_{CC} = 5 V, I_{OL} = 3 mA			0.4	V
I_{SDAH}	High-level output leakage current (SDA)	V_{SDA} = 5.5 V			10	µA
f_{SCL}	Clock frequency (SCL)			100	400	kHz
t_{HD-DAT}	Data hold time	See Figure 24	0		0.9	µs
t_{BUF}	Bus free time		1.3			µs
t_{HD-STA}	Start hold time		0.6			µs
t_{LOW}	SCL-low hold time		1.3			µs
t_{HIGH}	SCL-high hold time		0.6			µs
t_{SU-STA}	Start setup time		0.6			µs
t_{SU-DAT}	Data setup time		0.1			µs
t_r	Rise time (SCL, SDA)				0.3	µs
t_f	Fall time (SCL, SDA)				0.3	µs
t_{SU-STO}	Stop setup time		0.6			µs

PLL and Band Switch

V_{CC} = 4.5 V to 5.5 V, T_A = –20°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
N	Divider ratio	15-bit frequency word	512		32767	
f_{XTAL}	Crystal oscillator frequency	R_{XTAL} = 25 Ω to 300 Ω		4		MHz
Z_{XTAL}	Crystal oscillator input impedance		1.6	2.4		kΩ
V_{XLO}	XTALOUT output voltage	Load = 10 pF/5.1 kΩ, V_{CC} = 5 V, T_A = 25°C		0.4		Vp-p
V_{VTUL}	Tuning amplifier low-level output voltage	R_L = 20 kΩ, VTU = 33 V	0.2	0.3	0.46	V
I_{VTUOFF}	Tuning amplifier leakage current	Tuning amplifier = off, VTU = 33 V			10	µA
I_{CP11}	Charge-pump current	CP[2:0] = 011		600		µA
I_{CP10}		CP[2:0] = 010		350		
I_{CP01}		CP[2:0] = 001		140		
I_{CP00}		CP[2:0] = 000		70		
I_{CP100}		CP[2:0] = 100, Mode = 1		900		
V_{CP}	Charge-pump output voltage	PLL locked		1.95		V
I_{CPOFF}	Charge-pump leakage current	V_{CP} = 2 V, T_A = 25°C	–15		15	nA
I_{BS}	Band switch driver output current (BS1–BS4)				10	mA
V_{BS1}	Band switch driver output voltage (BS1–BS4)	I_{BS} = 10 mA	3			V
V_{BS2}		I_{BS} = 10 mA, V_{CC} = 5 V, T_A = 25°C	3.5	3.7		
I_{BSOFF}	Band switch driver leakage current (BS1–BS4)	V_{BS} = 0 V			8	µA
I_{P5}	Band switch port sink current (P5/ADC)				–5	mA
V_{P5ON}	Band switch port output voltage (P5/ADC)	I_{P5} = –2 mA, V_{CC} = 5 V, T_A = 25°C			0.6	V

RF AGC(1)

V_{CC} = 5 V, T_A = 25°C, measured in Figure 25 reference measurement circuit at 50-Ω system, IF = 44 MHz, IF filter characteristics: f_{peak} = 44 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OAGC0}	RF AGC output source current	ATC = 0		300		nA
I_{OAGC1}		ATC = 1		9		µA
$I_{OAGCSINK}$	RF AGC peak sink current	ATC = 0		100		µA
V_{OAGCH}	RFAGCOUT output high voltage (max level)	ATC = 1	3.5	4	4.5	V
V_{OAGCL}	RFAGCOUT output low voltage (min level)	ATC = 1		0.3		V
I_{AGCBUF}	RFAGCBUF output current	ATC = 0		1.5		mA
$V_{OAGCBFH}$	RFAGCBUF output high voltage (max level)	ATC = 1	3.5	4	4.5	V
$V_{OAGCBFL}$	RFAGCBUF output low voltage (min level)	ATC = 1		0.3		V
$V_{AGCSP00}$	Start-point IF output level	ATP[2:0] = 000		114		dBµV
$V_{AGCSP01}$		ATP[2:0] = 001		112		
$V_{AGCSP02}$		ATP[2:0] = 010		110		
$V_{AGCSP03}$		ATP[2:0] = 011		108		
$V_{AGCSP04}$		ATP[2:0] = 100		106		
$V_{AGCSP05}$		ATP[2:0] = 101		104		
$V_{AGCSP06}$		ATP[2:0] = 110		102		

(1) When AISL=1, RF AGC function is not available at VHF-L band (output level is undefined).

Mixer, Oscillator, IF Amplifier (DIF OUT)

V_{CC} = 5 V, T_A = 25°C, measured in Figure 25 reference measurement circuit at 50-Ω system, IF = 44 MHz, IF filter characteristics: f_{peak} = 44 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
G_{C1D}	Conversion gain (mixer-IF amplifier), VHF-LOW	f_{in} = 57 MHz (1)	35	dB
G_{C3D}		f_{in} = 171 MHz (1)	35	
G_{C4D}	Conversion gain (mixer-IF amplifier), VHF-HIGH	f_{in} = 177 MHz (1)	35	dB
G_{C6D}		f_{in} = 467 MHz (1)	35	
G_{C7D}	Conversion gain (mixer-IF amplifier), UHF	f_{in} = 473 MHz (1)	35	dB
G_{C9D}		f_{in} = 864 MHz (1)	35	
NF_{1D}	Noise figure, VHF-LOW	f_{in} = 57 MHz	9	dB
NF_{3D}		f_{in} = 171 MHz	9	
NF_{4D}	Noise figure, VHF-HIGH	f_{in} = 177 MHz	9	dB
NF_{6D}		f_{in} = 467 MHz	10	
NF_{7D}	Noise figure, UHF	f_{in} = 473 MHz	10	dB
NF_{9D}		f_{in} = 864 MHz	12	
CM_{1D}	Input voltage causing 1% cross-modulation distortion, VHF-LOW	f_{in} = 57 MHz (2)	79	dBµV
CM_{3D}		f_{in} = 171 MHz (2)	79	
CM_{4D}	Input voltage causing 1% cross-modulation distortion, VHF-HIGH	f_{in} = 177 MHz (2)	79	dBµV
CM_{6D}		f_{in} = 467 MHz (2)	79	
CM_{7D}	Input voltage causing 1% cross-modulation distortion, UHF	f_{in} = 473 MHz (2)	77	dBµV
CM_{9D}		f_{in} = 864 MHz (2)	77	
V_{IFO1D}	IF output voltage, VHF-LOW	f_{in} = 57 MHz	117	dBµV
V_{IFO3D}		f_{in} = 171 MHz	117	
V_{IFO4D}	IF output voltage, VHF-HIGH	f_{in} = 177 MHz	117	dBµV
V_{IFO6D}		f_{in} = 467 MHz	117	
V_{IFO7D}	IF output voltage, UHF	f_{in} = 473 MHz	117	dBµV
V_{IFO9D}		f_{in} = 864 MHz	117	
Φ_{PLVL1D}	Phase noise, VHF-LOW	f_{in} = 57 MHz (3)	–90	dBc/Hz
Φ_{PLVL3D}		f_{in} = 171 MHz (4)	–85	
Φ_{PLVL4D}	Phase noise, VHF-HIGH	f_{in} = 177 MHz (3)	–85	dBc/Hz
Φ_{PLVL6D}		f_{in} = 467 MHz (4)	–77	
Φ_{PLVL7D}	Phase noise, UHF	f_{in} = 473 MHz (3)	–80	dBc/Hz
Φ_{PLVL9D}		f_{in} = 864 MHz (4)	–77	

(1) IF = 44 MHz, RF input level = 70 dBµV, differential output
(2) f_{undes} = f_{des} ±6 MHz, Pin = 70 dBµV, AM 1 kHz, 30%, DES/CM = S/I = 46 dB
(3) Offset = 1 kHz, CP current = 350 µA, reference divider = 64
(4) Offset = 1 kHz, CP current = 900 µA, reference divider = 64

Mixer, Oscillator, IF Amplifier (AIF OUT)

V_{CC} = 5 V, T_A = 25°C, measured in Figure 25 reference measurement circuit at 50-Ω system, IF = 45.75 MHz, IF filter characteristics: f_{peak} = 44 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
G_{C1A}	Conversion gain (mixer-IF amplifier), VHF-LOW	f_{in} = 55.25 MHz (1)	29	dB
G_{C3A}		f_{in} = 169.25 MHz (1)	29	
G_{C4A}	Conversion gain (mixer-IF amplifier), VHF-HIGH	f_{in} = 175.25 MHz (1)	29	dB
G_{C6A}		f_{in} = 465.25 MHz (1)	29	
G_{C7A}	Conversion gain (mixer-IF amplifier), UHF	f_{in} = 471.25 MHz (1)	29	dB
G_{C9A}		f_{in} = 862.25 MHz (1)	29	
NF_{1A}	Noise figure, VHF-LOW	f_{in} = 55.25 MHz	9	dB
NF_{3A}		f_{in} = 169.25 MHz	9	
NF_{4A}	Noise figure, VHF-HIGH	f_{in} = 175.25 MHz	9	dB
NF_{6A}		f_{in} = 465.25 MHz	10	
NF_{7A}	Noise figure, UHF	f_{in} = 471.25 MHz	10	dB
NF_{9A}		f_{in} = 862.25 MHz	12	
CM_{1A}	Input voltage causing 1% cross-modulation distortion, VHF-LOW	f_{in} = 55.25 MHz (2)	79	dBµV
CM_{3A}		f_{in} = 169.25 MHz (2)	79	
CM_{4A}	Input voltage causing 1% cross-modulation distortion, VHF-HIGH	f_{in} = 175.25 MHz (2)	79	dBµV
CM_{6A}		f_{in} = 465.25 MHz (2)	79	
CM_{7A}	Input voltage causing 1% cross-modulation distortion, UHF	f_{in} = 471.25 MHz (2)	79	dBµV
CM_{9A}		f_{in} = 862.25 MHz (2)	77	
V_{IFO1A}	IF output voltage, VHF-LOW	f_{in} = 55.25 MHz	117	dBµV
V_{IFO3A}		f_{in} = 169.25 MHz	117	
V_{IFO4A}	IF output voltage, VHF-HIGH	f_{in} = 175.25 MHz	117	dBµV
V_{IFO6A}		f_{in} = 465.25 MHz	117	
V_{IFO7A}	IF output voltage, UHF	f_{in} = 471.25 MHz	117	dBµV
V_{IFO9A}		f_{in} = 862.25 MHz	117	
Φ_{PLVL1A}	Phase noise, VHF-LOW	f_{in} = 55.25 MHz (3)	–95	dBc/Hz
Φ_{PLVL3A}		f_{in} = 169.25 MHz (3)	–95	
Φ_{PLVL4A}	Phase noise, VHF-HIGH	f_{in} = 175.25 MHz (3)	–90	dBc/Hz
Φ_{PLVL6A}		f_{in} = 465.25 MHz (3)	–90	
Φ_{PLVL7A}	Phase noise, UHF	f_{in} = 471.25 MHz (3)	–85	dBc/Hz
Φ_{PLVL9A}		f_{in} = 862.25 MHz (3)	–90	

(1) IF = 44 MHz, RF input level = 70 dBµV, differential output
(2) f_{undes} = f_{des} ±6 MHz, Pin = 70 dBµV, AM 1 kHz, 30%, DES/CM = S/I = 46 dB
(3) Offset = 10 kHz, CP current = 70 µA, reference divider = 128

IF Gain Controlled Amplifier

V_{CC} = 5 V, T_A = 25°C, measured in Figure 25 reference measurement circuit at 50-Ω system, IF = 44 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IFGCA}	Input current (IF GCA CTRL)	V_{IFGCA} = 3 V		30	60	µA
$V_{IFGCAMAX}$	Maximum gain control voltage	Gain maximum	3		V_{CC}	V
$V_{IFGCAMIN}$	Minimum gain control voltage	Gain minimum	0		0.2	V
$G_{IFGCAMAX}$	Maximum gain	V_{IFGCA} = 3 V		65		dB
$G_{IFGCAMIN}$	Minimum gain	V_{IFGCA} = 0 V		–1		dB
GCR_{IFGCA}	Gain control range	V_{IFGCA} = 0 V to 3 V		66		dB
$V_{IFGCAOUT}$	Output voltage	Single-ended output, V_{IFGCA} = 3 V		2.1		Vp-p
NF_{IFGCA}	Noise figure	V_{IFGCA} = 3 V		8.5		dB
$IM3_{IFGCA}$	Third order intermodulation distortion	$f_{IFGCAIN1}$ = 43 MHz, $f_{IFGCAIIN2}$ = 44 MHz, $V_{IFGCAOUT}$ = –2 dBm, V_{IFGCA} = 3 V		–50		dBc
IIP_{3IFGCA}	Input intercept point	V_{IFGCA} = 0 V		11		dBm
$R_{IFGCAIN}$	Input resistance (IF GCA IN1, IF GCA IN2)			1		kΩ
$R_{IFGCAOUT}$	Output resistance (IF GCA OUT1, IF GCA OUT2)			25		Ω

FUNCTIONAL DESCRIPTION

I²C Bus Mode

I²C Write Mode (R/$\overline{W}$ = 0)

Table 1. Write Data Format

	MSB							LSB	
Address byte (ADB)	1	1	0	0	0	MA1	MA0	R/$\overline{W}$ = 0	A(1)
Divider byte 1 (DB1)	0	N14	N13	N12	N11	N10	N9	N8	A(1)
Divider byte 2 (DB2)	N7	N6	N5	N4	N3	N2	N1	N0	A(1)
Control byte 1 (CB1)	1	0	ATP2	ATP1	ATP0	RS2	RS1	RS0	A(1)
Band switch byte (BB)	CP1	CP0	AISL	P5	BS4	BS3	BS2	BS1	A(1)
Control byte 2 (CB2)	1	1	ATC	MODE	T3/DISGCA	T2/IFDA	T1/CP2	T0/XLO	A(1)

(1) A : acknowledge

Table 2. Write Data Symbol Description

SYMBOL	DESCRIPTION	DEFAULT
MA[1:0]	Address-set bits (see Table 3)	
N[14:0]	Programmable counter set bits $N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2 + N0$	N14 = N13 = N12 = ... = N0 = 0
ATP[2:0]	RF AGC start-point control bits (see Table 4)	ATP[2:0] = 000
RS[2:0]	Reference divider ratio-selection bits (see Table 5)	RS[2:0] = 000
CP[1:0]	Charge-pump current-set bit (see Table 6)	CP[1:0] = 00
AISL	RF AGC detector input selection bit AISL = 0: IF amplifier AISL = 1: Mixer output	AISL = 0
P5	Port output/ADC input control bit P5 = 0: ADC INPUT P5 = 1: Tr = ON	P5 = 0
BS[4:1]	Band switch control bits BSn = 0: Tr = OFF BSn = 1: Tr = ON	BSn = 0
	Band selection by BS[1:2] **BS1 BS2** 1 0 VHF-LO 0 1 VHF-HI 0 0 UHF 1 1 Standby mode/stop MOP function (XTALOUT is available in standby mode)	
ATC	RF AGC current-set bit ATC = 0: Current = 300 nA ATC = 1: Current = 9 μA	ATC = 0
Mode T3/DISGCA T2/IFDA T1/CP2 T0/XLO	Mode = 0 : IFGCA enabled, DIFOUT1, 2 selected T3/DISGCA, T2/IFDA, T1/CP2, T0/XLO are Test bits and XTALOUT control bit (see Table 7)	MODE = 0 T[3:0] = 0000
	Mode = 1 T3/DISGCA = 0 : IF GCA enabled T3/DISGCA = 1 : IF GCA disabled T2/IFDA = 0 : DIFOUT1, 2 selected T2/IFDA = 1 : AIFOUT selected T1/CP2 : Icp control bit, See Table 6 T0/XLO = 0 : XTALOUT enabled T0/XLO = 1 : XTALOUT disabled	

Table 3. Address Selection

MA1	MA0	VOLTAGE APPLIED ON AS INPUT
0	0	0 V to 0.1 V_{CC} (Low)
0	1	OPEN, or 0.2 V_{CC} to 0.3 V_{CC} (Mid2)
1	0	0.4 V_{CC} to 0.6 V_{CC} (Mid1)
1	1	0.9 V_{CC} to V_{CC} (High)

Table 4. RF AGC Start Point(1)

ATP2	ATP1	ATP0	IFOUT LEVEL (dBµV)
0	0	0	114
0	0	1	112
0	1	0	110
0	1	1	108
1	0	0	106
1	0	1	104
1	1	0	102
1	1	1	Disabled

(1) When AISL=1, RF AGC function is not available at VHF-L band (output level is undefined).

Table 5. Reference Divider Ratio

RS2	RS1	RS0	REFERENCE DIVIDER RATIO
0	0	0	24
0	0	1	28
0	1	0	32
0	1	1	64
1	0	0	128
1	X	1	80

Table 6. Charge-Pump Current

MODE	CP2	CP1	CP0	CHARGE PUMP CURRENT (µA)
X	0	0	0	70
X	0	0	1	140
X	0	1	0	350
X	0	1	1	600
1	1	0	0	900

Table 7. Test Bits/XTALOUT Control [(1)]

MODE	T3/DISGCA	T2/IFDA	T1/CP2	T0/XLO	DEVICE OPERATION	XTALOUT 4-MHz OUTPUT
0	0	0	0	0	Normal operation	Enabled
0	0	0	0	1	Normal operation	Disabled
1	X	X	X	0	Normal operation	Enabled
1	X	X	X	1	Normal operation	Disabled
0	X	1	X	X	Test mode	Not available
0	1	X	X	X	Test mode	Not available

(1) RFAGC and XTALOUT are not available in test mode.

Example I²C Data Write Sequences

Telegram examples:

Start-ADB-DB1-DB2-CB1-BB-CB2-Stop
Start-ADB-DB1-DB2-Stop
Start-ADB-CB1-BB-CB2-Stop
Start-ADB-CB1-BB-Stop
Start-ADB-CB2-Stop

Abbreviations:

ADB: Address byte
BB: Band switch byte
CB1: Control byte 1
CB2: Control byte 2
DB1: Divider byte 1
DB2: Divider byte 2
Start: Start condition
Stop: Stop condition

I²C Read Mode (R/$\overline{W}$ = 1)

Table 8. Read Data Format

	MSB							LSB	
Address byte (ADB)	1	1	0	0	0	MA1	MA0	R/$\overline{W}$ = 1	A [(1)]
Status byte (SB)	POR	FL	1	1	X	A2	A1	A0	–

(1) A : acknowledge

Table 9. Read Data Symbol Description

SYMBOL	DESCRIPTION	DEFAULT
MA[1:0]	Address set bits (see Table 3)	
POR	Power-on-reset flag POR set: power on POR reset: end-of-data transmission procedure	POR = 1
FL	In-lock flag PLL locked (FL = 1), unlocked (FL = 0)	
A[2:0]	Digital data of ADC (see Table 10) Bit P5 must be set to 0.	

Table 10. ADC Level(1)

A2	A1	A0	VOLTAGE APPLIED ON ADC INPUT
1	0	0	0.6 V_{CC} to V_{CC}
0	1	1	0.45 V_{CC} to 0.6 V_{CC}
0	1	0	0.3 V_{CC} to 0.45 V_{CC}
0	0	1	0.15 V_{CC} to 0.3 V_{CC}
0	0	0	0 V to 0.15 V_{CC}

(1) Accuracy is 0.03 × V_{CC}.

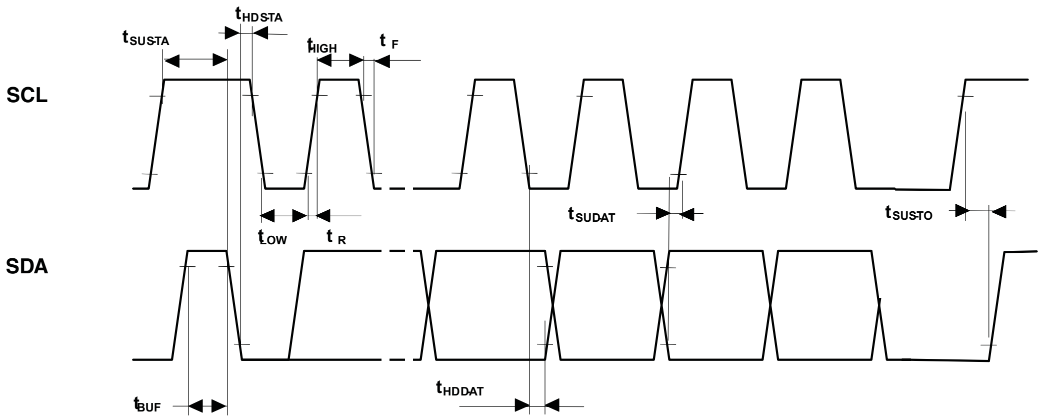
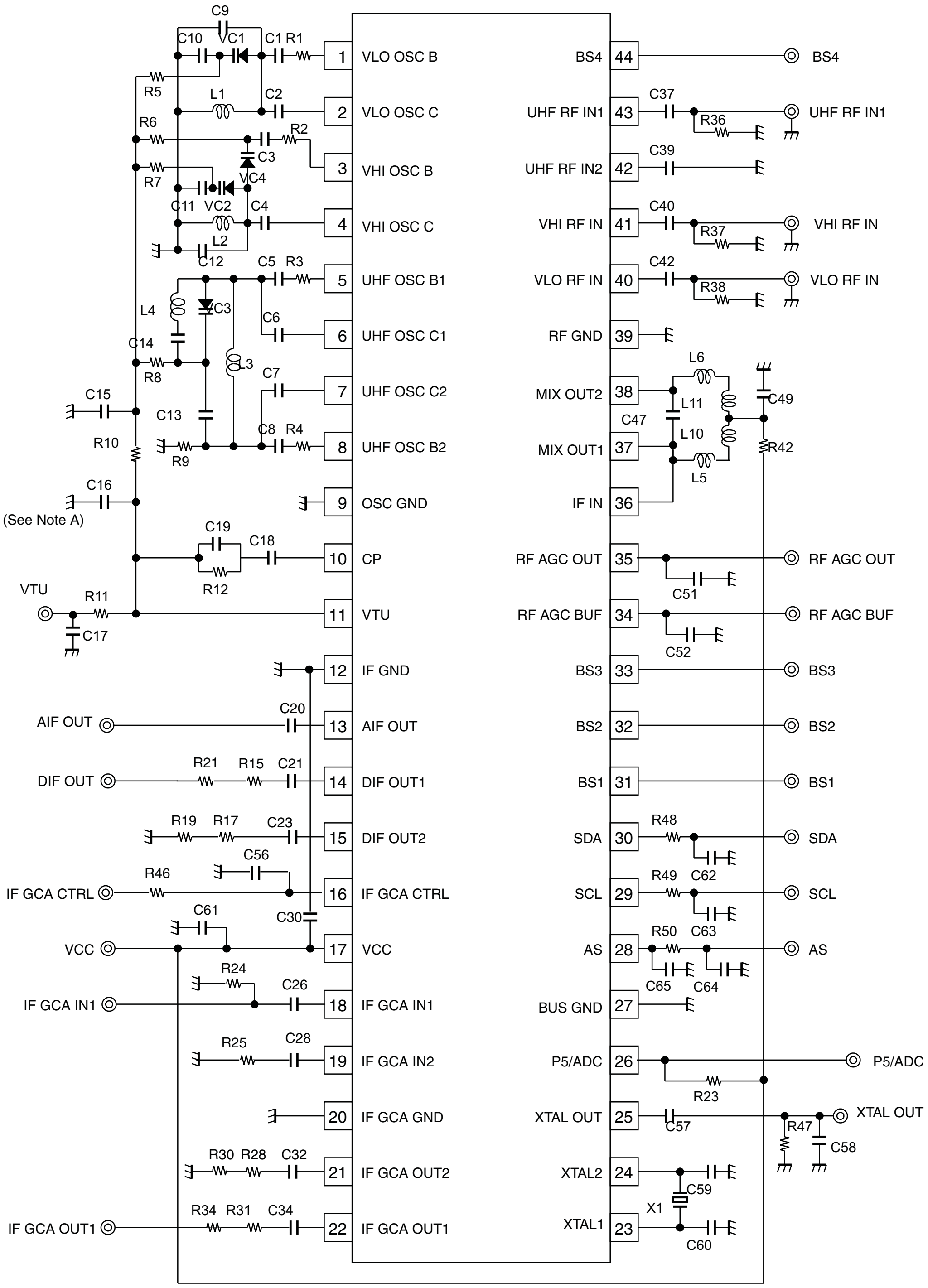


Figure 24. I²C Timing Chart

APPLICATION INFORMATION



A. To prevent abnormal oscillation, connect C16, which does not affect a PLL.

B. This application information is advisory and performance-check is required at actual application circuits. TI assumes no responsibility for the consequences of use of this circuit, such as an infringement of intellectual property rights or other rights, including patents, of third parties.

Figure 25. Reference Measurement Circuit

Component Values for Measurement Circuit

PARTS NAME	VALUE	PARTS NAME	VALUE
C1 (VLO OSC B)	1 pF	L1 (VLO OSC)	3.0 mm, 7T, wire 0.32 mm
C2 (VLO OSC C)	2 pF	L2 (VHI OSC)	2.0 mm, 3T, wire 0.4 mm
C3 (VHI OSC B)	7 pF	L3 (UHF OSC)	1.8 mm, 3T, wire 0.4 mm
C4 (VHI OSC C)	5 pF	L4 (UHF OSC)	1.8 mm, 3T, wire 0.4 mm
C5 (UHF OSCB1)	1.5 pF	L5 (MIX OUT)	680 nH (LK1608R68K-T)
C6 (UHF OSCC1)	1 pF	L6 (MIX OUT)	680 nH (LK1608R68K-T)
C7 (UHF OSCC2)	1 pF	L10 (MIX OUT)	Short
C8 (UHF OSCB2)	1.5 pF	L11 (MIX OUT)	Short
C9 (VLO OSC)	OPEN	R1(VLO OSC B)	0
C10(VLO OSC)	43 pF	R2 (VHI OSC B)	4.7 Ω
C11 (VHI OSC)	51 pF	R3 (UHF OSC B1)	4.7 Ω
C12 (VHI OSC)	0.5 pF	R4 (UHF OSC B2)	0
C13 (UHF OSC)	10 pF	R5 (VLO OSC)	3.3 kΩ
C14 (UHF OSC)	100 pF	R6 (VHI OSC)	3.3 kΩ
C15 (VTU)	2.2 nF/50 V	R7 (VHI OSC)	3.3 kΩ
C16 (CP)	150 pF/50 V	R8 (UHF OSC)	1 kΩ
C17 (VTU)	2.2 nF/50 V	R9 (UHF OSC)	2.2 k
C18(CP)	0.01 u/50 V	R10 (VTU)	3 kΩ
C19(CP)	22 pF/50 V	R11 (VTU)	20 kΩ
C20 (AIF OUT)	2.2 nF	R12 (CP)	47 kΩ
C21 (DIF OUT1)	2.2 nF	R15 (DIF OUT1)	200 Ω
C23 (DIF OUT2)	2.2 nF	R17 (DIF OUT2)	200 Ω
C26 (IF GCA IN1)	2.2 nF	R19 (DIF OUT2)	50 Ω
C28 (IF GCA IN2)	2.2 nF	R21 (DIF OUT1)	0
C30 (VCC)	0.1 uF	R23 (P5/ADC)	Open
C32 (IF GCA OUT1)	2.2 nF	R24 (IF GCA IN1)	(50 Ω)
C34 (IF GCA OUT2)	2.2 nF	R25 (IF GCA IN2)	0
C37 (UHF RF IN1)	2.2 nF	R28 (IF GCA OUT1)	200 Ω
C39 (UHF RFIN2)	2.2 nF	R30 (IF GCA OUT1)	50 Ω
C40 (VHI RF IN)	2.2 nF	R31 (IF GCA OUT2)	200 Ω
C42 (VLO RF IN)	2.2 nF	R34 (IF GCA OUT2)	0
C47 (MIX OUT)	6 pF	R36 (UHF RF IN1)	(50 Ω)
C49 (MIX OUT)	2.2 nF	R37 (VHI RF IN)	(50 Ω)
C51 (RF AGC OUT)	0.15 uF	R38 (VLO RF IN)	(50 Ω)
C52 (RF AGC BUF)	Open	R42 (MIX OUT)	0
C56 (IFGCA CTRL)	0.1 μF	R46 (IFGCA CTRL)	0
C57 (XTAL OUT)	0.01 uF	R47 (XTAL OUT)	5.1 kΩ
C58 (XTAL OUT)	10 pF	R48 (SDA)	330 Ω
C59(XTAL)	27 pF	R49 (SCL)	330 Ω
C60 (XTAL)	27 pF	R50 (AS)	Open
C61 (VCC)	2.2 nF	VC1 (VLO OSC)	MA2S374
C62 (SDA)	Open	VC2 (VHI OSC)	MA2S374
C63 (SCL)	Open	VC3 (UHF OSC)	MA2S372
C64 (AS)	Open	VC4 (VHI OSC)	MA2S372
C65 (AS)	22 pF	X1	4-MHz crystal

APPLICATION INFORMATION (CONTINUED)

Test Circuits

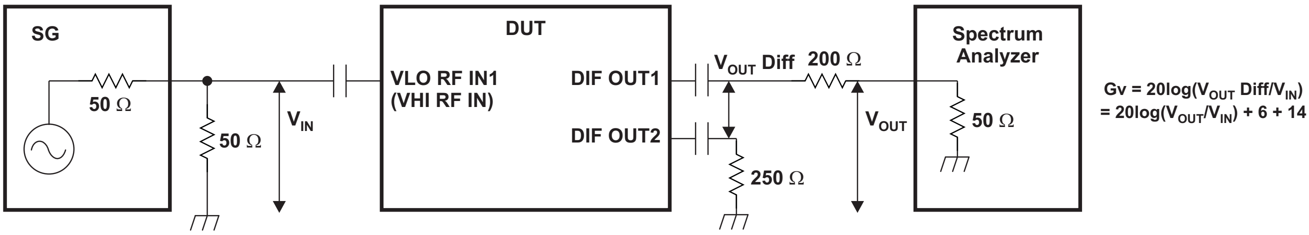


Figure 26. VHF-Conversion Gain-Measurement Circuit (at DIFOUT)

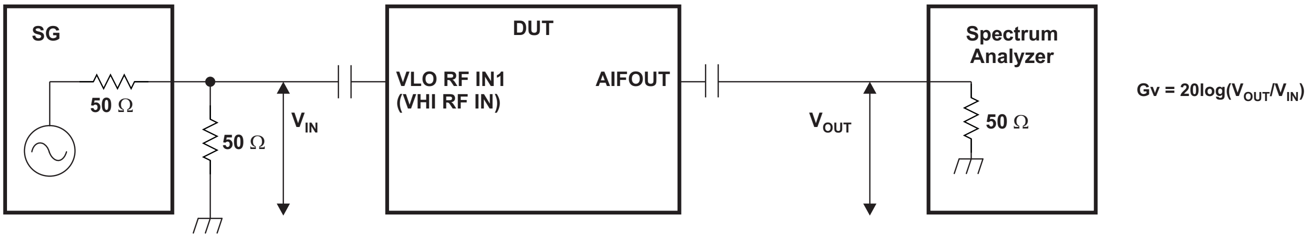


Figure 27. VHF-Conversion Gain Measurement Circuit (at AIFOUT)

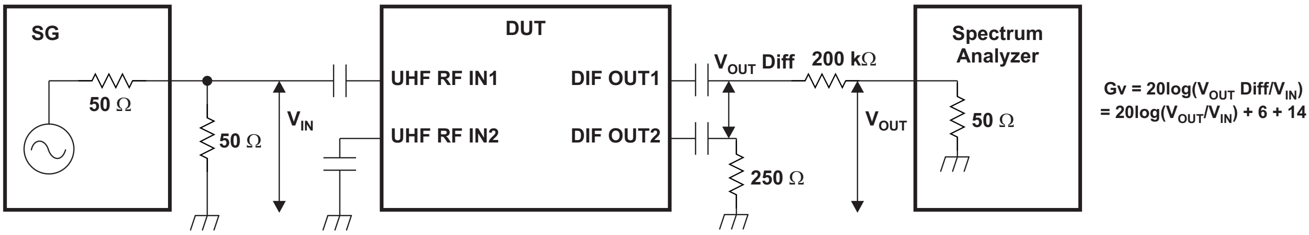


Figure 28. UHF-Conversion Gain-Measurement Circuit (at DIFOUT)

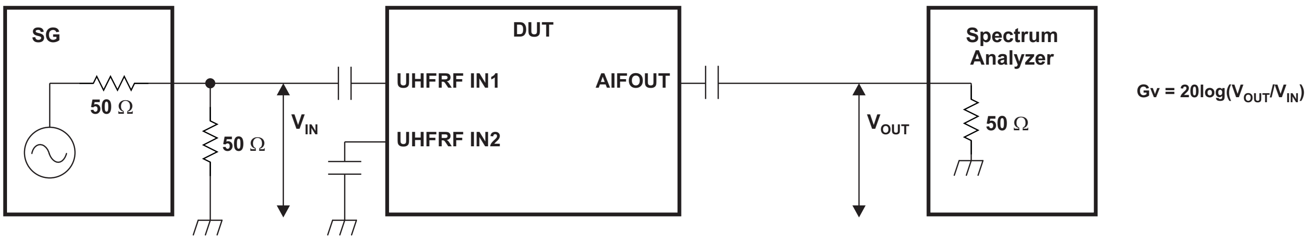


Figure 29. UHF-Conversion Gain Measurement Circuit (at AIFOUT)

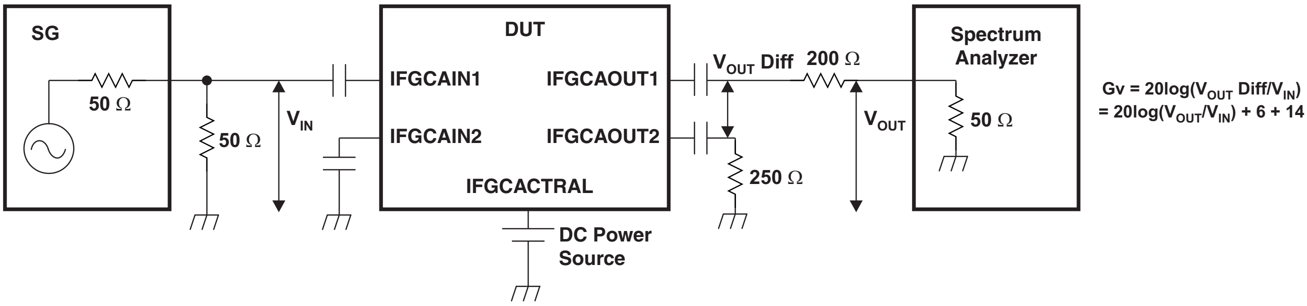


Figure 30. IF GCA Gain Measurement Circuit

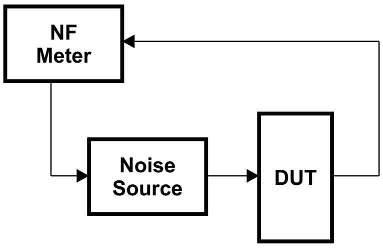


Figure 31. Noise-Figure Measurement Circuit

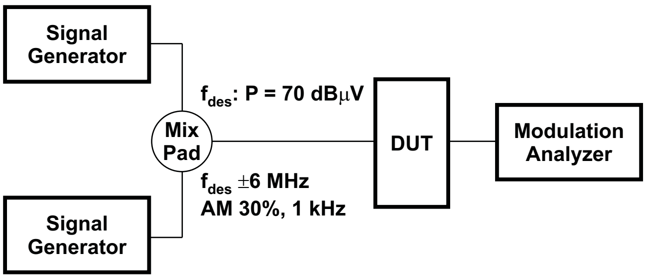


Figure 32. 1% Cross-Modulation Distortion Measurement Circuit

TYPICAL CHARACTERISTICS

Band Switch Driver Output Voltage (BS1–BS4)

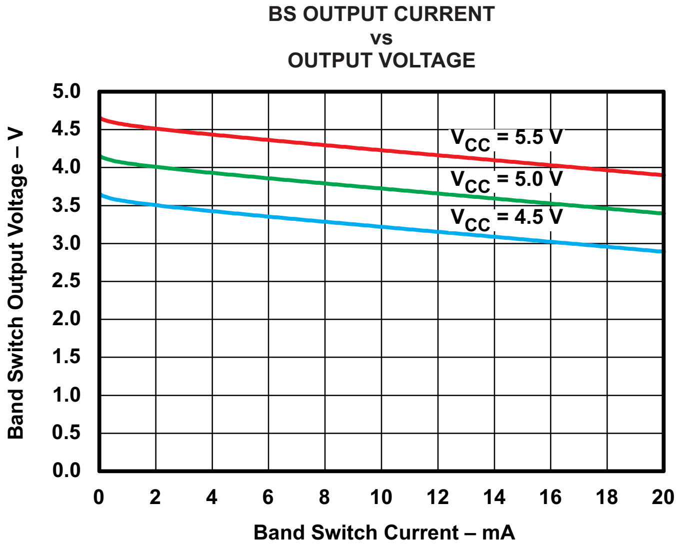


Figure 33. Band Switch Driver Output Voltage

S-Parameter

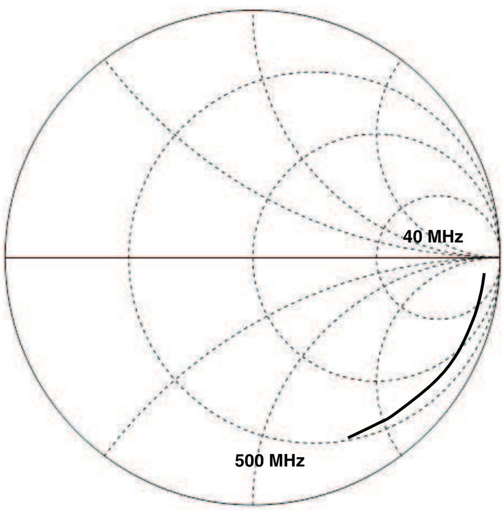


Figure 34. VLO RFIN, VHI RFIN

TYPICAL CHARACTERISTICS (continued)

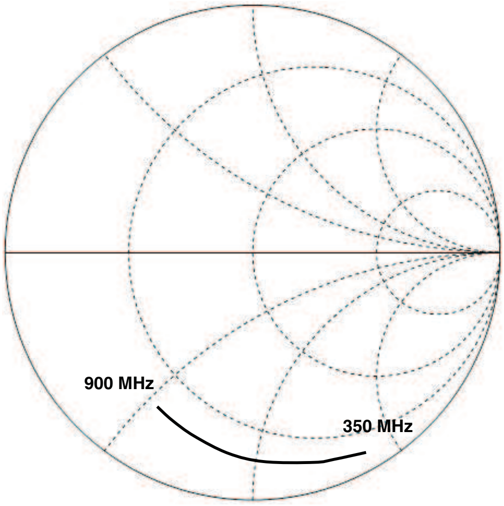


Figure 35. UHF RFIN

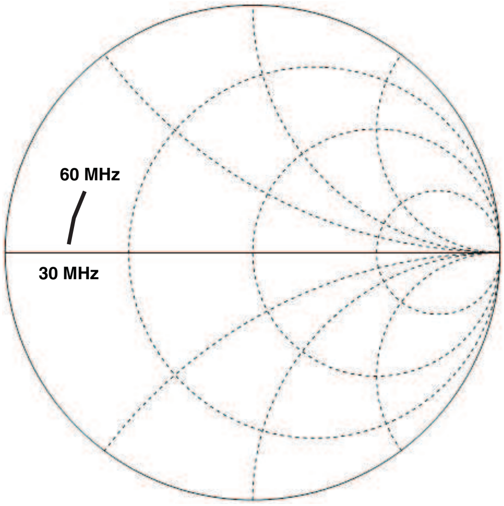


Figure 36. DIFOUT

TYPICAL CHARACTERISTICS (continued)

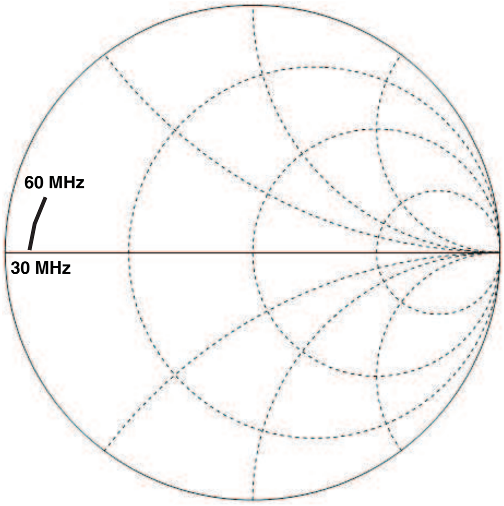


Figure 37. AIFOUT

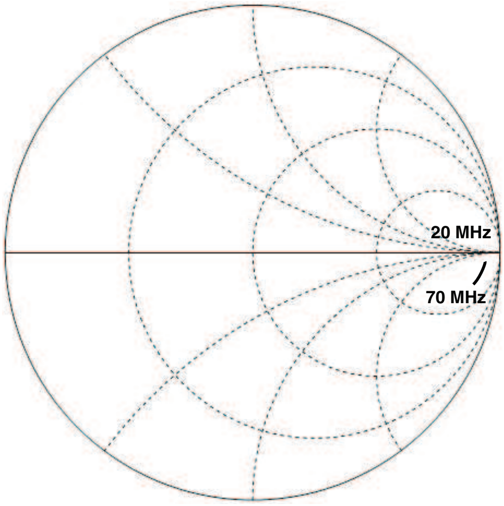


Figure 38. IF GCA IN

TYPICAL CHARACTERISTICS (continued)

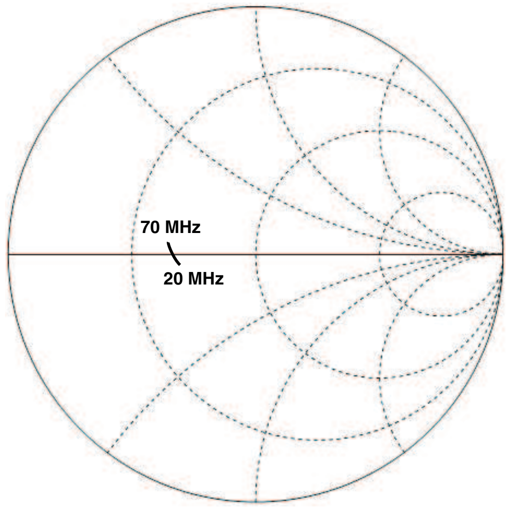


Figure 39. IF GCAOUT

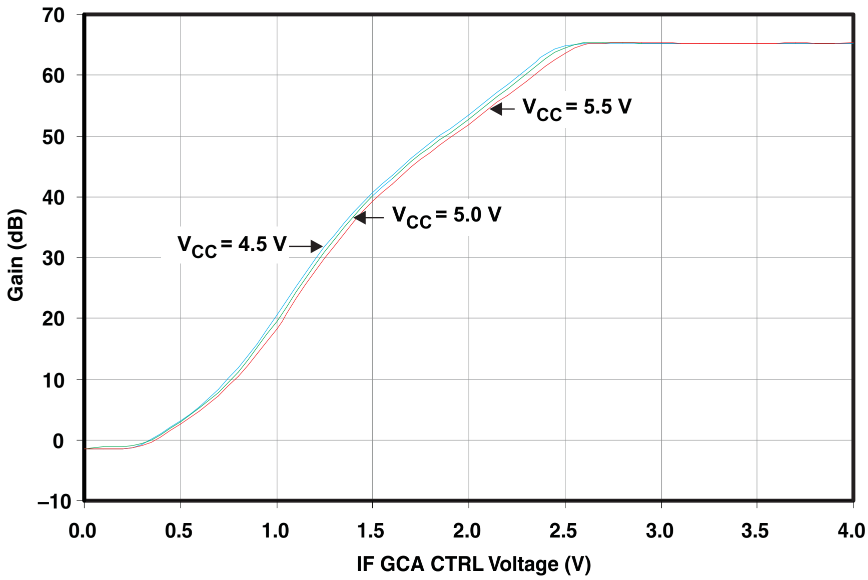


Figure 40. IF GCA Gain vs Control Voltage 1

TYPICAL CHARACTERISTICS (continued)

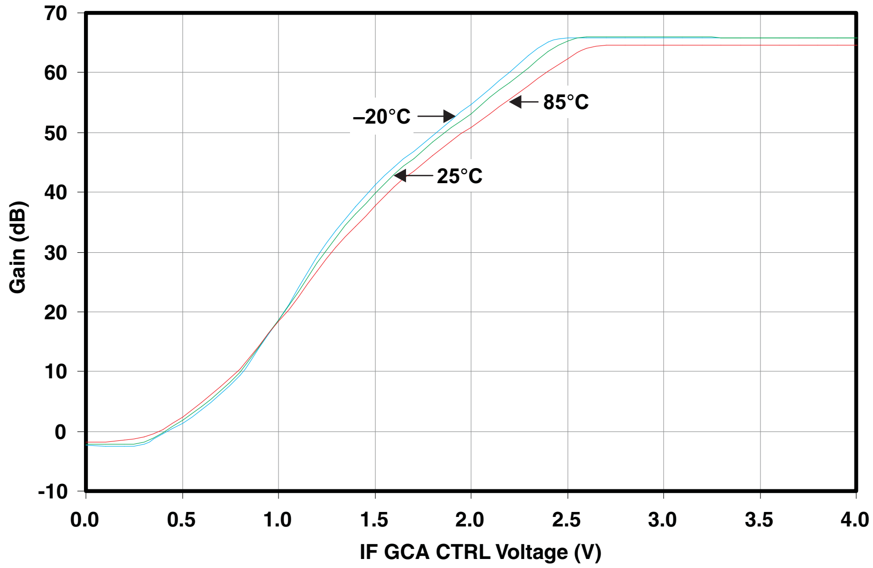


Figure 41. IF GCA Gain vs Control Voltage 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN761640DBTR	OBSOLETE	TSSOP	DBT	44		TBD	Call TI	Call TI	-20 to 85	SN761640	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

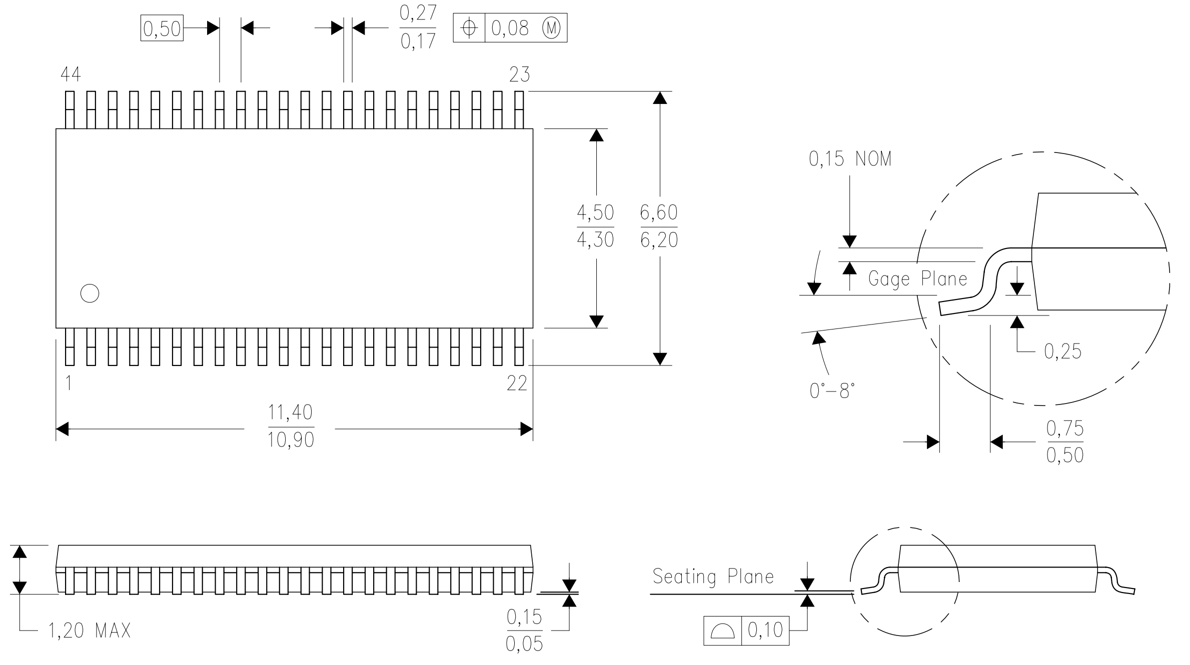
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

DBT (R–PDSO–G44) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

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