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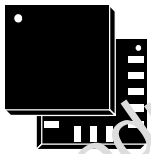
LY530AL

MEMS inertial sensor
single-axis analog and digital output yaw rate gyroscope

Preliminary Data

Features

- 2.7 V to 3.6 V single supply operation
- Low power consumption
- Embedded power-down
- ±300°/sec full scale
- Absolute analog rate output
- I^2C/SPI digital output interface
- Integrated low-pass filters
- Additional high pass filter for digital output
- Embedded self-test
- High shock survivability
- ECOPACK® RoHS and “Green” compliant (see *Section 7*)



LGA 16 (5x5x1.5mm)

Description

The LY530AL is a low-power single axis yaw rate sensor. It includes a sensing element and an IC interface able to provide the measured angular rate to the external world through an analog output voltage and I^2C/SPI digital interface.

The sensing element, capable of detecting the yaw rate, is manufactured using a dedicated micromachining process developed by ST to produce inertial sensors and actuators on silicon wafers.

The IC interface is manufactured using a CMOS process that allows a high level of integration to design a dedicated circuit which is trimmed to better match the sensing element characteristics.

The output of LY530AL has a full scale of ±300 °/s and is capable of measuring rates with a -3 dB bandwidth up to 88 Hz.

The LY530AL is available in a plastic land grid array (LGA) package and can operate within a temperature range from -40 °C to +85 °C.

The LY530AL belongs to a family of products suitable for a variety of applications, including:

- Gaming and virtual reality input devices
- Motion control with MMI (man-machine interface)
- Image stabilization for digital video and digital still cameras
- GPS navigation systems
- Appliances and robotics

Table 1. Device summary

Order code	Temperature range (°C)	Package	Packing
LY530AL	-40 to +85	LGA-16 (5x5x1.5)	Tray
LY530ALTR	-40 to +85	LGA-16 (5x5x1.5)	Tape and reel

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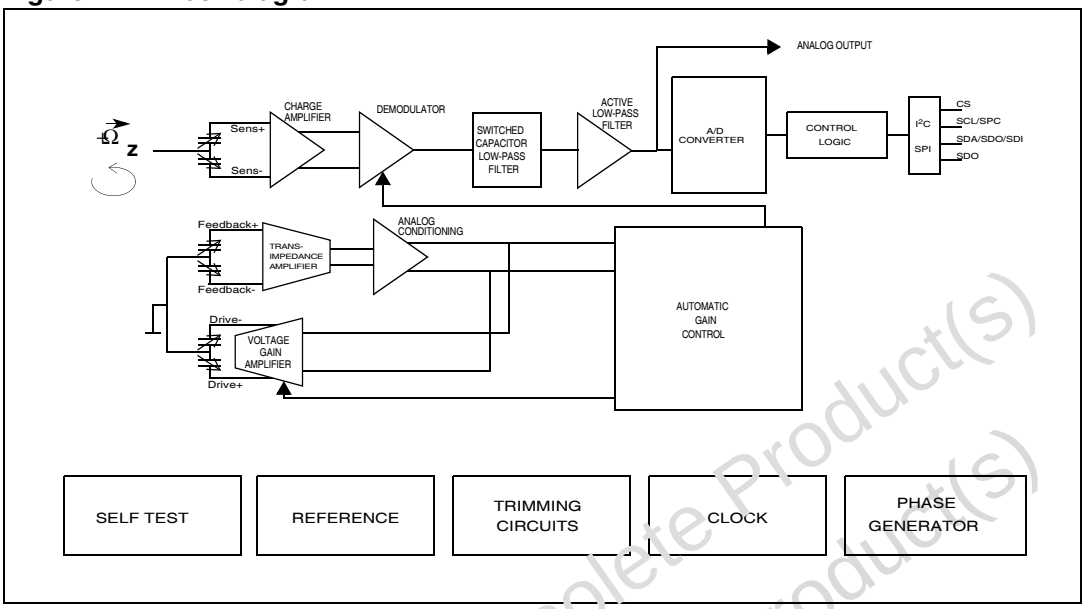
1 Block diagram and pin description

Figure 1. Block diagram



1.1 Pin description

Figure 2. Pin connection

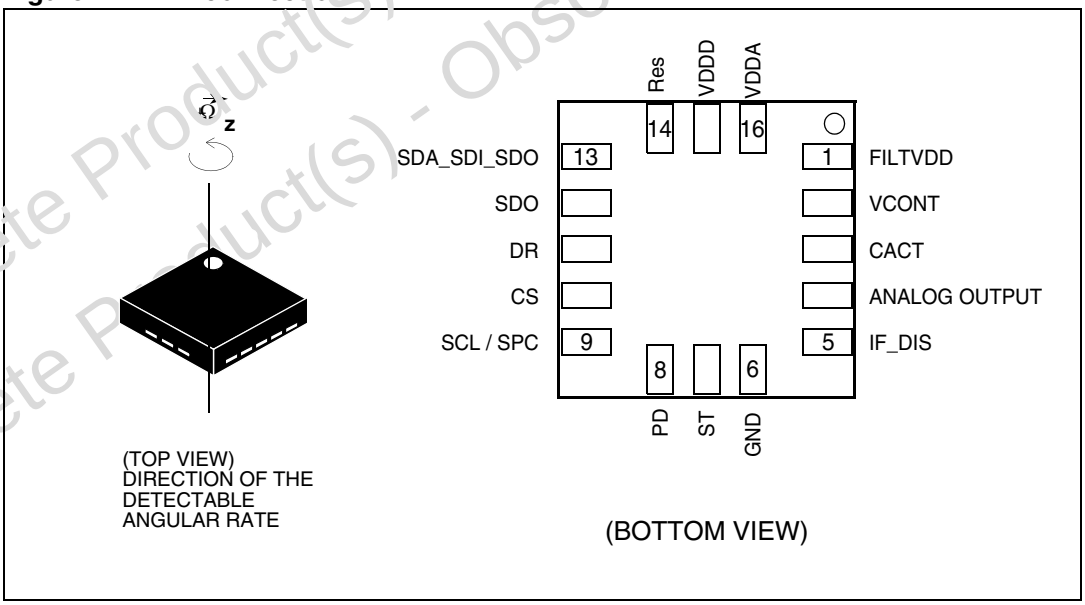


Table 2. Pin description

Pin #	Pin Name	Analog function	Digital function
1	FILTVDD	PLL filter connection pin #2	PLL filter connection pin #2
2	VCONT	PLL filter connection pin #1	PLL filter connection pin #1
3	CACT	Active filter capacitor	Active filter capacitor
4	ANALOG OUTPUT	Rate signal output voltage	Leave unconnected
5	IF_DIS	Leave unconnected	Digital Interface Selection (See *Table 19*)
6	GND	0V supply voltage	0V supply voltage
7	ST	Self-test (logic 0: normal mode; logic 1: self-test)	Leave unconnected
8	PD	Power-down (logic 0: normal mode; logic 1: power-down mode)	Connect to Vdd
9	SCL SPC	Leave unconnected	I^2C Serial Clock (SCL) SPI Serial Port Clock (SPC)
10	CS	Leave unconnected	SPI enable I^2C/SPI mode selection (1: I^2C mode; 0: SPI mode)
11	DR	Leave unconnected	DataReady
12	SDO	Leave unconnected or connect to Vdd	SPI Serial data output (4-wire mode only) I^2C less significant bit of the device address
13	SDA_SDI_SDO	Leave unconnected or connect to Vdd	I^2C Serial Data (SDA) SPI Serial Data Input (SDI) 3-wire Interface Serial Data Output
14	Res	Connect to Vdd	Connect to Vdd
15	VDDD	Digital side Vdd supply	Digital side Vdd supply
16	VDDA	Analog side Vdd supply	Analog side Vdd supply

2 Mechanical and electrical specifications

2.1 Mechanical characteristics (analog output)

Table 3. Mechanical characteristics @ Vdd = 3.3 V, T = 25 °C unless otherwise noted(1)

Symbol	Parameter	Test condition	Min.	Typ.(2)	Max.	Unit
FS	Measurement range			±300		°/s
So	Sensitivity			3.3		mV/ °/s
SoDr	Sensitivity change vs. temperature	From -40 °C to +85 °C		4		%
Voff	Zero-rate level(3)			1.65		V
OffDr	Zero-rate level change vs. temperature	From -40 °C to +85 °C		5		°/s
NL	Non linearity(4)	Best fit straight line		±0.8		% FS
BW	-3dB bandwidth(5)(6)	C_{ACT} = 10 nF		23		Hz
Rn	Rate noise density			0.1		$°/s / \sqrt{Hz}$
Vt	Self-test output voltage change(7)			+300		mV
Sup	Start-up time	Settling to ±5 °/s		300		ms
Fres	Sensing element resonant frequency			4.5		kHz
Top	Operating temperature range		-40		+85	°C
Wh	Product weight			160		mg

1. The product is factory calibrated at 3.3 V. The operational power supply range is specified in *Table 5*.
2. Typical specifications are not guaranteed
3. Zero rate level is absolute with respect to power supply
4. Specified by design
5. The product is capable of sensing angular rates extending from DC to the selected bandwidth
6. User selectable by external capacitor C_{ACT}
7. "Self-test output voltage change" is defined as $Vout_{(Vst = logic\ 1)}$ - $Vout_{(Vst = logic\ 0)}$

2.2 Mechanical characteristics (digital output)

Table 4. Mechanical characteristics @ Vdd = 3.3 V, T = 25 °C unless otherwise noted(1)

Symbol	Parameter	Test condition	Min.	Typ.(2)	Max.	Unit
So	Sensitivity			1.55		LSb/ °/s
Voff	Zero-rate level(3)			0		LSb
ODR	Output data rate			1		kHz

Table 4. Mechanical characteristics @ Vdd = 3.3 V, T = 25 °C unless otherwise noted(1)

Symbol	Parameter	Test condition	Min.	Typ.(2)	Max.	Unit
Vt	Self-test output change(4)			230		LSb
Fres	Sensing element resonant frequency			4.5		kHz
Top	Operating temperature range		-40		+85	°C
Wh	Product weight			160		mg

1. The product is factory calibrated at 3.3 V. The operational power supply range is specified in *Table 5*.
2. Typical specifications are not guaranteed
3. The product is capable of sensing angular rates extending from DC to the selected bandwidth
4. "Self test output change" is defined as $OUTPUT[LSb]_{(Self\text{-}test\ bit\ on\ OUTPUT\_SEL\_REG=1)}$ $OUTPUT[LSb]_{(Self\text{-}test\ bit\ on\ OUTPUT\_SEL\_REG=0)}$.

2.3 Electrical characteristics

Table 5. Electrical characteristics @ Vdd =3.3 V, T=25 °C unless otherwise noted(1)

Symbol	Parameter	Test condition	Min.	Typ.(2)	Max.	Unit
Vdd	Supply voltage		2.7	3.3	3.6	V
Idd_A	Supply current (analog)	PD pin connected to GND		4.8		mA
Idd_D	Supply current (digital)			5.5		mA
IddPdn	Supply current in power-down mode	PD pin connected to Vdd		1		µA
V_{ST}	Self-test input (Analog use)	Logic 0 level	0		0.2*Vdd	V
		Logic 1 level	0.8*Vdd		Vdd	
V_{PD}	Power-down input (Analog use)	Logic 0 level	0		0.2*Vdd	V
		Logic 1 level	0.8*Vdd		Vdd	
C_{ACT}	Active low-pass filter capacitor		10			nF
OVS	Output voltage swing(3)	Iout = ±100µA	0.4		V_{dd}-0.4	V
C_{LOAD}	Capacitive load drive(3)		0.4		10	nF
Top	Operating temperature range		-40		+85	°C

1. The product is factory calibrated at 3.3 V
2. Typical specifications are not guaranteed
3. Referred to ANALOG OUTPUT pin #6

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

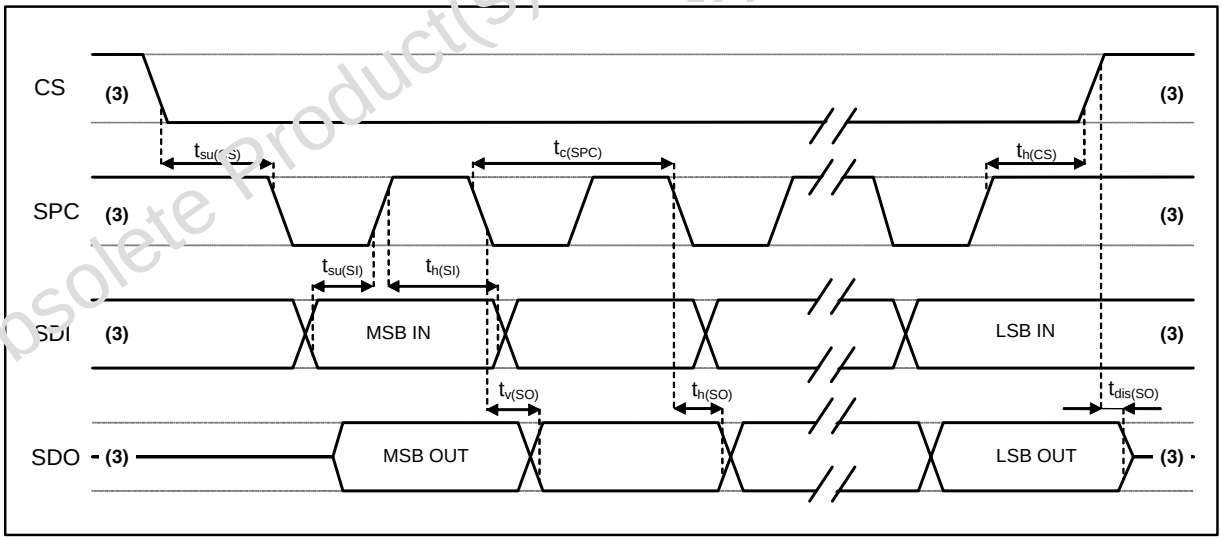
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min	Max	
tc(SPC)	SPI clock cycle	100		ns
fc(SPC)	SPI clock frequency		10	MHz
tsu(CS)	CS setup time	5		ns
th(CS)	CS hold time	8		
tsu(SI)	SDI input setup time	5		
th(SI)	SDI input hold time	15		
tv(SO)	SDO valid output time		50	
th(SO)	SDO output hold time	6		
tdis(SO)	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production

Figure 3. SPI slave timing diagram (2)



2. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both Input and Output port
3. When no communication is on-going, data on CS, SPC, SDI and SDO are driven by internal pull-up resistors

2.4.2 I²C - Inter IC control interface

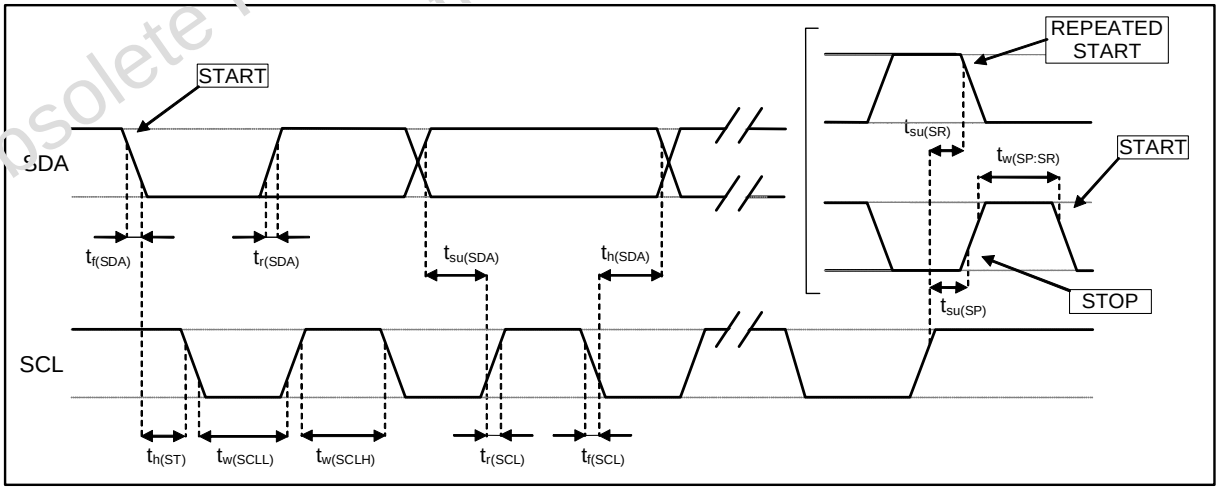
Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values

Symbol	Parameter	I²C Standard mode(1)		I²C Fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	KHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(2)	3.45	0(2)	0.9	µs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	20 + 0.1C_b (3)	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	20 + 0.1C_b (3)	300	
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production
2. A device must internally provide an hold time of at least 300ns for the SDA signal (referred to VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL
3. Cb = total capacitance of one bus line, in pF

Figure 4. I²C slave timing diagram (4)



4. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports

2.5 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 6	V
Vin	Input voltage on any control pin (PD, ST)	-0.3 to Vdd +0.3	V
A_{UNP}	Acceleration (not powered)	3000 g for 0.5 ms	
		10000 g for 0.1 ms	
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part

This is an ESD sensitive device, improper handling can cause permanent damage to the part

2.6 Terminology

2.6.1 Sensitivity

A yaw rate gyroscope is a Z-axis rate device that produces a positive-going output value for counterclockwise rotation around the axis normal to the package top. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and also very little over time.

2.6.2 Zero-rate level

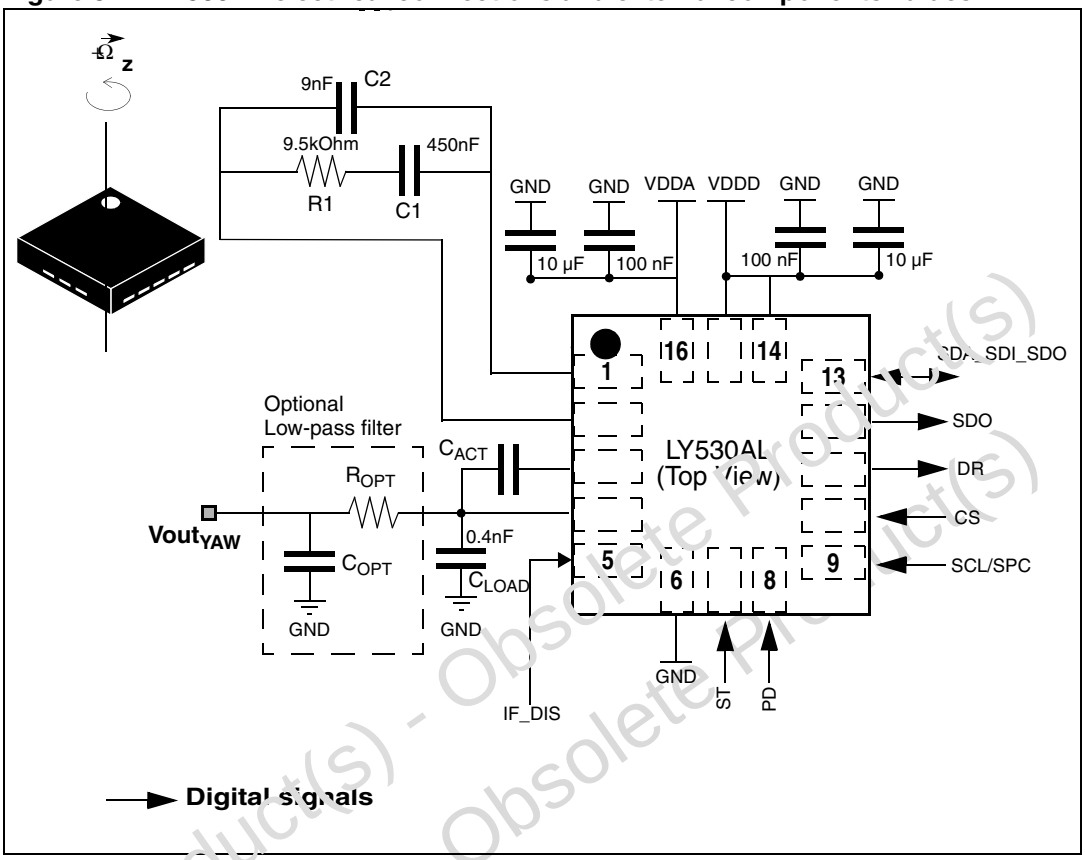
Zero-rate level describes the actual output value if there is no angular rate present.Zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and also very little over time.

2.6.3 Self-test

Self-test allows to test the mechanical and electric part of the sensor, allowing the seismic mass to be moved by means of an electrostatic test-force. If the device is used as analog component the Self-test function is off when the ST pin is connected to GND. When the ST pin is tied to Vdd, an actuation force is applied to the sensor, emulating a definite Coriolis force. In this case the sensor output will exhibit a voltage change in its DC level which is also depending on the supply voltage.
For the digital use of the device, the self test function is enabled acting on ST_bit inside OUTPUT_SEL_REG(23h).
When ST is active, the device output level is given by the algebraic sum of the signals produced by the velocity acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified in *Table 3*, then the mechanical element is working properly and the parameters of the interface chip are within the defined specification.

3 Application hints

Figure 5. LY530AL electrical connections and external components values



Power supply decoupling capacitors (100 nF ceramic or polyester + 10 µF Aluminum) should be placed as near as possible to the device (common design practice). VDDA(pin 16) and VDDD(pin 15) lines have been kept separated to avoid switching noise coupling on the analog side.

The LY530AL allows to band limit the output rate response through the use of two first-order on-chip filters: a switched capacitor low-pass filter, with 400Hz -3dB bandwidth, in combination with an active low-pass filter. The active filter -3 dB nominal frequency (f_{tA}) is set through an internal resistor R_{ACT} and the external capacitor C_{ACT} (added between **CACT** pin #3 and **ANALOG OUTPUT** pin #4), by the formula:

$$f_{tA} = \frac{1}{2\pi \cdot R_{ACT} \cdot C_{ACT}}$$

The value of the internal resistor R_{ACT} is 180 kΩ, while the external capacitor C_{ACT} is used to select the signal bandwidth. The sensed frequency range spans from DC up to the selected bandwidth.

In order to further reduce high-frequency noise, the LY530AL supports an additional optional low-pass filter on **ANALOG OUTPUT** pin #4 (*Figure 5*). The cutoff frequency (f_{tP}) is given by the formula:

$$f_{tP} = \frac{1}{2\pi \cdot R_{OPT} \cdot C_{OPT}}$$

The LY530AL IC includes a PLL (phase locked loop) circuit to synchronize driving and sensing interfaces. Capacitors and resistors must be added at the **FILTVDD** and **VCONT** pins (as shown in *Figure 5*) to implement a second-order low-pass filter. *Table 9* summarizes the PLL low-pass filter components' values.

Table 9. PLL low-pass filter components' values

Component	Value
C1	450 nF ± 10%
C2	9 nF ± 10%
R1	9.5 kΩ ± 10%

3.1 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and "Green" standard. It is qualified for soldering heat resistance according to JEDEC J-STD-020C.

Leave "Pin 1 Indicator" unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com/mems.

4 Digital interfaces

The registers embedded inside the LY530AL may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pins. To select/exploit the I^2C interface, CS line must be tied high (i.e connected to Vdd_IO).

Table 10. Serial interface pin description

Pin name	Pin description
CS	SPI enable I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
SCL/SPC	I^2C Serial Clock (SCL) SPI Serial Port Clock (SPC)
SDA/SDI/SDO	I^2C Serial Data (SDA) SPI Serial Data Input (SDI) 3-wire Interface Serial Data Output (SDO)
SDO	SPI Serial Data Output (SDO) I^2C less significant bit of the device address

4.1 I^2C serial interface

The LY530AL I^2C is a bus slave. The I^2C is employed to write data into registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 11. I^2C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the Serial Clock Line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines are connected to Vdd_IO through a pull-up resistor embedded inside the LY530AL. When the bus is free both the lines are high.

The I^2C interface is compliant with fast mode (400 kHz) I^2C standards as well as with the normal mode.

4.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the Master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the Master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the Master.

The Slave ADdress (SAD) associated to the LY530AL is 110100xb. **SDO** pin can be used to modify less significant bit of the device address. If SDO pin is connected to voltage supply LSb is '1' (address 1101001b) else if SDO pin is connected to ground LSb value is '0' (address 1101000b). This solution permits to connect and address two different gyroscopes to the same I²C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LY530AL behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, a 8-bit sub-address will be transmitted: the 7 LSb represent the actual register address while the MSB enables address auto increment. If the MSb of the SUB field is 1, the SUB (register address) will be automatically incremented to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition will have to be issued after the two sub-address bytes; if the bit is '0' (Write) the Master will transmit to the slave with direction unchanged. *Table* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 12. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SDO	R/W	SAD+R/W
Read	110100	0	1	11010001 (39h)
Write	110100	0	0	11010000 (38h)
Read	110100	1	1	11010011 (3Bh)
Write	110100	1	0	11010010 (3Ah)

Table 13. Transfer when Master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 14. Transfer when Master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 15. Transfer when Master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 16. Transfer when Master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real time function) the data line must be left HIGH by the slave. The Master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of first register to be read.

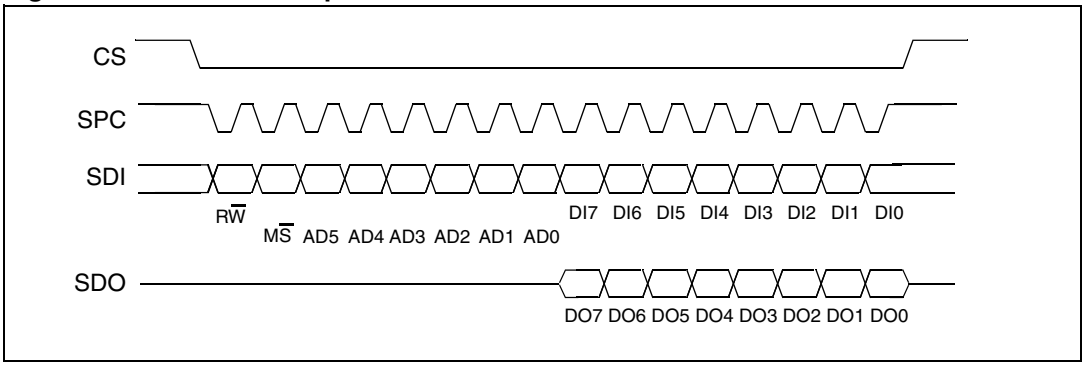
In the presented communication format MAK is Master Acknowledge and NMAK is No Master Acknowledge.

4.2 SPI bus interface

The LY530AL SPI is a bus slave. The SPI allows to write and read the registers of the device.

The Serial Interface interacts with the outside world with 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 6. Read & write protocol



CS is the Serial Port Enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the Serial Port Clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the Serial Port Data Input and Output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the Read Register and Write Register commands are completed in 16 clock pulses or in multiple of 8 in case of multiple bytes read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive **SDO** at the start of bit 8.

bit 1: M$\overline{S}$ bit. When 0, the address will remain unchanged in multiple read/write commands. When 1, the address will be auto incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that will be written into the device (MSb first).

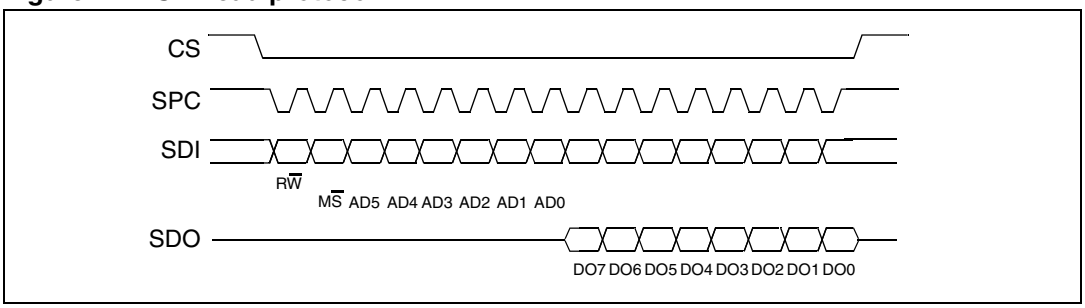
bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When M$\overline{S}$ bit is 0 the address used to read/write data remains the same for every block. When M$\overline{S}$ bit is 1 the address used to read/write data is incremented at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

4.2.1 SPI read

Figure 7. SPI read protocol



The SPI Read command is performed with 16 clock pulses. Multiple byte read command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: READ bit. The value is 1.

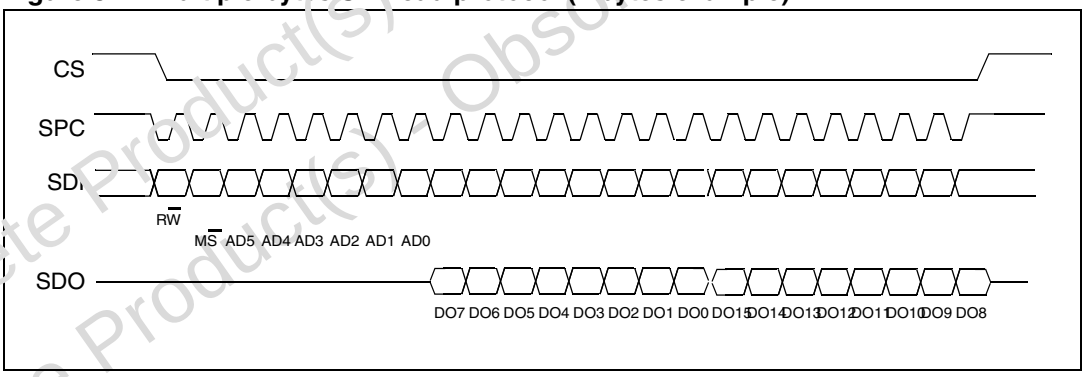
bit 1: MS bit. When 0 do not increment address, when 1 increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

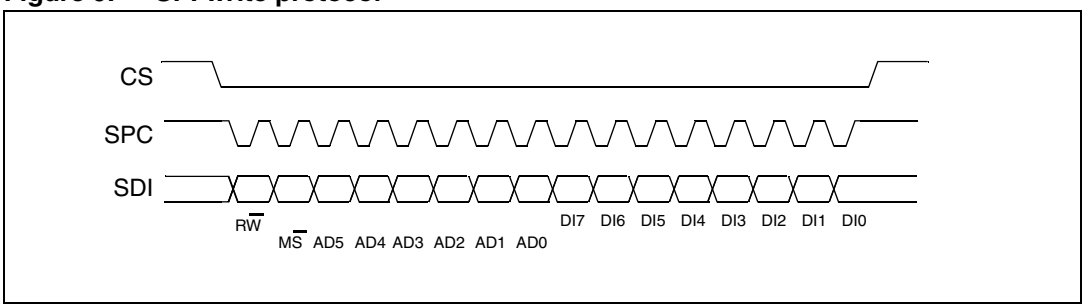
bit 16-... : data DO(...-8). Further data in multiple byte reading.

Figure 8. Multiple bytes SPI read protocol (2 bytes example)



4.2.2 SPI write

Figure 9. SPI write protocol



The SPI Write command is performed with 16 clock pulses. Multiple byte write command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: WRITE bit. The value is 0.

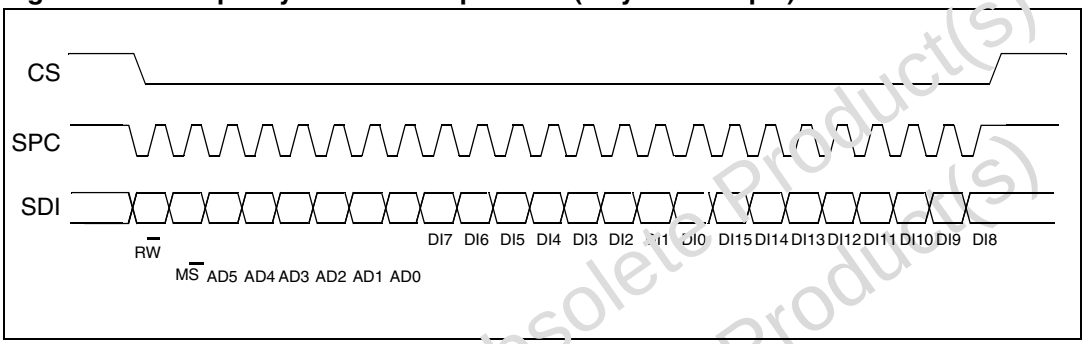
bit 1: MS bit. When 0 do not increment address, when 1 increment address in multiple writing.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that will be written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writing.

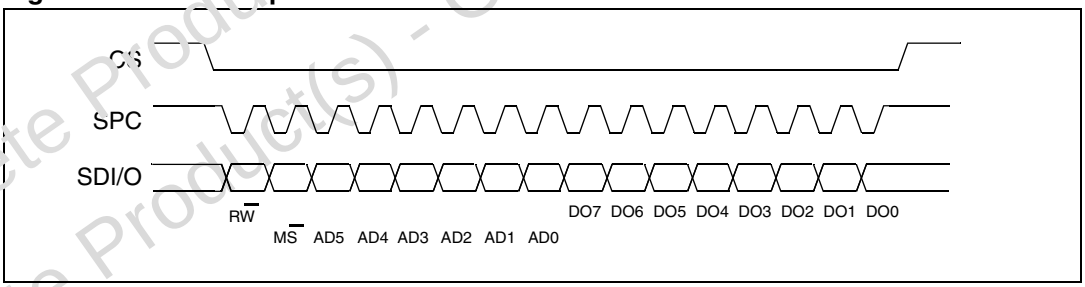
Figure 10. Multiple bytes SPI write protocol (2 bytes example)



4.2.3 SPI read in 3-wires mode

3-wires mode is entered by setting to 1 bit SIM (SPI Serial Interface Mode selection) in CTRL_REG2.

Figure 11. SPI read protocol in 3-wires mode



The SPI Read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: MS bit. When 0 do not increment address, when 1 increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

Multiple read command is also available in 3-wires mode.

5 Register mapping

The table given below provides a listing of the 8 bit registers embedded in the device and the related addresses:

Table 17. Registers addresses map

Name	Type	Register address		Default	Comment
		Hex	Binary		
Reserved (do not modify)		00-0E			Reserved
WHO_AM_I	r	0F	000 1111	11010001	Dummy register
Reserved (do not modify)		10-1F			Reserved
CTRL_REG	rw	20	010 0000	00000000	
Reserved (do not modify)		21	010 0001		Reserved
FILTER_CFG_REG	rw	22	010 0010		Loaded at boot
OUTPUT_SEL_REG	rw	23	010 0011	00000000	
Reserved (do not modify)		24	001 1000		Reserved
Reserved (do not modify)		25	001 1001		Reserved
Reserved (do not modify)		26	001 1010		Reserved
STATUS_REG	r	27	010 0111	00000000	
OUT_CONV_H	r	28	010 1000		
OUT_CONV_L	r	29	010 1001		

Registers marked as “Reserved” or not listed must not be changed. The writing to those registers may cause permanent damages to the device.

6 Register description

The device contains a set of registers which are used to control its behavior and to retrieve angular rate data. The registers address, made of 7 bits, is used to identify them and to write the data through serial interface.

6.1 WHO_AM_I (0Fh)

Table 18. WHO_AM_I register

1	1	0	1	0	0	0	1

Device identification register.

This register contains the device identifier that for LY530AL is set to D1h.

6.2 CTRL_REG (20h)

Table 19. CTRL_REG register

TUD_SDO	DIG_en	0(1)	IF_SEL	BDU	alg	BOOT	SIM

1. '0' is the default value. This value must not be changed

Table 20. CTRL_REG description

TUD_SDO	Pull Up disable for SDO pin. Default value: 0 (0: Pull Up connected; 1: Pull Up disabled)
DIG_en	Power Down bit. Default value: 0 (0: Device is in power down mode; 1: Divice is in normal mode)
IF_SEL	Interface selection. Default value: 0 (0: both interfaces available; 1: IF_DIS pin value selects the interface)
BDU	Block data update. Default value: 0 (0: continuos update; 1: update inhibited)
alg	Data alignment selection bit. Default value: 0 (0: 16 bit left justified; 1: 10 bit right justified)
BOOT	Reboot of memory content. Default value: 0 (0: normal mode; 1: memory reboot)
SIM	SPI serial interface mode selection bit. Default value: 0 (0: 4-wire mode; 1:3-wire mode)

TUD_SDO: When this bit is set to '1' the Pull Up on SDO pin is disabled.

DIG_en: When this bit is set to '1' the device is in normal mode. When DIG_en bit is '0' the device is in power down mode.

IF_SEL: Setting this bit to '1' the voltage value applied to IF_DIS pin selects one of the two digital interfaces ('1' for I2C only, '0' for SPI only).

BDU: This bit is used to inhibit output registers update until both upper and lower parts are read. In default mode (BDU='0') the output registers values are updated continuosly. It is recommended to set BDU bit to '1' if the reading is not faster than the output data rate.

alg: This bit permits to decide between 16 bits left justified (default value) and 10 bits right justified representation of data coming from the device. In this last case the most significant bits are replaced by the bit representing the sign.

BOOT bit is used to refresh the content of internal registers stored in the flash memory block. At the device power up the content of the flash memory block is transferred to the internal registers related to trimming functions to permit a good behavior of the device itself. If for any reason the content of trimming registers was changed it is sufficient to use this bit to restore correct values. When BOOT bit is set to '1' the content of internal flash is copied inside corresponding internal registers and it is used to calibrate the device. These values are factory trimmed and they are different for every gyroscope. They permit a good behavior of the device and normally they have not to be changed. At the end of the boot process the BOOT bit is set again to '0'.

SIM bit selects the SPI Serial Interface Mode. When SIM is '0' (default value) the 4-wire interface mode is selected. The data coming from the device are sent to SDO pin. In 3-wire interface mode output data are sent to SDA/SDI/SDO pin.

6.3 FILTER_CFG_REG (22h)

Table 21. FILTER_CFG_REG register

HP_BW1	HP_BW0	LP_BW2	LP_BW1	LP_BW0	0 (1)	0	0

1. 0 is the default value loaded at boot. This value must not be changed.

Table 22. FILTER_CFG_REG description

HP_BW(1-0)	High pass filter pole frequency selection
LP_BW(2-0)	Low pass filter pole frequency selection

Table 23. High pass filter pole -3dB frequency selection

HP_BW[1:0]	Pole frequency [Hz]
00	1.25
01	0.31
10	0.15
11	0.08

Table 24. Low pass filter pole -3dB frequency selection

LP_BW[2:0]	Pole frequency [Hz]
000	115
001	46.1
010	21.3

Table 24. Low pass filter pole -3dB frequency selection (continued)

LP_BW[2:0]	Pole frequency [Hz]
011	10.3
100	5.1
101	2.5
110	1.2
111	0.6

6.4 OUTPUT_SEL_REG (23h)

Table 25. OUTPUT_SEL_REG register

X	X	ST_bit	X	X	OUT2	OUT1	OUT0

Table 26. OUTPUT_SEL_REG description

ST_bit	When Dig_en is set to '1', ST_bit enables Selft Test function. Default value: 0 (0: no selft test activated; 1: self test enabled)
OUT2-0	Output data filtering selection

Table 27. Filtering selection

OUTPUT_SEL_REG[2:0]	Filter type
000	no filtering
001	high pass
011	2 x high pass
100	low pass
101	high pass + low pass
111	2 x high pass + low pass

Table 28. Forbidden combinations

FILTER_CFG_REG[2:0]	OUTPUT_SEL_REG[2:0]
101	111
101	100
100	111
100	101
111	101
111	100

6.5 STATUS_REG(27h)

Table 29. STATUS_REG(27h) register

X(1)	X	X	X	X	ow	davbH	davbL

1. Undefined value

Table 30. STATUS_REG(27h) description

ow	Digital data overrun. When '1', output registers have been updated before being read.
davbH	When this bit is '1', new data is available on OUT_CONV_H (high part)
davbL	When this bit is '1', new data is available on OUT_CONV_L (low part)

6.6 OUT_CONV_H(28h)

Table 31. OUT_CONV_H register

DOH7	DOH6	DOH5	DOH4	DOH3	DOH2	DOH1	DOH0

These bits are the high part of digital output expressed as 2's complement number. For data alignment see alg bit in CTRL_REG(20h) (*Table 20*).

6.7 OUT_CONV_L(29h)

Table 32. OUT_CONV_L register

DOL7	DOL6	DOL5	DOL4	DOL3	DOL2	DOL1	DOL0

These bits are the lowpart of digital output expressed as 2's complement number. For data alignment see alg bit in CTRL_REG(20h) (*Table 20*).

7 Package information

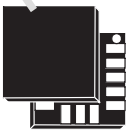
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK® is an ST trademark.

ECOPACK® specifications are available at: www.st.com.

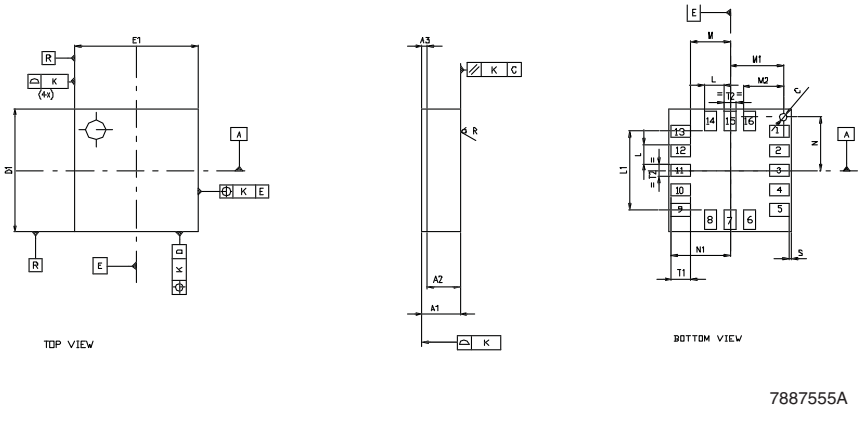
Figure 12. LGA-16: mechanical data and package dimensions

Dimensions						
Ref.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A1	1.46	1.5	1.6	0.057	0.059	0.063
A2			1.33			0.052
A3	0.16	0.2	0.24	0.006	0.008	0.009
C		0.3			0.012	
D1	4.85	5	5.15	0.191	0.197	0.203
E1	4.85	5	5.15	0.191	0.197	0.203
L		0.8			0.031	
L1		3.2			0.126	
M		1.6			0.062	
M1	2.15	2.175	2.20	0.085	0.086	0.087
M2		1.625			0.064	
N		2.175			0.086	
N1		2.4			0.094	
T1		0.8			0.031	
T2	0.475	0.5	0.525	0.019	0.020	0.021
R	1.2		1.6	0.047		0.063
S		0.1			0.004	
h		0.15			0.006	
k		0.05			0.002	
j		0.1			0.004	

Outline and mechanical data



LGA-16 (5x5x1.6mm)
Land Grid Array Package



8 Revision history

Table 33. Document revision history

Date	Revision	Changes
03-Sep-2008	1	Initial release

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