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# NTD5805N, NVD5805N

## Power MOSFET 40 V, 51 A, Single N-Channel, DPAK

### Features

- Low  $R_{DS(on)}$
- High Current Capability
- Avalanche Energy Specified
- NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### Applications

- LED Backlight Driver
- CCFL Backlight
- DC Motor Control
- Power Supply Secondary Side Synchronous Rectification

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DSS}$	40	V	
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 20$	V	
Gate-to-Source Voltage – Non-Repetitive ( $t_p < 10 \mu\text{s}$ )	$V_{GS}$	$\pm 30$	V	
Continuous Drain Current ( $R_{\theta JC}$ ) (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	51	A
		$T_C = 100^\circ\text{C}$	36	
Power Dissipation ( $R_{\theta JC}$ ) (Note 1)		$T_C = 25^\circ\text{C}$	47	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	$I_{DM}$	85	A
Operating Junction and Storage Temperature	$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$	
Source Current (Body Diode)	$I_S$	30	A	
Single Pulse Drain-to-Source Avalanche Energy ( $V_{DD} = 50 \text{ V}, V_{GS} = 10 \text{ V}, R_G = 25 \Omega, I_{L(pk)} = 40 \text{ A}, L = 0.1 \text{ mH}, V_{DS} = 40 \text{ V}$ )	$E_{AS}$	80	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	3.2	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	107	

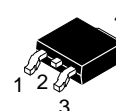
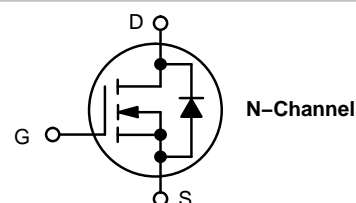
1. Surface-mounted on FR4 board using the minimum recommended pad size.



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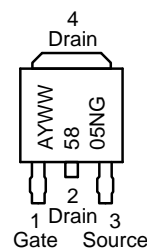
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
40 V	16 m $\Omega$ @ 5.0 V	51 A
	9.5 m $\Omega$ @ 10 V	



DPAK  
 CASE 369C  
 (Surface Mount)  
 STYLE 2

### MARKING DIAGRAM & PIN ASSIGNMENT



- A = Assembly Location\*
- Y = Year
- WW = Work Week
- 5805N = Device Code
- G = Pb-Free Package

\* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

## NTD5805N, NVD5805N

**ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	40			V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			40.8		mV/°C	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}$	$T_J = 25^\circ\text{C}$			1.0	$\mu\text{A}$
			$T_J = 150^\circ\text{C}$			100	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA	

**ON CHARACTERISTICS** (Note 2)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.5		3.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			7.04		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$		7.6	9.5	m $\Omega$
		$V_{GS} = 5.0\text{ V}, I_D = 10\text{ A}$		10.9	16	
Forward Transconductance	$g_{FS}$	$V_{DS} = 15\text{ V}, I_D = 15\text{ A}$		8.54		S

**CHARGES, CAPACITANCES AND GATE RESISTANCES**

Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 25\text{ V}$		1725		pF
Output Capacitance	$C_{oss}$			220		
Reverse Transfer Capacitance	$C_{rss}$			160		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 32\text{ V}, I_D = 30\text{ A}$		33	80	nC
Threshold Gate Charge	$Q_{G(TH)}$			2.0		
Gate-to-Source Charge	$Q_{GS}$			7.2		
Gate-to-Drain Charge	$Q_{GD}$			9.8		

**SWITCHING CHARACTERISTICS** (Note 3)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DD} = 32\text{ V}, I_D = 30\text{ A}, R_G = 2.5\ \Omega$		10.2		ns
Rise Time	$t_r$			17.9		
Turn-Off Delay Time	$t_{d(off)}$			22.9		
Fall Time	$t_f$			4.5		

**DRAIN-SOURCE DIODE CHARACTERISTICS**

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 10\text{ A}$	$T_J = 25^\circ\text{C}$		0.83	1.2	V
			$T_J = 150^\circ\text{C}$		0.65		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, di/dt = 100\text{ A}/\mu\text{s}, I_S = 30\text{ A}$		24.8		ns	
Charge Time	$t_a$			14.6			
Discharge Time	$t_b$			10.2			
Reverse Recovery Charge	$Q_{RR}$			15.5			nC

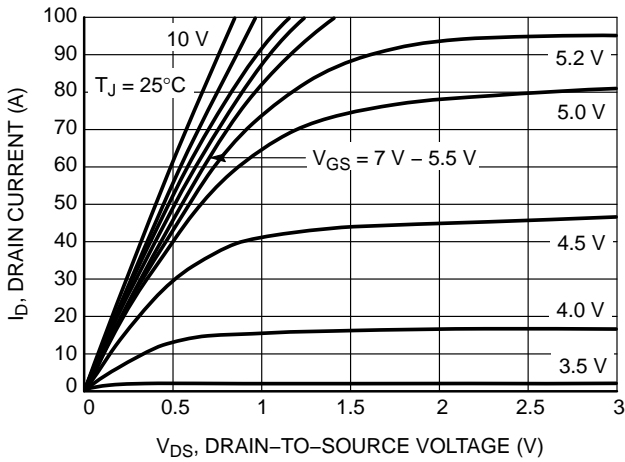
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

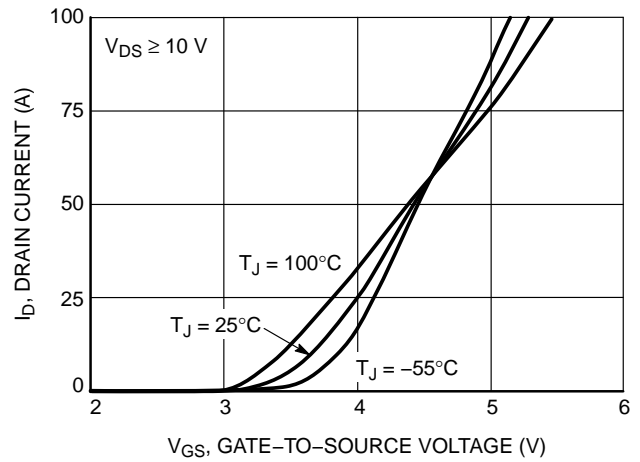
3. Switching characteristics are independent of operating junction temperatures.

**NTD5805N, NVD5805N**

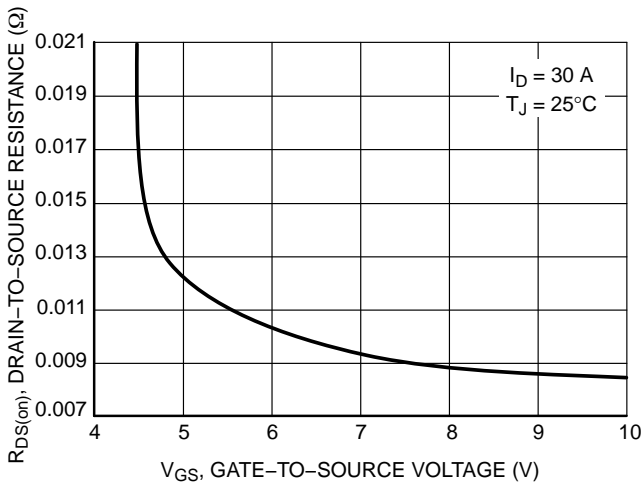
**TYPICAL PERFORMANCE CHARACTERISTICS**



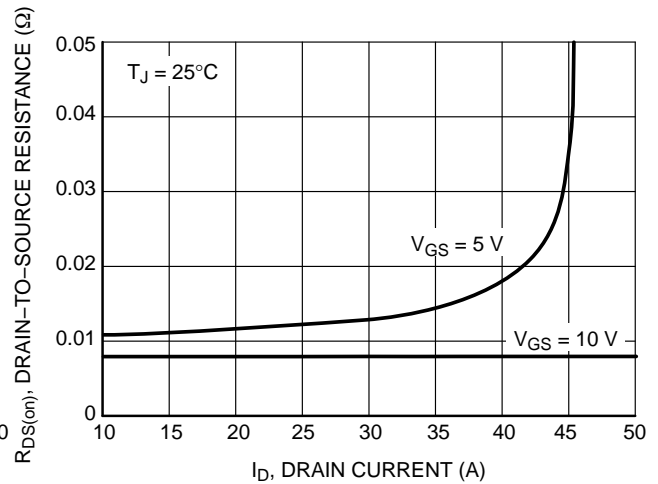
**Figure 1. On-Region Characteristics**



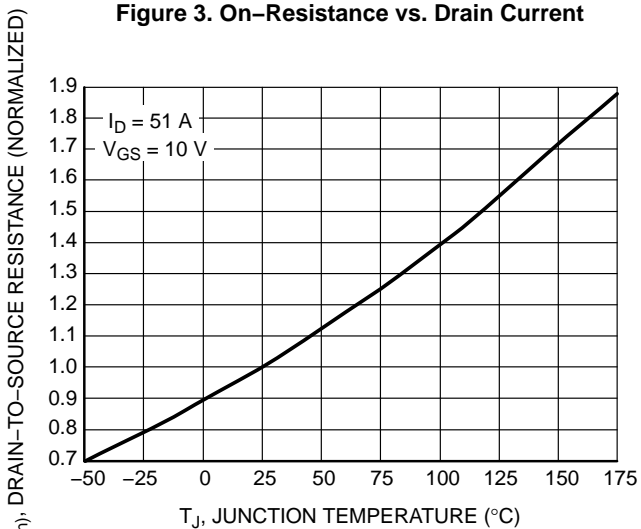
**Figure 2. Transfer Characteristics**



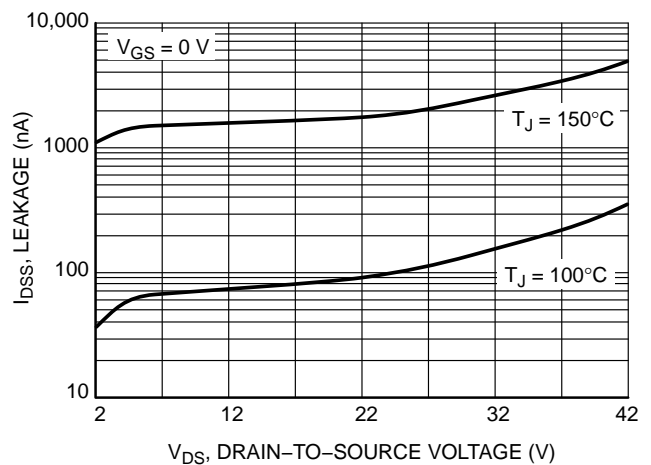
**Figure 3. On-Resistance vs. Drain Current**



**Figure 4. On-Resistance vs. Drain Current and Gate Voltage**



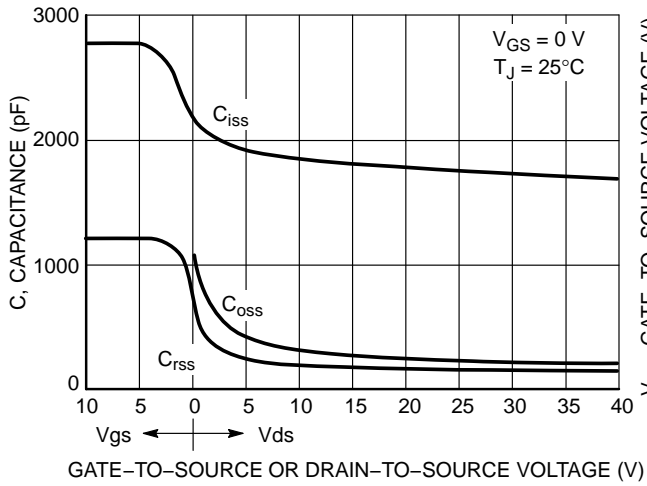
**Figure 5. On-Resistance Variation with Temperature**



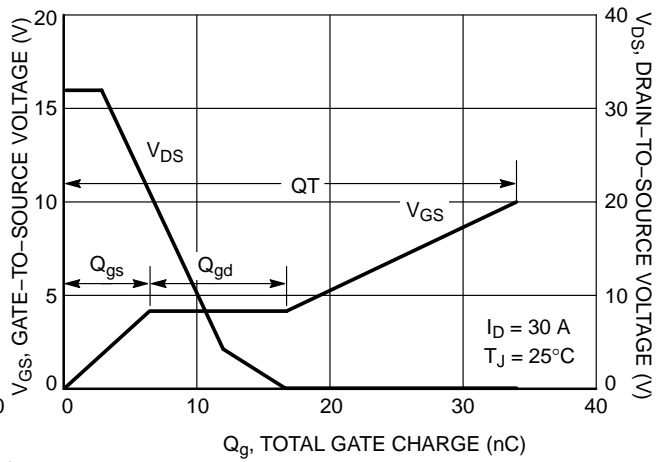
**Figure 6. Drain-to-Source Leakage Current vs. Voltage**

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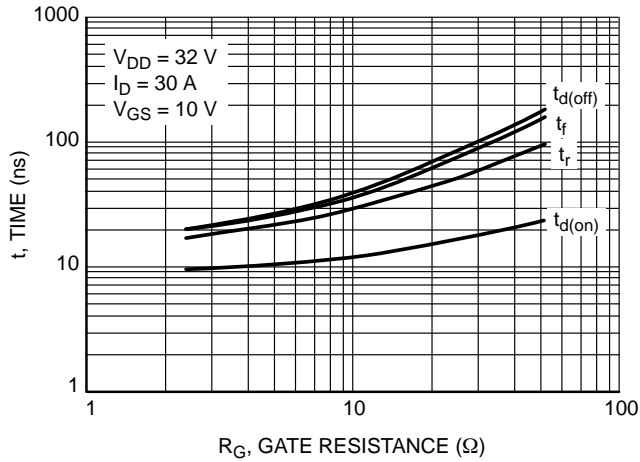
**TYPICAL PERFORMANCE CHARACTERISTICS**



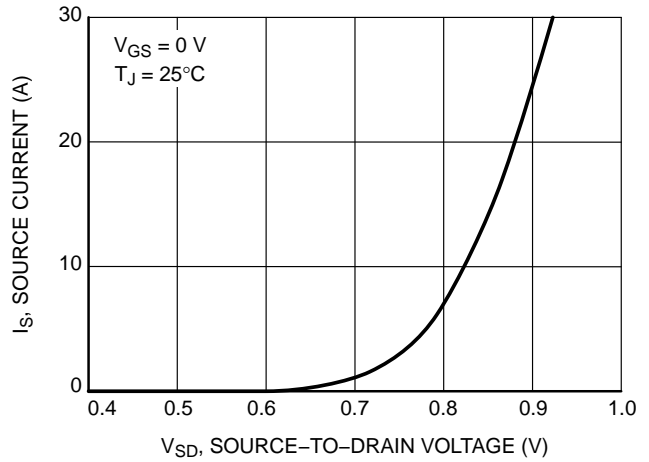
**Figure 7. Capacitance Variation**



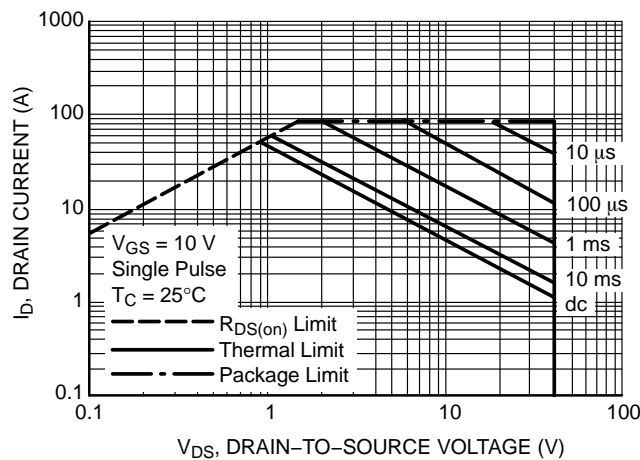
**Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge**



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**



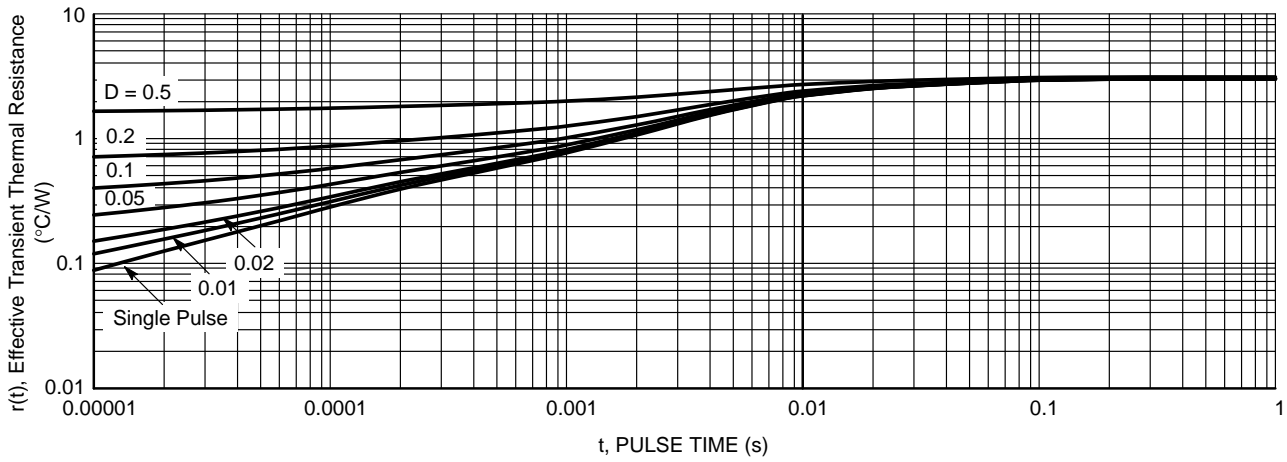
**Figure 10. Diode Forward Voltage vs. Current**



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

**NTD5805N, NVD5805N**

**TYPICAL PERFORMANCE CHARACTERISTICS**



**Figure 12. Thermal Response**

**ORDERING INFORMATION**

Order Number	Package	Shipping†
NTD5805NT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NVD5805NT4G*	DPAK (Pb-Free)	2500 / Tape & Reel

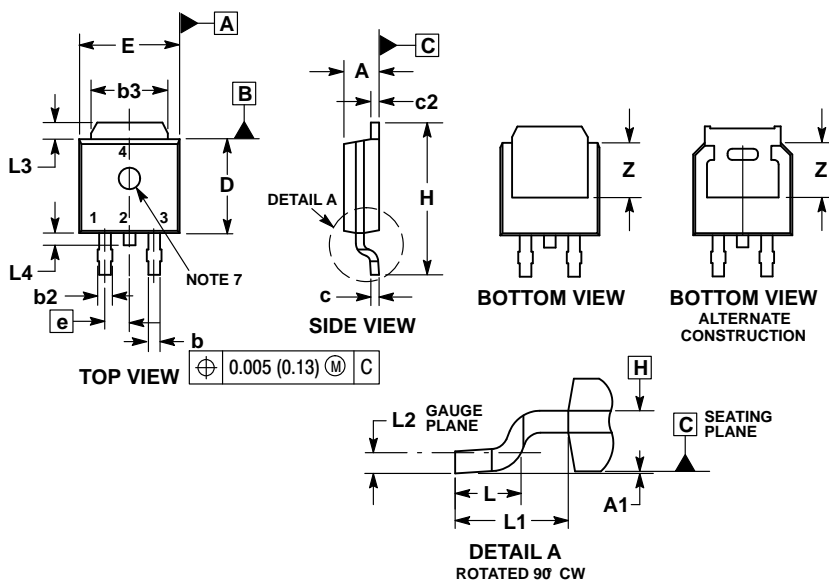
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

## NTD5805N, NVD5805N

### PACKAGE DIMENSIONS

#### DPAK (SINGLE GAUGE) CASE 369C ISSUE E

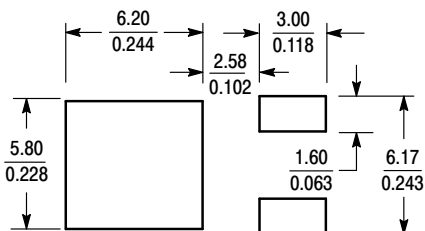


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

#### SOLDERING FOOTPRINT\*



SCALE 3:1 (mm/inches)

STYLE 2:

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

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