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IR3500V

DATA SHEET

XPHASE3™ VR11.1 CPU VTT CONTROL IC

DESCRIPTION

The IR3500V Control IC combined with one or more *xPhase3*™ Phase IC implement the control and MOSFET driver functions for a VR11.1 CPU VTT power supply.

FEATURES

- 1 to X phase operation with matching Phase IC
- 0.7% overall system set point accuracy
- Programmable 250kHz to 9MHz Daisy-chain digital phase timing clock oscillator frequency provides a per phase switching frequency of 250kHz to 1.5MHz without external components
- Programmable Dynamic VID Slew Rate
- Programmable Load Line Output Impedance
- High speed error amplifier with wide bandwidth of 30MHz and fast slew rate of 12V/us
- Programmable converter current limit during soft start, hiccup with delay during normal operation
- Central over voltage detection with programmable threshold and communication to phase IC(s)
- Over voltage signal output to system with overvoltage detection during powerup and normal operation
- Detection and protection of open remote sense line and open control loop
- IC bias linear regulator control with programmable output voltage and UVLO
- Programmable VRHOT function monitors temperature of power stage through a NTC thermistor
- Remote sense amplifier with true converter voltage sensing and less than 50uA bias current
- Simplified PGOOD output provides indication of proper operation and avoids false triggering
- Small thermally enhanced 32L 5mm x 5mm MLPQ package
- RoHS Compliant

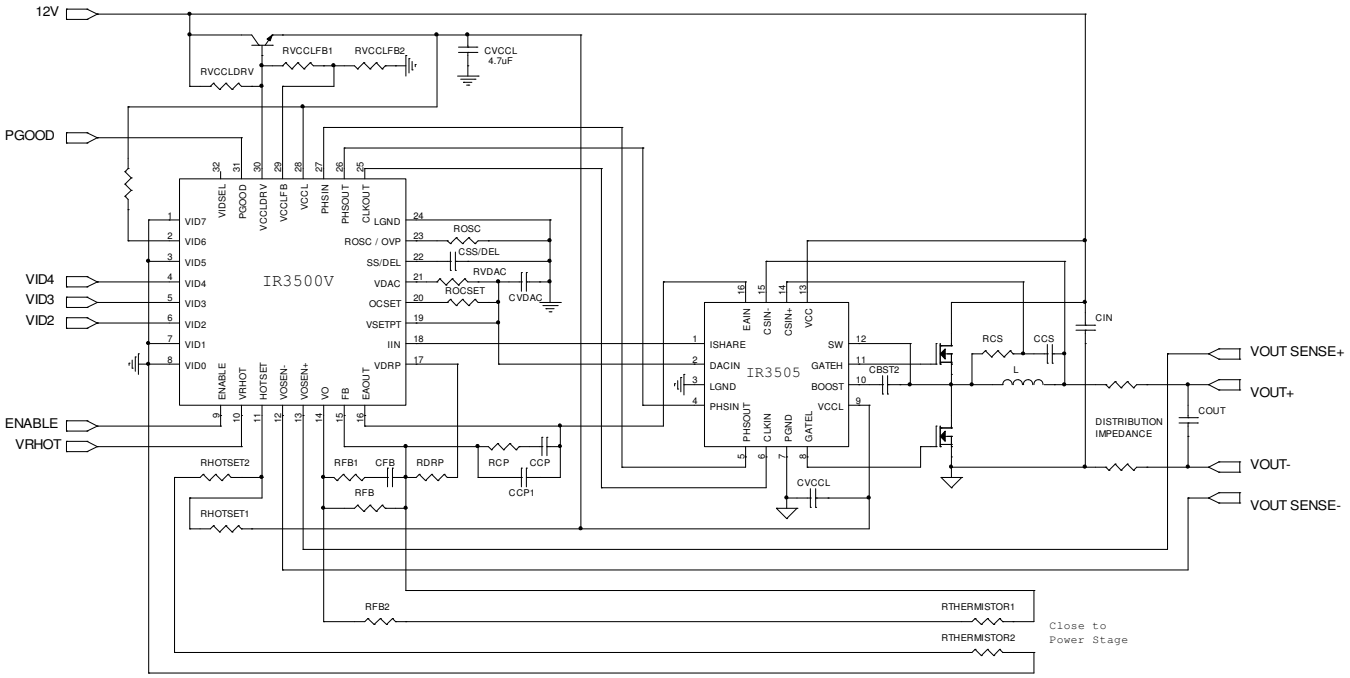


Figure 1 – Single Phase VR11.1 CPU VTT Application Circuit

ORDERING INFORMATION

Device	Package	Order Quantity
IR3500V MTRPBF	32 Lead MLPQ (5 x 5 mm body)	3000 per reel
* IR3500V MPBF *Samples only	32 Lead MLPQ (5 x 5 mm body)	100 piece strips

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed below may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

Operating Junction Temperature…….. 0°C to 150°C
Storage Temperature Range……-65°C to 150°C
ESD Rating……HBM Class 1C JEDEC Standard
MSL Rating……2
Reflow Temperature……260°C

PIN #	PIN NAME	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
1-8	VID7-0	7.5V	-0.3V	1mA	1mA
9	ENABLE	3.5V	-0.3V	1mA	1mA
10	VRHOT	7.5V	-0.3V	1mA	50mA
11	HOTSET	7.5V	-0.3V	1mA	1mA
12	VOSEN-	1.0V	-0.5V	5mA	1mA
13	VOSEN+	7.5V	-0.5V	5mA	1mA
14	VO	7.5V	-0.3V	5mA	25mA
15	FB	7.5V	-0.3V	1mA	1mA
16	EAOUT	7.5V	-0.3V	25mA	10mA
17	VDRP	7.5V	-0.3V	35mA	1mA
18	IIN	7.5V	-0.3V	100mA	1mA
19	VSETPT	3.5V	-0.3V	1mA	1mA
20	OCSET	7.5V	-0.3V	1mA	1mA
21	VDAC	3.5V	-0.3V	1mA	1mA
22	SS/DEL	7.5V	-0.3V	1mA	1mA
23	ROSC/OVP	7.5V	-0.3V	1mA	1mA
24	LGND	n/a	n/a	20mA	1mA
25	CLKOUT	7.5V	-0.3V	100mA	100mA
26	PHSOUT	7.5V	-0.3V	10mA	10mA
27	PHSIN	7.5V	-0.3V	1mA	1mA
28	VCCL	7.5V	-0.3V	1mA	20mA
29	VCCLFB	3.5V	-0.3V	1mA	1mA
30	VCCLDRV	10V	-0.3V	1mA	50mA
31	PGOOD	VCCL + 0.3V	-0.3V	1mA	20mA
32	VIDSEL	7.5V	-0.3V	5mA	1mA

RECOMMENDED OPERATING CONDITIONS FOR RELIABLE OPERATION WITH MARGIN

4.75V ≤ V_{CCL} ≤ 7.5V, -0.3V ≤ VOSEN- ≤ 0.3V, 0 °C ≤ T_J ≤ 100 °C, 7.75KΩ ≤ R_{OSC} ≤ 50.0 KΩ

ELECTRICAL SPECIFICATIONS

The electrical characteristics involve the spread of values guaranteed within the recommended operating conditions. Typical values represent the median values, which are related to 25°C. $C_{SS/DEL}$ = 0.1µF +/-10%.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VDAC Reference					
System Set-Point Accuracy	Deviation from Table 1 per test circuit in Figure 2	-0.7		0.7	%
Source & Sink Currents	Include OCSET and VSETPT currents	30	44	58	µA
VR11 VIDx Input Threshold	Float VIDSEL	500	600	700	mV
VR11 VIDx Input Bias Current	Float VIDSEL. 0V ≤ V(VIDx) ≤ 2.5V.	-1	0	1	µA
VIDSEL Pull-up Resistance		3.0	4.0	5.0	KΩ
Oscillator					
ROSC Voltage		0.570	0.595	0.620	V
CLKOUT High Voltage	I(CLKOUT)= -10 mA, measure V(VCCL) – V(CLKOUT).			1	V
CLKOUT Low Voltage	I(CLKOUT)= 10 mA			1	V
PHSOUT Frequency	R_{OSC} = 50.0 KΩ	225	250	275	kHz
PHSOUT Frequency	R_{OSC} = 24.5 KΩ	450	500	550	kHz
PHSOUT Frequency	R_{OSC} = 7.75 KΩ	1.35	1.50	1.65	MHz
PHSOUT High Voltage	I(PHSOUT)= -1 mA, measure V(VCCL) – V(PHSOUT)			1	V
PHSOUT Low Voltage	I(PHSOUT)= 1 mA			1	V
PHSIN Threshold Voltage	Compare to V(VCCL)	30	50	70	%
Remote Sense Differential Amplifier					
Unity Gain Bandwidth	Note 1	3.0	6.4	9.0	MHz
Input Offset Voltage	1V≤ V(VOSEN+) - V(VOSEN-)	-3	0	3	mV
Source Current	1V≤ V(VOSEN+) - V(VOSEN-)	0.5	1.0	1.7	mA
Sink Current	1V≤ V(VOSEN+) - V(VOSEN-)	2	12	18	mA
Slew Rate	1V≤ V(VOSEN+) - V(VOSEN-) Note1	2	4	8	V/us
VOSEN+ Bias Current	1 V < V(VOSEN+)		30	50	uA
VOSEN- Bias Current	-0.3V ≤ VOSEN- ≤ 0.3V, All VID Codes		30	50	uA
VOSEN+ Input Voltage Range	V(VCCL)=7V			5.5	V
High Voltage	V(VCCL) – V(VO)		0.5	1	V
Low Voltage	V(VCCL)=7V			250	mV
Enable Input					
VR 11 Threshold Voltage	ENABLE rising	830	855	880	mV
VR 11 Threshold Voltage	ENABLE falling	780	805	830	mV
VR 11 Hysteresis		25	50	75	mV
Bias Current	0V ≤ V(ENABLE) ≤ 3.3V	-5	0	5	µA
Blanking Time	Noise Pulse < 100ns will not register an ENABLE state change. Note 1	75	250	400	ns

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Soft Start and Delay					
Start Delay (TD1)		1.0	2.9	3.5	ms
Soft Start Time (TD2)	To reach 1.1V	0.8	2.2	3.25	ms
VID Sample Delay (TD3)		0.3	1.2	3.0	ms
PGOOD Delay (TD4 + TD5)		0.5	1.2	2.3	ms
OC Delay Time	V(IIN) – V(OCSET) = 500 mV	75	125	300	us
SS/DEL to FB Input Offset Voltage	With FB = 0V, adjust V(SS/DEL) until EAOUT drives high	0.7	1.4	1.9	V
Charge Current		35.0	52.5	70.0	µA
Discharge Current		2.5	4.5	6.5	µA
Charge/Discharge Current Ratio		10	12	16	µA/µA
Charge Voltage			3.75		V
Delay Comparator Threshold	Relative to Charge Voltage, SS/DEL rising		80		mV
Delay Comparator Threshold	Relative to Charge Voltage, SS/DEL falling		110		mV
Delay Comparator Hysteresis			30		mV
VID Sample Delay Comparator Threshold			3.0		V
Discharge Comp. Threshold		150	200	275	mV
Error Amplifier					
Input Offset Voltage	Measure V(FB) – V(VSETPT). Note 2	-1	0	1	mV
FB Bias Current		-1	0	1	µA
VSETPT Bias Current	ROSC= 24.5 KΩ	23.00	24.25	25.50	µA
DC Gain	Note 1	100	110	120	dB
Bandwidth	Note 1	20	30	40	MHz
Slew Rate	Note 1	7	12	20	V/µs
Sink Current		0.40	0.85	1.00	mA
Source Current		5	8	12	mA
Minimum Voltage			120	250	mV
Maximum Voltage	Measure V(VCCL) – V(EAOUT)	500	780	950	mV
Open Voltage Loop Detection Threshold	Measure V(VCCL) - V(EAOUT), Relative to Error Amplifier maximum voltage.	125	300	600	mV
Open Voltage Loop Detection Delay	Measure PHSOUT pulse numbers from V(EAOUT) = V(VCCL) to PGOOD = low.		8		Pulses
Over-Current Comparator					
Input Offset Voltage	1V ≤ V(OCSET) ≤ 3.3V	-30	-13	0	mV
OCSET Bias Current	ROSC= 24.5 KΩ	23.25	24.50	25.75	µA
Over-Current Delay Counter	ROSC = 7.75 KΩ (PHSOUT=1.5MHz)		4096		Cycle
Over-Current Delay Counter	ROSC = 15.0 KΩ (PHSOUT=800kHZ)		2048		Cycle
Over-Current Delay Counter	ROSC = 50.0 KΩ (PHSOUT=250kHz)		1024		Cycle
Over-Current Limit Amplifier					
Input Offset Voltage		-10	0	10	mV
Transconductance	Note 1	0.50	1.00	1.75	mA/V
Sink Current		35	55	75	uA
Unity Gain Bandwidth	Note 1	0.75	2.00	3.00	kHz

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Over Voltage Protection (OVP) Comparators					
Threshold at Power-up		1.60	1.73	1.83	V
Threshold during Normal Operation	Compare to V(VDAC)	110	130	150	mV
OVP Release Voltage during Normal Operation	Compare to V(VDAC)	-13	3	20	mV
Threshold during Dynamic VID down		1.72	1.75	1.77	V
Dynamic VID Detect Comparator Threshold		25	50	75	mV
Propagation Delay to IIN	Measure time from V(VO) > V(VDAC) (250mV overdrive) to V(IIN) transition to > 0.9 * V(VCCL).		90	180	ns
IIN Pull-up Resistance			5	15	Ω
Propagation Delay to OVP	Measure time from V(VO) > V(VDAC) (250mV overdrive) to V(ROSC/OVP) transition to >1V.		90	180	ns
OVP High Voltage	Measure V(VCCL)-V(ROSC/OVP)	0		1.2	V
OVP Power-up High Voltage	V(VCCLDRV)=1.8V. Measure V(VCCL)-V(ROSC/OVP)	0		0.2	V
VDRP Buffer Amplifier					
Input Offset Voltage	V(VDRP) – V(IIN), 0.5V ≤ V(IIN) ≤ 3.3V	-5	3	11	mV
Source Current	0.5V ≤ V(IIN) ≤ 3.3V	2		30	mA
Sink Current	0.5V ≤ V(IIN) ≤ 3.3V	0.2	0.4	0.6	mA
Unity Gain Bandwidth	Note 1		8		MHz
Slew Rate	Note 1		4.7		V/µs
IIN Bias Current		-1	0	1	µA
PGOOD Output					
Output Voltage	I(PGOOD) = 4mA		150	300	mV
Leakage Current	V(PGOOD) = 5.5V		0	10	µA
Under Voltage Threshold-VO decreasing	Reference to VDAC	-380	-330	-280	mV
Under Voltage Threshold-VO increasing	Reference to VDAC	-315	-265	-215	mV
Under Voltage Threshold Hysteresis		25	60	95	mV
VCCL_DRV Activation Threshold	I(PG)=4mA, V(PG)<400mV, V(VCCL)=0	1	2	3.6	V
Open Sense Line Detection					
Sense Line Detection Active Comparator Threshold Voltage		150	200	250	mV
Sense Line Detection Active Comparator Offset Voltage	V(VO) < [V(VOSEN+) – V(LGND)] / 2	35	60	85	mV
VOSEN+ Open Sense Line Comparator Threshold	Compare to V(VCCL)	87.5	90.0	92.5	%
VOSEN- Open Sense Line Comparator Threshold		0.36	0.40	0.44	V
Sense Line Detection Source Currents	V(VO) = 100mV	200	500	700	uA

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VCCL Regulator Amplifier					
Reference Feedback Voltage		1.15	1.19	1.23	V
VCCLFB Bias Current		-1	0	1	uA
VCCLDRV Sink Current		10	30		mA
UVLO Start Threshold	Compare to V(VCCL)	91	93	99	%
UVLO Stop Threshold	Compare to V(VCCL)	83	87	91	%
Hysteresis	Compare to V(VCCL)	7	8.25	9.5	%
General					
VCCL Supply Current		3.0	6.5	10.0	mA

Note 1: Guaranteed by design, but not tested in production
Note 2: VDAC Output is trimmed to compensate for Error Amplifier input offset errors

VID CODES & SYSTEM SET POINT

VID Hex	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VSET
40	0	1	0	0	0	0	0	0	1.220
44				0	0	1			1.195
48				0	1	0			1.170
4C				0	1	1			1.145
50				1	0	0			1.120
54				1	0	1			1.095
58				1	1	0			1.070
5C				1	1	1			1.045

Table 1 – VR11.1 CPU VTT VID Codes

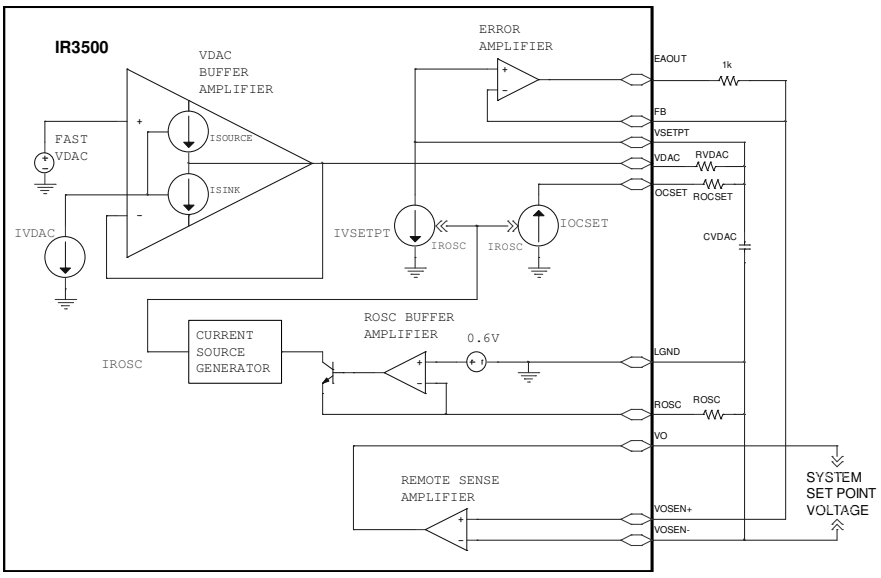


Figure 2 - System Set Point Test Circuit for VR11.1 VTT VID

PIN DESCRIPTION

PIN#	PIN SYMBOL	PIN DESCRIPTION
1-8	VID7-0	VID0, 1, 5, 7 are grounded. VID6 is pulled up. VID2~4 are inputs to VID D to A converter.
9	ENABLE	Enable input. A logic low applied to this pin puts the IC into fault mode. Do not float this pin as the logic state will be undefined.
10	VRHOT	Open collector output of the VRHOT comparator which drives low if HOTSET pin voltage is lower than 1.6V. Connect external pull-up.
11	HOTSET	A resistor divider including thermistor senses the temperature, which is used for VRHOT comparator.
12	VOSEN-	Remote sense amplifier input. Connect to ground at the load.
13	VOSEN+	Remote sense amplifier input. Connect to output at the load.
14	VO	Remote sense amplifier output.
15	FB	Inverting input to the error amplifier.
16	EAOUT	Output of the error amplifier.
17	VDRP	Buffered IIN signal. Connect an external RC network to FB to program converter output impedance.
18	IIN	Average current input from the phase IC(s). This pin is also used to communicate over voltage condition to phase ICs.
19	VSETPT	Error amplifier non-inverting input. Converter output voltage can be decreased from the VDAC voltage with an external resistor connected between VDAC and this pin (there is an internal sink current at this pin).
20	OCSET	Programs the constant converter output current limit and hiccup over-current thresholds through an external resistor tied to VDAC and an internal current source from this pin. Over-current protection can be disabled by connecting a resistor from this pin to VDAC to program the threshold higher than the possible signal into the IIN pin from the phase ICs but no greater than VCCL – 2V (do not float this pin as improper operation will occur).
21	VDAC	Regulated voltage programmed by the VID inputs. Connect an external RC network to LGND to program dynamic VID slew rate and provide compensation for the internal buffer amplifier.
22	SS/DEL	Programs converter startup and over current protection delay timing. It is also used to compensate the constant output current loop during soft start. Connect an external capacitor to LGND to program.
23	ROSC/OVP	Connect a resistor to LGND to program oscillator frequency and OCSET, VSETPT and VDAC bias currents. Oscillator frequency equals switching frequency per phase. The pin voltage is 0.6V during normal operation and higher than 1.6V if over-voltage condition is detected.
24	LGND	Local Ground for internal circuitry and IC substrate connection.
25	CLKOUT	Clock output at switching frequency multiplied by phase number. Connect to CLKIN pins of phase ICs.
26	PHSOUT	Phase clock output at switching frequency per phase. Connect to PHSIN pin of the first phase IC.
27	PHSIN	Feedback input of phase clock. Connect to PHSOUT pin of the last phase IC.
28	VCCL	Output of the voltage regulator, and power input for clock oscillator circuitry. Connect a decoupling capacitor to LGND.
29	VCCLFB	Non-inverting input of the voltage regulator error amplifier. Output voltage of the regulator is programmed by the resistor divider connected to VCCL.

30	VCCLDRV	Output of the VCCL regulator error amplifier to control external transistor. The pin senses 12V power supply through a resistor.
31	PGOOD	Open collector output that drives low during startup and under any external fault condition. Indicates converter within regulation. Connect external pull-up.
32	VIDSEL	Float this pin for VR11.1 CPU VTT application

SYSTEM THEORY OF OPERATION

PWM Control Method

The PWM block diagram of the *XPhase3*™ architecture is shown in Figure 3. Feed-forward voltage mode control with trailing edge modulation is used. A high-gain wide-bandwidth voltage type error amplifier in the Control IC is used for the voltage control loop. Input voltage is sensed in phase ICs and feed-forward control is realized. The PWM ramp slope will change with the input voltage and automatically compensate for changes in the input voltage. The input voltage can change due to variations in the silver box output voltage or due to the wire and PCB-trace voltage drop related to changes in load current.

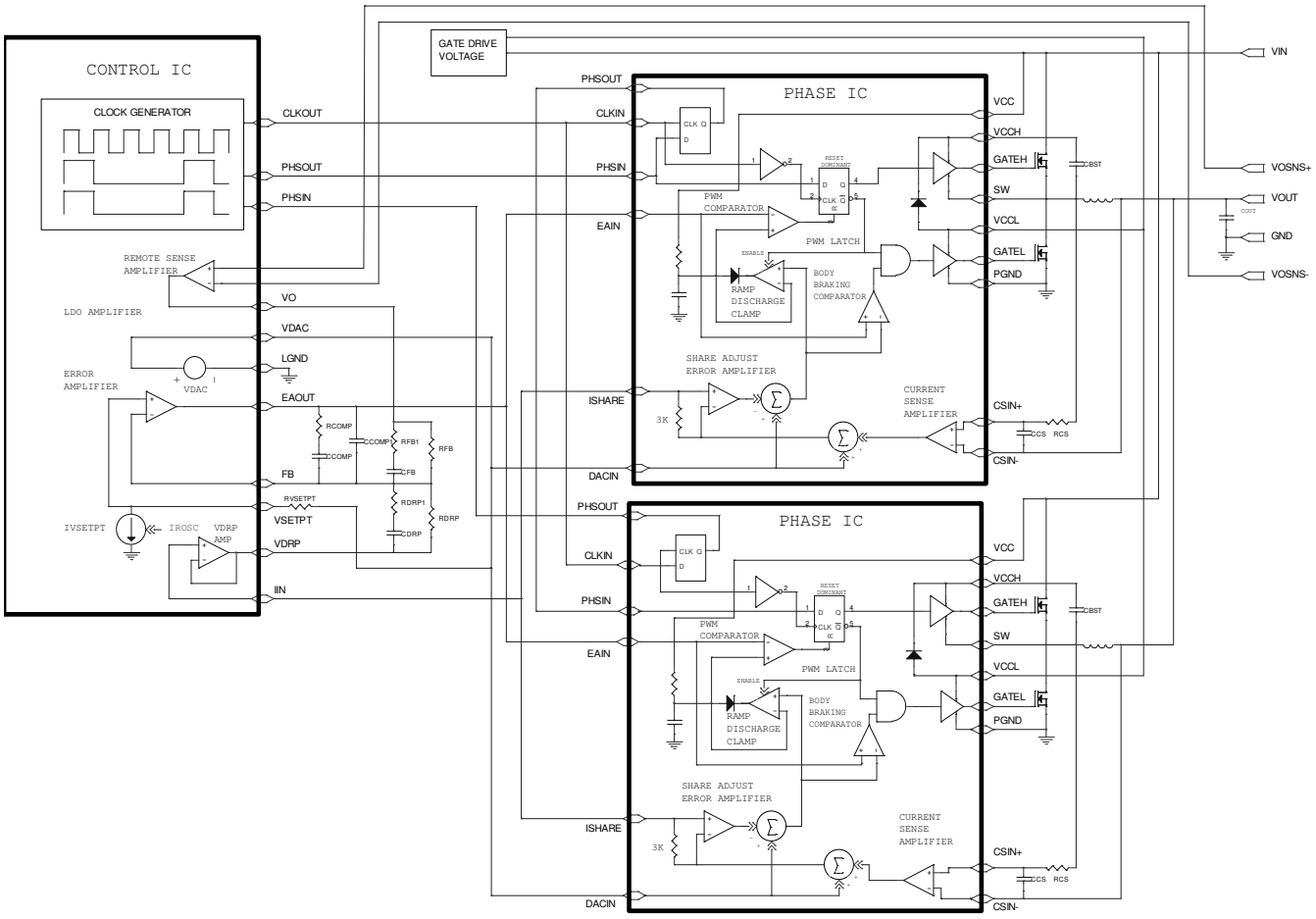


Figure 3 - PWM Block Diagram

Frequency and Phase Timing Control

The oscillator and system clock frequency is programmable from 250kHz to 9MHZ by an external resistor (ROSC). The control IC system clock signal (CLKOUT) is connected to CLKIN of all the phase ICs. The phase timing of the phase ICs is controlled by the daisy chain loop, where control IC phase clock output (PHSOUT) is connected to the phase clock input (PHSIN) of the first phase IC, and PHSOUT of the first phase IC is connected to PHSIN of the second phase IC, etc. and PHSOUT of the last phase IC is connected back to PHSIN of the control IC. During power up, the control IC sends out clock signals from both CLKOUT and PHSOUT pins and detects the feedback at PHSIN pin to determine the phase number and monitor any fault in the daisy chain loop. Figure 4 shows the phase timing for a four phase converter. The switching frequency is programmed by the ROSC resistor as shown in Figure 5. The clock frequency equals the number of phase times the switching frequency.

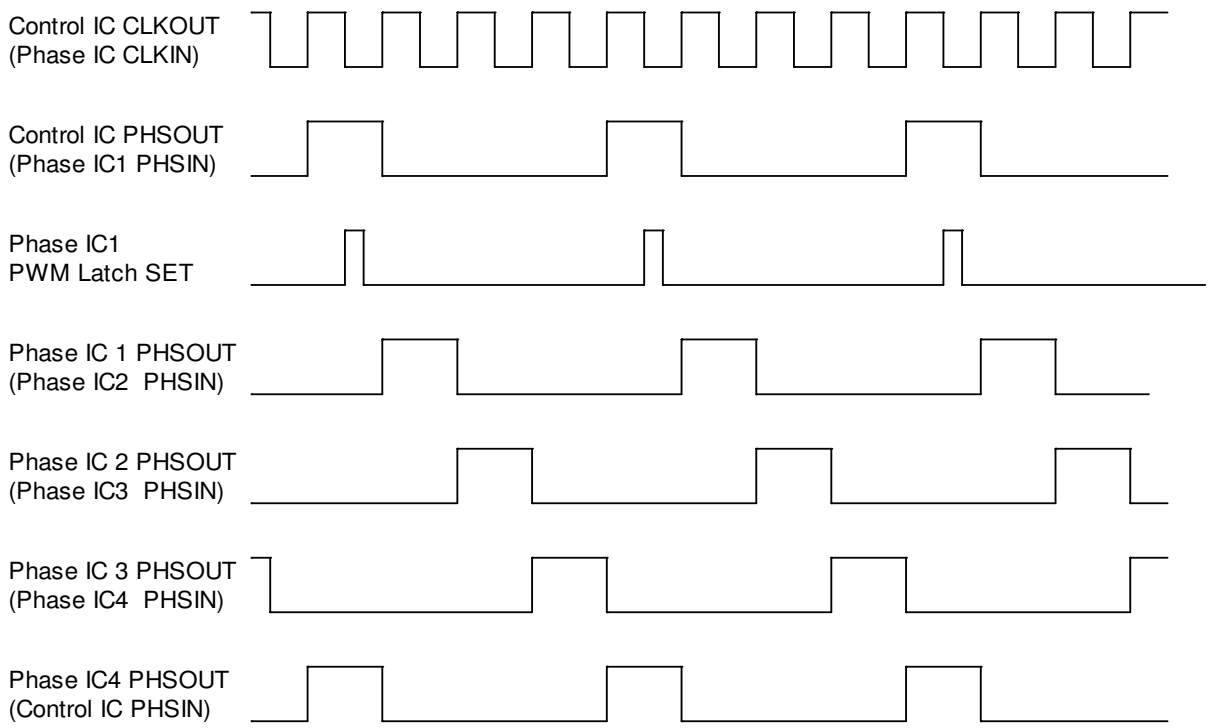


Figure 4 - Four Phase Oscillator Waveforms

PWM Operation

The PWM comparator is located in the phase IC. Upon receiving the falling edge of a clock pulse, the PWM latch is set; the PWM ramp voltage begins to increase; the low side driver is turned off, and the high side driver is then turned on after the non-overlap time. When the PWM ramp voltage exceeds the error amplifier's output voltage the PWM latch is reset. This turns off the high side driver, then turns on the low side driver after the non-overlap time, and activates the ramp discharge clamp. The ramp discharge clamp quickly discharges the PWM ramp capacitor to the output voltage of the share adjust amplifier in the phase IC until the next clock pulse.

The PWM latch is reset dominant allowing all phases to go to zero duty cycle within a few tens of nanoseconds in response to a load step decrease. Phases can overlap and go up to 100% duty cycle in response to a load step increase with turn-on gated by the clock pulses. An error amplifier output voltage greater than the common mode input range of the PWM comparator results in 100% duty cycle regardless of the voltage of the PWM ramp.

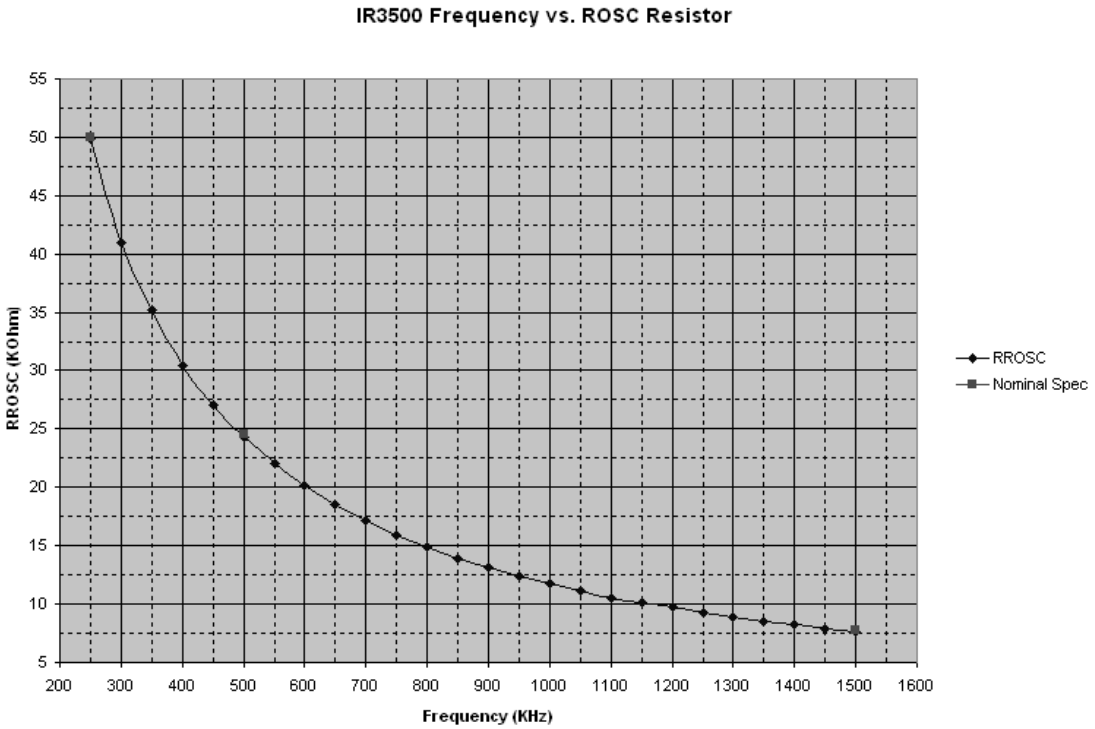


Figure 5 - Frequency variation with ROSC

This arrangement guarantees the error amplifier is always in control and can demand 0 to 100% duty cycle as required. It also favors response to a load step decrease which is appropriate given the low output to input voltage ratio of most systems. The inductor current will increase much more rapidly than decrease in response to load transients. An additional advantage of the architecture is that differences in ground or input voltage at the phases have no effect on operation since the PWM ramps are referenced to VDAC. The error amplifier is a high speed amplifier with 110 dB of open loop gain. It is not unity gain stable. Figure 6 depicts PWM operating waveforms under various conditions.

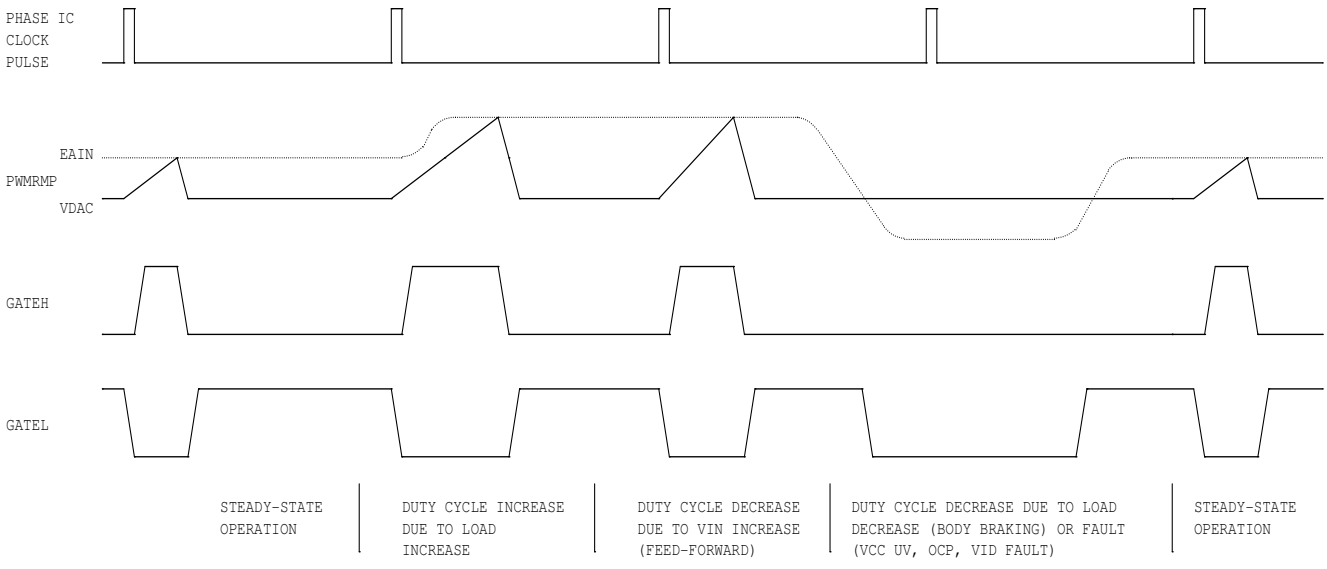


Figure 6 - PWM Operating Waveforms

Body Braking™

In a conventional synchronous buck converter, the minimum time required to reduce the current in the inductor in response to a load step decrease is;

$$T_{SLEW} = \frac{L*(I_{MAX} - I_{MIN})}{V_O}$$

The slew rate of the inductor current can be significantly increased by turning off the synchronous rectifier in response to a load step decrease. The switch node voltage is then forced to decrease until conduction of the synchronous rectifier's body diode occurs. This increases the voltage across the inductor from Vout to Vout + $V_{BODYDIODE}$. The minimum time required to reduce the current in the inductor in response to a load transient decrease is now;

$$T_{SLEW} = \frac{L*(I_{MAX} - I_{MIN})}{V_O + V_{BODYDIODE}}$$

Since the voltage drop in the body diode is often comparable to the output voltage, the inductor current slew rate can be increased significantly. This patented method is referred to as "body braking" and is accomplished through the "body braking comparator" located in the phase IC. If the error amplifier's output voltage drops below the output voltage of the share adjust amplifier in the phase IC, this comparator turns off the low side gate driver.

Lossless Average Inductor Current Sensing

Inductor current can be sensed by connecting a series resistor and a capacitor network in parallel with the inductor and measuring the voltage across the capacitor, as shown in Figure 7. The equation of the sensing network is,

$$v_C(s) = v_L(s)\frac{1}{1+sR_{CS}C_{CS}} = i_L(s)\frac{R_L + sL}{1+sR_{CS}C_{CS}}$$

Usually the resistor Rcs and capacitor Ccs are chosen so that the time constant of Rcs and Ccs equals the time constant of the inductor which is the inductance L over the inductor DCR (RL). If the two time constants match, the voltage across Ccs is proportional to the current through L, and the sense circuit can be treated as if only a sense resistor with the value of RL was used. The mismatch of the time constants does not affect the measurement of inductor DC current, but affects the AC component of the inductor current.

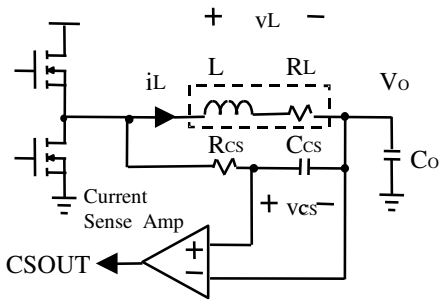


Figure 7 - Inductor Current Sensing and Current Sense Amplifier

The advantage of sensing the inductor current versus high side or low side sensing is that actual output current being delivered to the load is obtained rather than peak or sampled information about the switch currents. The output voltage can be positioned to meet a load line based on real time information. Except for a sense resistor in series with the inductor, this is the only sense method that can support a single cycle transient response. Other methods provide no information during either load increase (low side sensing) or load decrease (high side sensing).

An additional problem associated with peak or valley current mode control for voltage positioning is that they suffer from peak-to-average errors. These errors will show in many ways but one example is the effect of frequency variation. If the frequency of a particular unit is 10% low, the peak to peak inductor current will be 10% larger and the output impedance of the converter will drop by about 10%. Variations in inductance, current sense amplifier bandwidth, PWM prop delay, any added slope compensation, input voltage, and output voltage are all additional sources of peak-to-average errors.

Current Sense Amplifier

A high speed differential current sense amplifier is located in the phase IC, as shown in Figure 7. Its gain is nominally 32.5 and the 3850 ppm/ºC increase in inductor DCR should be compensated in the voltage loop feedback path.

The current sense amplifier can accept positive differential input up to 50mV and negative up to -10mV before clipping. The output of the current sense amplifier is summed with the DAC voltage and sent to the control IC and other phases through an on-chip 3KΩ resistor connected to the ISHARE pin. The ISHARE pins of all the phases are tied together and the voltage on the share bus represents the average current through all the inductors and is used by the control IC for voltage positioning and current limit protection. The input offset of this amplifier is calibrated to +/- 1mV in order to reduce the current sense error.

The input offset voltage is the primary source of error for the current share loop. In order to achieve very small input offset error and superior current sense accuracy, the current sense amplifier continuously calibrates itself. This calibration algorithm creates ripple on the ISHARE bus with a frequency of fsw / 896 in a multiphase architecture.

Average Current Share Loop

Current sharing between phases of the converter is achieved by the average current share loop in each phase IC. The output of the current sense amplifier is compared with average current at the share bus. If current in a phase is smaller than the average current, the share adjust amplifier of the phase will pull down the starting point of the PWM ramp thereby increasing its duty cycle and output current; if current in a phase is larger than the average current, the share adjust amplifier of the phase will pull up the starting point of the PWM ramp thereby decreasing its duty cycle and output current. The current share amplifier is internally compensated so that the crossover frequency of the current share loop is much slower than that of the voltage loop and the two loops do not interact.

IR3500V THEORY OF OPERATION

Block Diagram

The Block diagram of the IR3500V is shown in Figure 8, and specific features are discussed in the following sections.

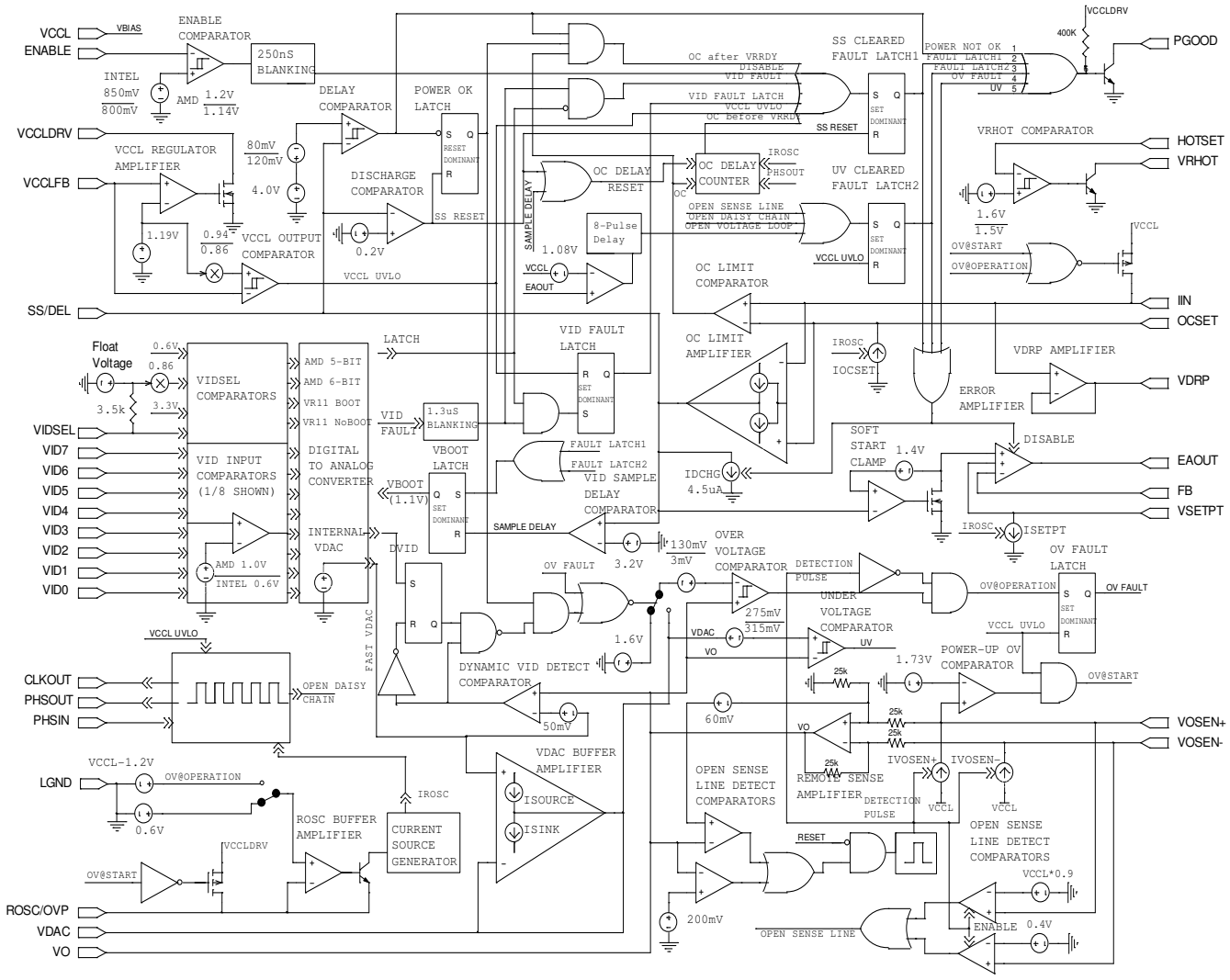


Figure 8 – IR3500V Block Diagram

VID Control

The VID pins require an external bias voltage and should not be floated. The VID input comparators monitor the VID pins and control the Digital-to-Analog Converter (DAC) whose output is sent to the VDAC buffer amplifier. The output of the buffer amplifier is the VDAC pin. The VDAC voltage, input offsets of error amplifier and remote sense differential amplifier are post-package trimmed to provide 0.7% **system set-point** accuracy. The actual VDAC voltage does not directly determine the system accuracy, which has a wider tolerance.

The IR3500V can accept changes in the VID code while operating and vary the DAC voltage accordingly. The slew rate of the voltage at the VDAC pin can be adjusted by an external capacitor between VDAC pin and LGND pin. A resistor connected in series with this capacitor is required to compensate the VDAC buffer amplifier. Digital VID transitions result in a smooth analog transition of the VDAC voltage and converter output voltage minimizing inrush currents in the input and output capacitors and overshoot of the output voltage.

Adaptive Voltage Positioning

Adaptive voltage positioning is implemented needed to reduce the output voltage deviations during load transients and the power dissipation of the load at heavy load. The circuitry related to voltage positioning is shown in Figure 9. The output voltage is set by the reference voltage VSETPT at the positive input to the error amplifier. This reference voltage can be programmed to have a constant DC offset bellow the VDAC by connecting RSETPT between VDAC and VSETPT. The IVSETPT is controlled by the ROSC as shown in Figure 10.

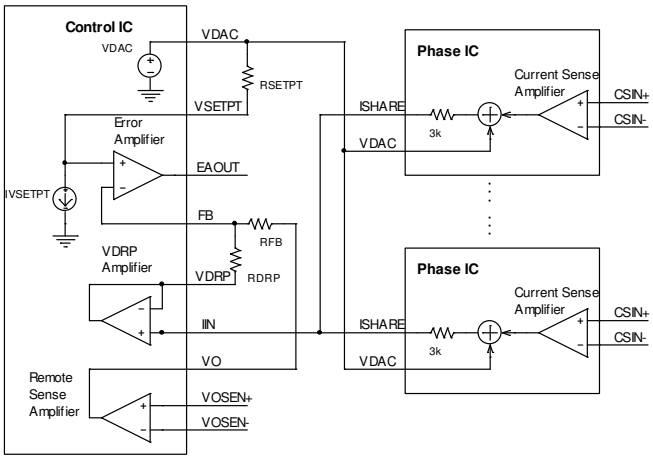


Figure 9 - Adaptive voltage positioning

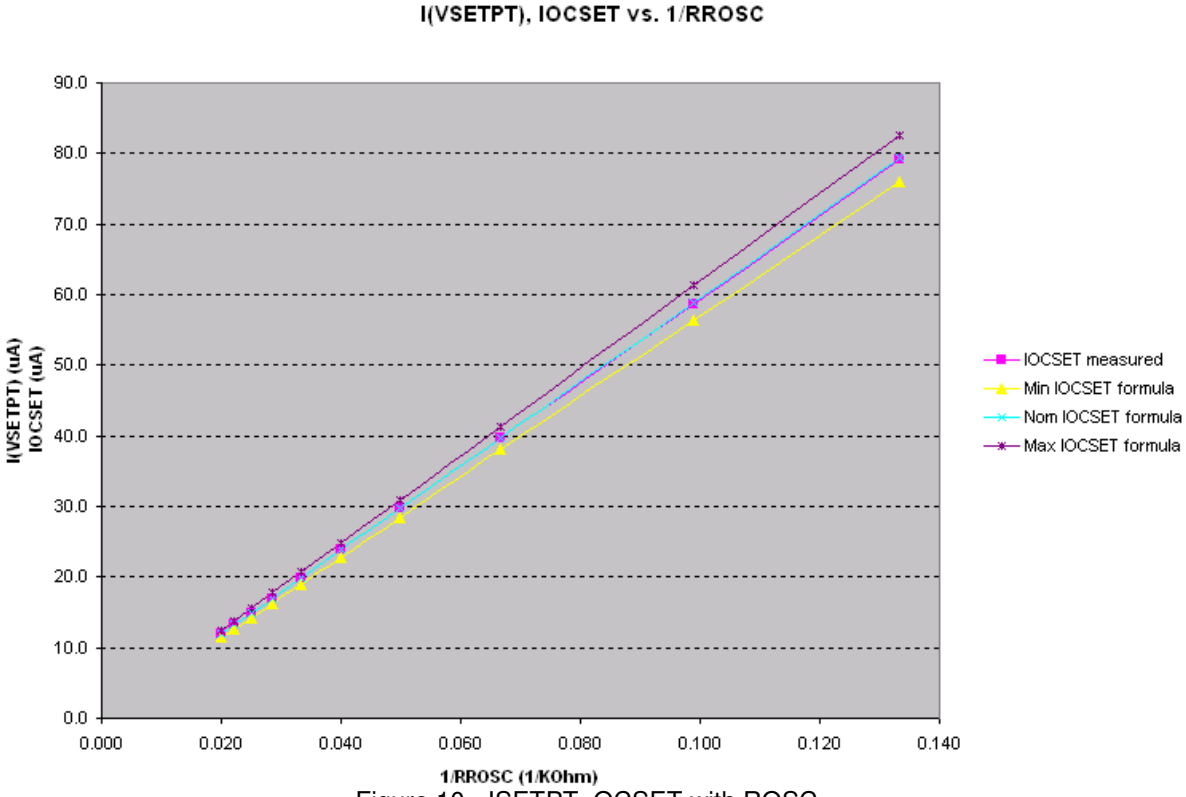


Figure 10 - ISETPT, OCSET with ROSC

The voltage at the VDRP pin is a buffered version of the share bus IIN and represents the sum of the DAC voltage and the average inductor current of all the phases. The VDRP pin is connected to the FB pin through the resistor RDRP. Since the error amplifier will force the loop to maintain FB to be equal to the VSETPT, an additional current will flow into the FB pin equal to (VDRP-VSETPT) / RDRP. When the load current increases, the adaptive positioning voltage increases accordingly. More current flows through the feedback resistor RFB, and makes the output voltage lower proportional to the load current. The positioning voltage can be programmed by the resistor RDRP so that the droop impedance produces the desired converter output impedance. The offset and slope of the converter output impedance are referenced to and therefore independent of the VDAC voltage.

Remote Voltage Sensing

VOSEN+ and VOSEN- are used for remote sensing and connected directly to the load. The remote sense differential amplifier with high speed, low input offset and low input bias current ensures accurate voltage sensing and fast transient response.

Inductor DCR Temperature Compensation

A negative temperature coefficient (NTC) thermistor should be used for inductor DCR temperature compensation. The thermistor should be placed close to the inductor and connected in parallel with the feedback resistor, as shown in Figure 11. The resistor in series with the thermistor is used to reduce the nonlinearity of the thermistor.

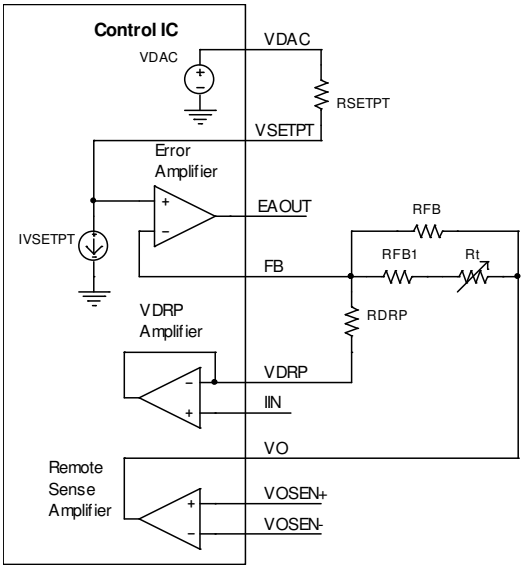


Figure 11 - Temperature compensation of inductor DCR

Start-up Sequence

The IR3500V has a programmable soft-start function to limit the surge current during the converter start-up. A capacitor connected between the SS/DEL and LGND pins controls soft start timing, over-current protection delay and hiccup mode timing. A charge current of 52.5uA and discharge current of 4uA control the up slope and down slope of the voltage at the SS/DEL pin respectively.

Figure 12 depicts the start-up sequence VR11 VID with boot voltage. If there is no fault, the SS/DEL pin will start charging when the enable crosses the threshold. The error amplifier output EAOUT is clamped low until SS/DEL reaches 1.4V. The error amplifier will then regulate the converter's output voltage to match the SS/DEL voltage less the 1.4V offset until the converter output reaches the 1.1V boot voltage. The SS/DEL voltage continues to increase until it rises above the 3.0V threshold of VID delay comparator. The VID set inputs are then activated and VDAC pin transitions to the level determined by the VID inputs. The SS/DEL voltage continues to increase until it rises above 3.92V and allows the PGOOD signal to be asserted. SS/DEL finally settles at 4.0V, indicating the end of the soft start.

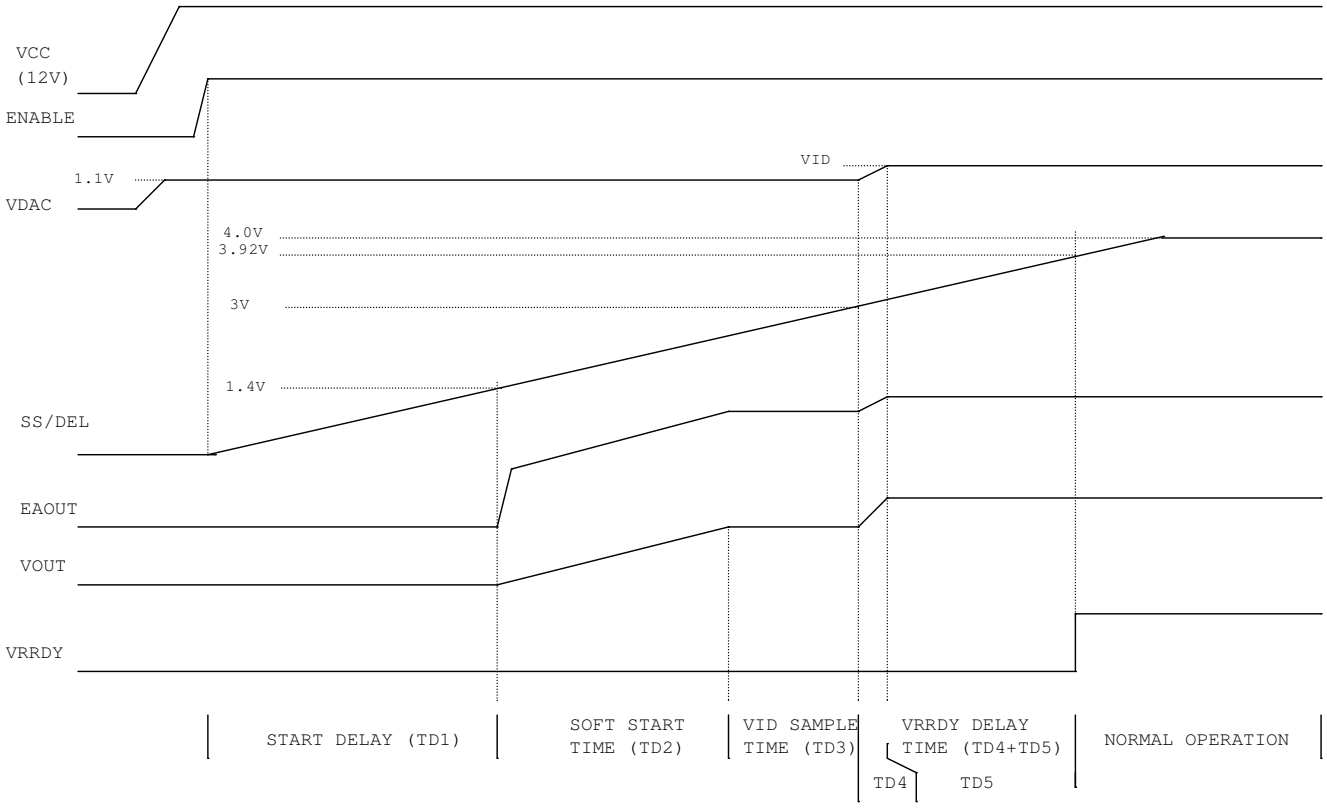


Figure 12 - Start-up sequence

VCCL under voltage lock-out, VID fault modes, over current, as well as a low signal on the ENABLE input immediately sets the fault latch, which causes the EAOUT pin to drive low turning off the phase IC drivers. The PGOOD pin also drives low, and SS/DEL begin to discharge until the voltage reaches 0.2V. If the fault has cleared the fault latch will be reset by the discharge comparator allowing a normal soft start to occur.

Other fault conditions, such as over voltage, open sense lines, open loop monitor, and open daisy chain, set different fault latches, which start discharging SS/DEL, pull down EAOUT voltage and drive PGOOD low. However, the latches can only be reset by cycling VCCL power.

Constant Over-Current Control during Soft Start

The over current limit threshold is set by a resistor connected between OCSET and VDAC. If the IIN pin voltage, which is proportional to the average current plus VDAC voltage, exceeds the OCSET voltage during soft start, the constant over-current control is activated. Figure 13 shows the constant over-current control with delay during soft start. The delay time is set by the ROSC resistor, which sets the number of switching cycles for the delay counter.

The delay is required since over-current conditions can occur as part of normal operation due to inrush current. If an over-current occurs during soft start (before PGOOD is asserted), the SS/DEL voltage is regulated by the over current amplifier to limit the output current below the threshold set by OCSET voltage. If the over-current condition persists after delay time is reached, the fault latch will be set pulling the error amplifier's output low and inhibiting switching in the phase ICs. The SS/DEL capacitor will discharge until it reaches 0.2V and the fault latch is reset allowing a normal soft start to occur. If an over-current condition is again encountered during the soft start cycle, the constant over-current control actions will repeat and the converter will be in hiccup mode. The delay time is controlled by a counter which is triggered by clock. The counter values vary with switching frequency per phase in order to have a similar delay time for different switching frequencies.

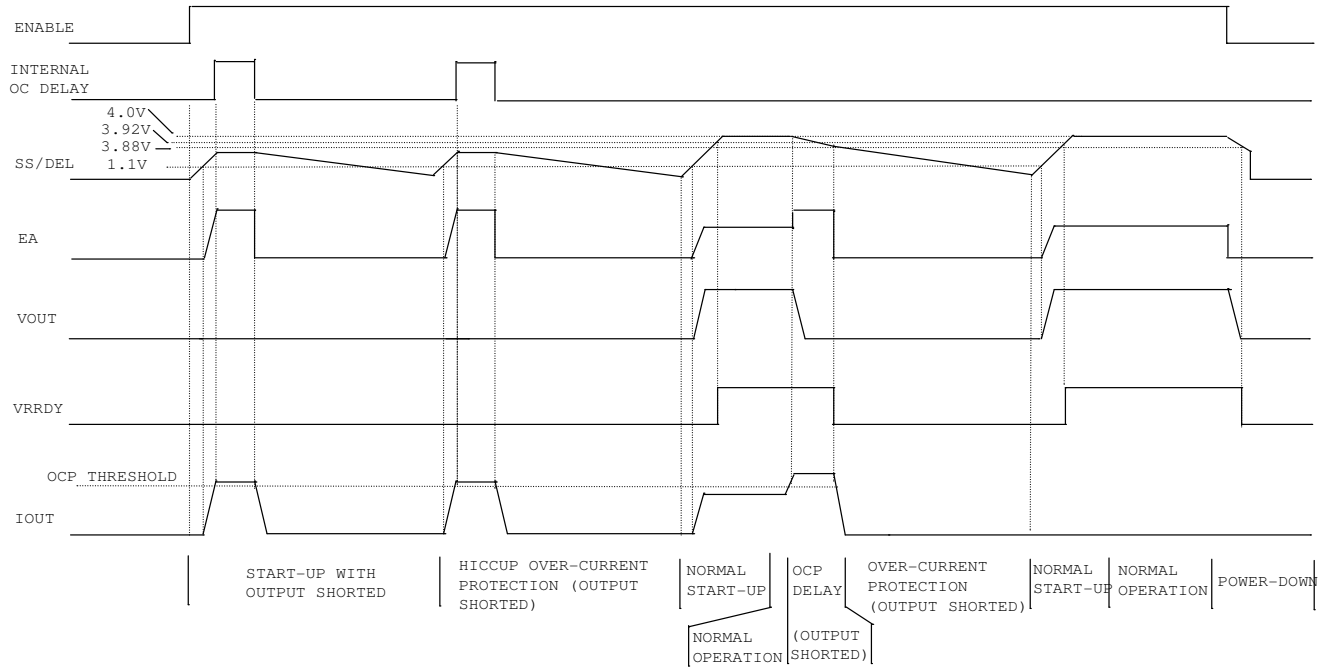


Figure 13 - Over Current Protection waveforms during and after soft start

Over-Current Hiccup Protection after Soft Start

The over current limit threshold is set by a resistor connected between OCSET and VDAC pins. Figure 13 shows the constant over-current control with delay after PGOOD is asserted. The delay is required since over-current conditions can occur as part of normal operation due to load transients or VID transitions.

If the IIN pin voltage, which is proportional to the average current plus VDAC voltage, exceeds the OCSET voltage after PGOOD is asserted, it will initiate the discharge of the capacitor at SS/DEL. The magnitude of the discharge current is proportional to the voltage difference between IIN and OCSET and has a maximum nominal value of 55uA. If the over-current condition persists long enough for the SS/DEL capacitor to discharge below the 120mV offset of the delay comparator, the fault latch will be set pulling the error amplifier's output low and inhibiting switching in the phase ICs and de-asserting the PGOOD signal. The output current is not controlled during the delay time. The SS/DEL capacitor will discharge until it reaches 200 mV and the fault latch is reset allowing a normal soft start to occur. If an over-current condition is again encountered during the soft start cycle, the over-current action will repeat and the converter will be in hiccup mode.

Linear Regulator Output (VCCL)

The IR3500V has a built-in linear regulator controller, and only an external NPN transistor is needed to create a linear regulator. The output voltage of the linear regulator can be programmed between 4.75V and 7.5V by the resistor divider at VCCLFB pin. The regulator output powers the gate drivers and other circuits of the phase ICs along with circuits in the control IC, and the voltage is usually programmed to optimize the converter efficiency. The linear regulator can be compensated by a 4.7uF capacitor at the VCCL pin. Due to stability reasons, there is an upper limit to the maximum value of capacitor that can be used at this pin and it's a function of the number of phases used in the multiphase architecture and their switching frequency. Figure 14 provides Bode plots for the linear regulator with 5 phases switching at 750 kHz.

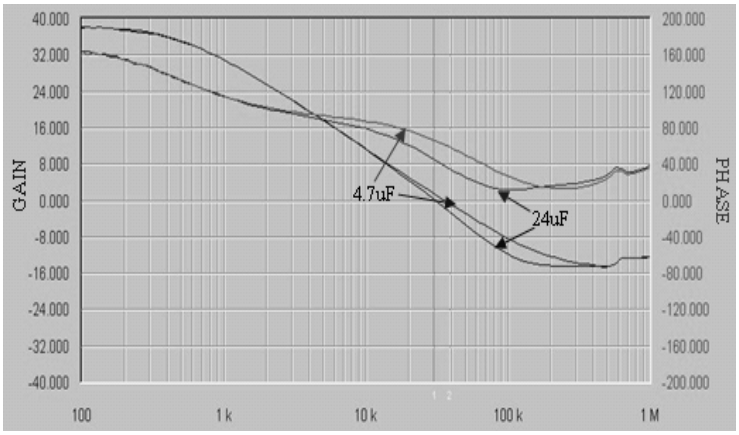


Figure 14 - VCCL regulator stability with 5 phases and PHSOUT equals 750 kHz.

VCCL Under Voltage Lockout (UVLO)

The IR3500V has no under voltage lockout for converter input voltage (VCC), but monitors the VCCL voltage instead, which is used for the gate drivers of phase ICs and circuits in control IC and phase ICs. During power up, the fault latch will be reset if VCCL is above 94% of the voltage set by resistor divider at VCCLFB pin. If VCCL voltage drops below 86% of the set value, the fault latch will be set.

VID Fault Codes

VID codes of 0000000X and 1111111X will set the fault latch and disable the error amplifier. A 1.3us delay is provided to prevent a fault condition from occurring during Dynamic VID changes. A VID FAULT condition is latched and can only be cleared by cycling power to VCCL.

Voltage Regulator Ready (PGOOD)

The PGOOD pin is an open-collector output and should be pulled up to a voltage source through a resistor. During start-up, it is pulled low with an input voltage as low as 2 V. Until the soft start cycle is complete, PGOOD remains low until the output voltage is within regulation and SS/DEL is above 3.92V. The PGOOD pin drives low if the fault latch, over voltage latch, open sense line latch, or open daisy chain latch is set. A high level at the PGOOD pin indicates that the converter is in operation and has no fault. The PGOOD stays high as long as the output voltage is within 300 mV of the programmed VID.

Open Voltage Loop Detection

The output voltage range of error amplifier is detected all the time to ensure the voltage loop is in regulation. If any fault condition forces the error amplifier output above VCCL-1.08V for 8 switching cycles, the fault latch is set. The fault latch can only be cleared by cycling power to VCCL.

Load Current Indicator Output

The VDRP pin voltage represents the average current of the converter plus the VDAC voltage. The load current information can be retrieved by a differential amplifier that subtracts the VDAC voltage from the VDRP voltage.

Enable Input

Pulling the ENABLE pin below 0.8V sets the Fault Latch and a voltage above 0.85V enables the soft start of the converter.

Thermal Monitoring (VRHOT)

A resistor divider including a thermistor at the HOTSET pin sets the VRHOT threshold. The thermistor is usually placed at the temperature sensitive region of the converter, and is linearized by a series resistor. The IR3500V compares the HOTSET pin voltage with a reference voltage of 1.6V. The VRHOT pin is an open-collector output and should be pulled up to a voltage source through a resistor. If the thermal trip point is reached the VRHOT output drives low. The hysteresis of the VRHOT comparator is added to eliminate toggling of VRHOT output.

Over Voltage Protection (OVP)

The output over-voltage happens during normal operation if a high side MOSFET short occurs or if output voltage is out of regulation. The over-voltage protection comparator monitors the output of the remote sense amplifier (Vo pin). If the Vo pin voltage exceeds VDAC by 130mV, as shown in Figure 15, the IR3500V raises the ROSC/OVP pin voltage to V(VCCL) - 1V. This signal can be used by the host system as an indication that an over voltage event has occurred enabling an appropriate response such as disabling the AC-DC converter. The ROSC/OVP pin can also be connected to a thyrister in a crowbar circuit to blow an input fuse.

The over voltage condition also sets the over voltage fault latch, which pulls the error amplifier output low to turn off the converter output. At the same time the IIN pin (ISHARE of phase ICs) is pulled up to VCCL to communicate the over voltage condition to phase ICs, as shown in Figure 15. In each phase IC, an OVP circuit overrides the normal PWM operation and will fully turn-on the low side MOSFET within approximately 150ns. The low side MOSFET will remain on until the ISHARE pin voltage drops below V(VCCL) - 800mV, which signals the end of over voltage condition. An over voltage fault condition is latched in the IR3500V and can only be cleared by cycling power to the IR3500V VCCL.

In the event of a high side MOSFET short before power up, the OVP flag is activated with as little supply voltage as possible, as shown in Figure 16. The VOSEN+ pin is compared against a fixed voltage of 1.73V (typical) for OVP conditions at power-up. The ROSC/OVP pin will be pulled higher than 1.6V with VCCLDRV voltage as low as 1.8V. An external MOSFET or comparator should be used to disable the silver box, activate a crowbar, or turn off the supply source. The 1.8V threshold is used to prevent false over-voltage triggering caused by pre-charging of output capacitors.

Pre-charging of converter output voltage may trigger OVP. If the converter output is pre-charged above 1.73V as shown in Figure 17, the ROSC/OVP pin voltage will be higher than 1.6V when VCCLDRV voltage reaches 1.8V. ROSC/OVP pin voltage will be VCCLDRV-1V and rise with VCCLDRV voltage until VCCL is above UVLO threshold, after which ROSC/OVP pin voltage will be VCCL-1V. The converter cannot start unless the over voltage condition stops and VCCL is cycled. If the converter output is pre-charged 130mV above VDAC but lower than 1.73V, as shown in Figure 18, the converter will soft start until SS/DEL voltage is above 3.92V (4.0V-0.08V). Then, the over voltage comparator is activated and fault latch is set.

During dynamic VID down, OVP could be triggered when output voltage can not follow VDAC voltage change at light load with large output capacitance. Therefore, the over-voltage threshold is raised to 1.73V from VDAC+130mV whenever dynamic VID is detected and the difference between output voltage and VDAC is more than 50mV, as shown in Figure 19. The over-voltage threshold is changed back to VDAC+130mV if the difference is smaller than 50mV.

The overall system must be considered when designing for OVP. In many cases the over-current protection of the AC-DC or DC-DC converter supplying the multiphase converter will be triggered and provide effective protection without damage as long as all PCB traces and components are sized to handle the worst-case maximum current. If this is not possible, a fuse can be added in the input supply to the multiphase converter.

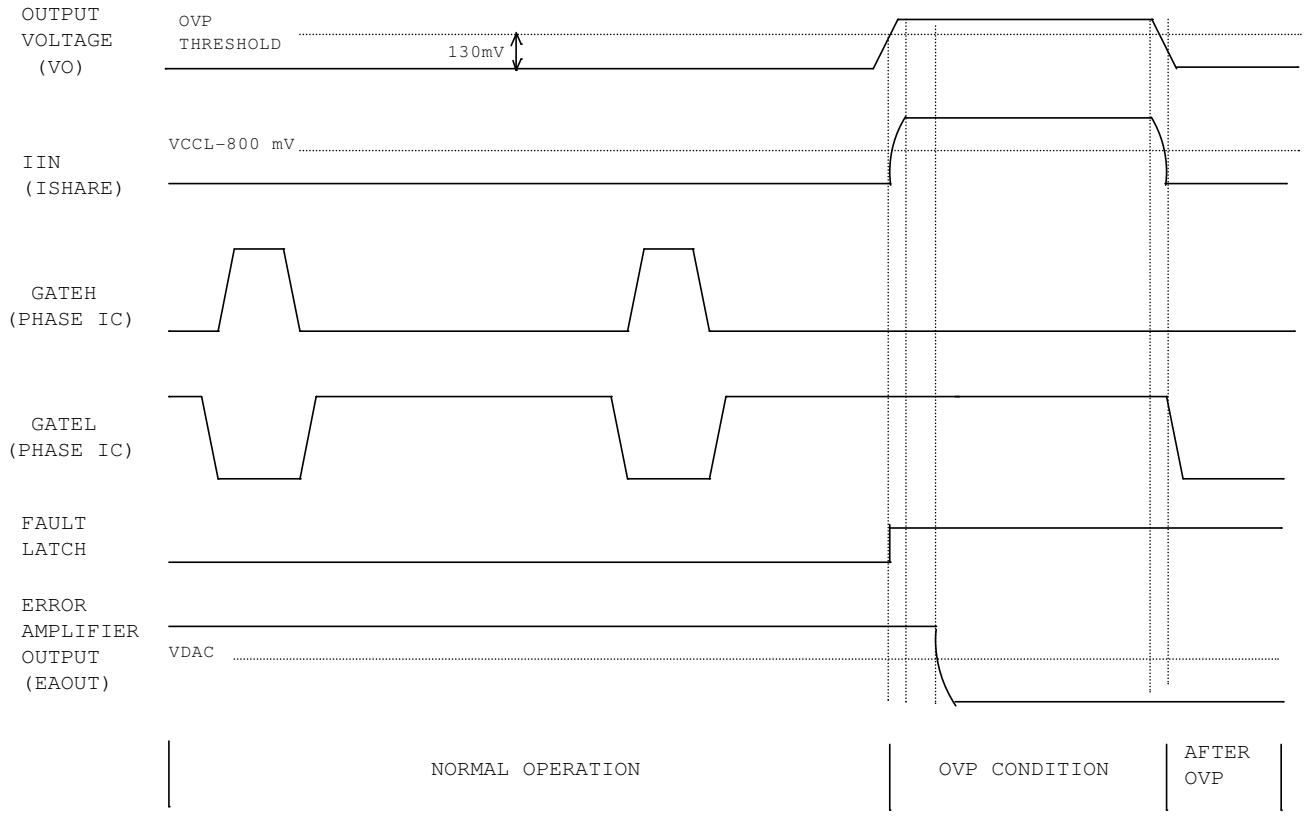


Figure 15 - Over-voltage protection during normal operation

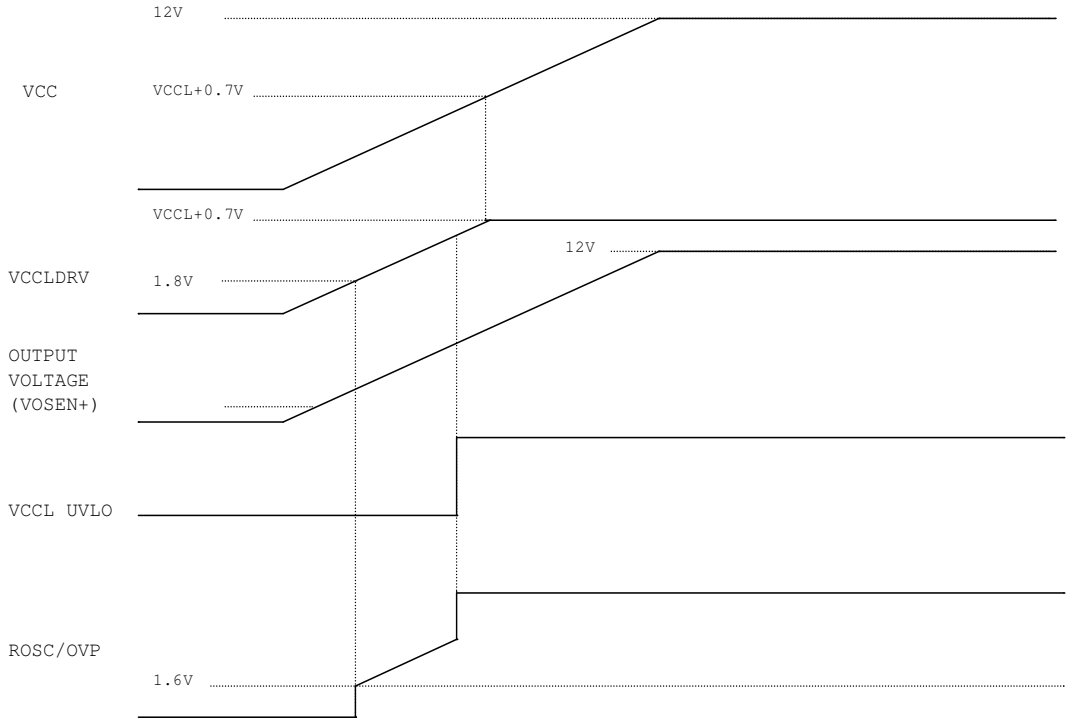


Figure 16 - Over-voltage protection during power-up

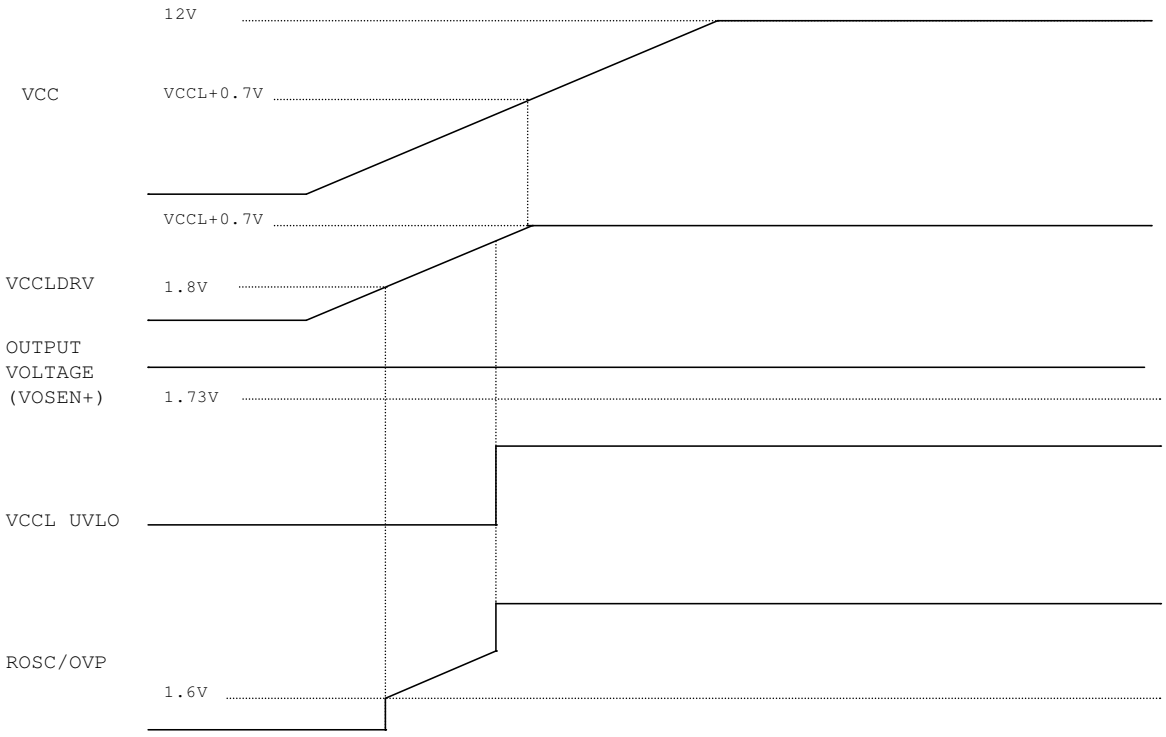


Figure 17 - Over-voltage protection with pre-charging converter output Vo > 1.73V

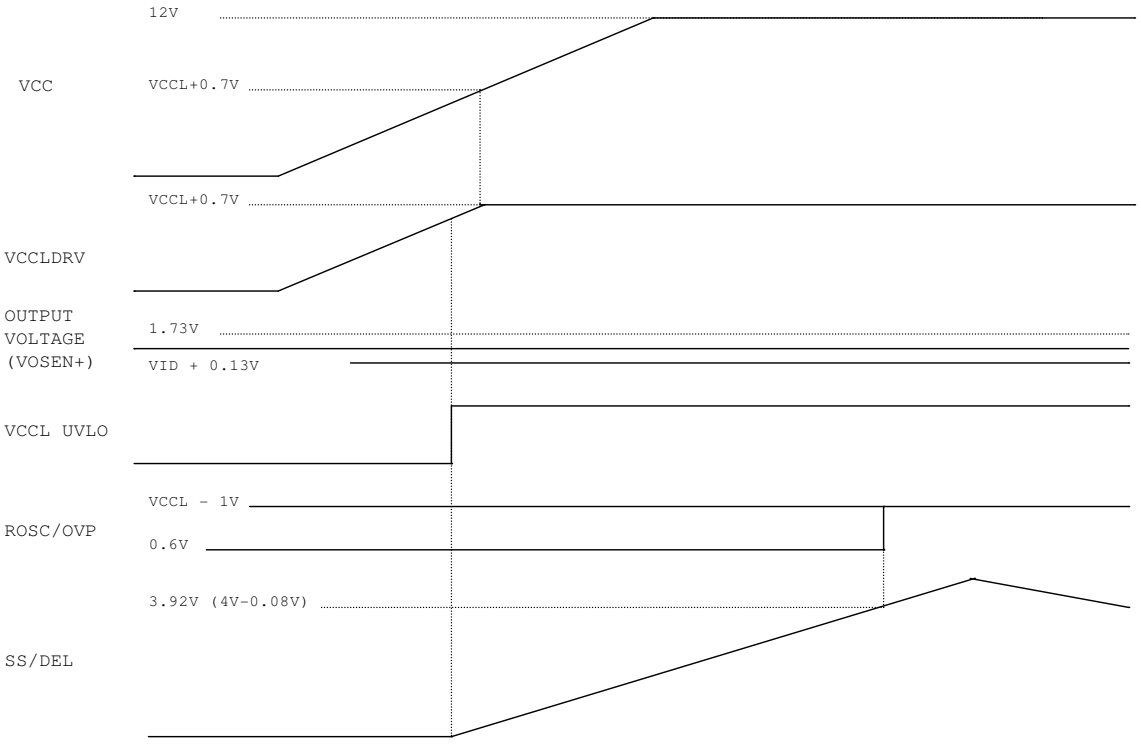


Figure 18 - Over-voltage protection with pre-charging converter output VID + 0.13V <Vo < 1.73V

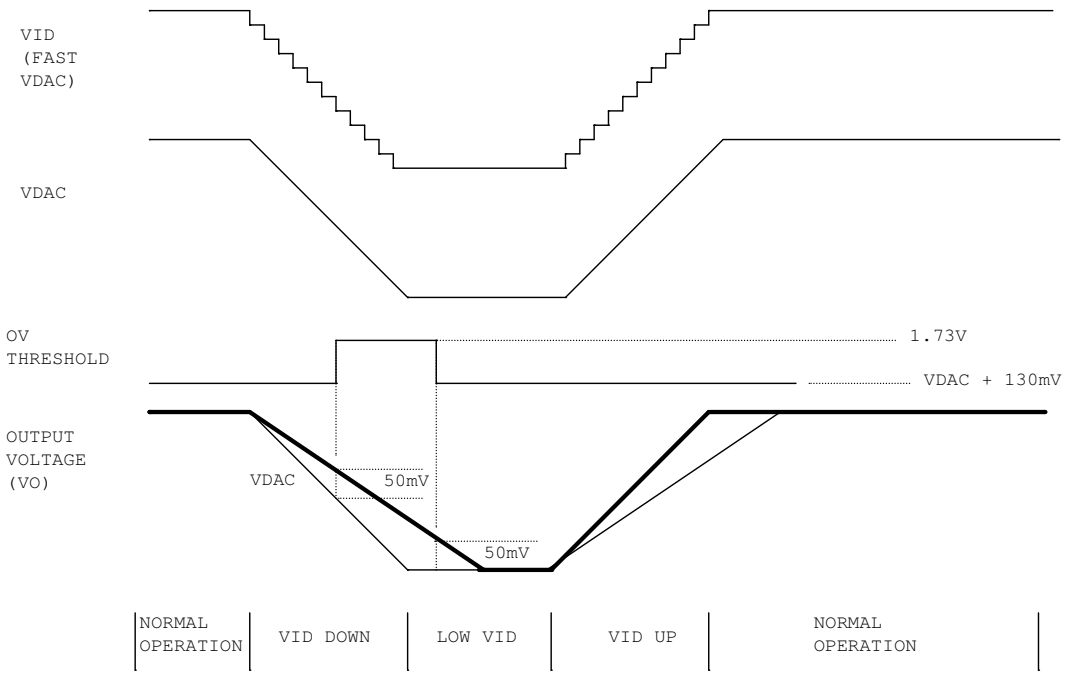


Figure 19 - Over-voltage protection during dynamic VID

Open Remote Sense Line Protection

If either remote sense line VOSEN+ or VOSEN- or both are open, the output of remote sense amplifier (VO) drops. The IR3500V monitors VO pin voltage continuously. If VO voltage is lower than 200 mV, two separate pulse currents are applied to VOSEN+ and VOSEN- pins respectively to check if the sense lines are open. If VOSEN+ is open, a voltage higher than 90% of V(VCCL) will be present at VOSEN+ pin and the output of open line detect comparator will be high. If VOSEN- is open, a voltage higher than 700mV will be present at VOSEN- pin and the output of open-line-detect comparator will be high. The open sense line fault latch is set, which pulls the error amplifier output low immediately and shut down the converter. The SS/DEL voltage is discharged and the fault latch can only be reset by cycling VCCL power.

Open Daisy Chain Protection

IR3500V checks the daisy chain every time it powers up. It starts a daisy chain pulse on the PHSOUT pin and detects the feedback at PHSIN pin. If no pulse comes back after 32 CLKOUT pulses, the pulse is restarted again. If the pulse fails to come back the second time, the open daisy chain fault is registered, and SS/DEL is not allowed to charge. The fault latch can only be reset by cycling the power to VCCL.

After powering up, the IR3500V monitors PHSIN pin for a phase input pulse equal or less than the number of phases detected. If PHSIN pulse does not return within the number of phases in the converter, another pulse is started on PHSOUT pin. If the second started PHSOUT pulse does not return on PHSIN, an open daisy chain fault is registered.

Phase Number Determination

After a daisy chain pulse is started, the IR3500V checks the timing of the input pulse at PHSIN pin to determine the phase number. This information is used to have symmetrical phase delay between phase switching without the need of any external component.

Single Phase Operation

In an architecture where only a single phase is needed the switching frequency is determined by the clock frequency.

Fault Operation Table

The Fault Table shown in figure 20 describes the different faults that can occur and how IR3500V will react to protect the supply and the load from possible damage. The fault types that can occur are listed in row 1. Row 2 has the method that a fault is cleared. The first 5 faults are latched in the UV fault latch and the VCCL power has to be recycled by switching off the input and switching it back on for the converter to work again. The rest of the faults (except for UVLO Vout) are latched in the SS fault latch and do not require the VCCL power to be recycled in order to resume normal operation once the fault condition clears. Most of the faults disable the error amplifier (EA) and discharge the soft start capacitor. All the faults flag PGOOD. PGOOD returns back to high when the faults are cleared. The delay row shows reaction time after detecting a fault condition. Delays are provided to minimize the possibility of nuisance faults.

	Fault Type									
	Open Daisy	**Open Control Loop**	**Open Sense Line**	**Over Voltage**	**VID**	**Disable**	**VCCL UVLO**	**OC Before Start-up**	**OC After Start-up**	**VOUT UVLO**
Fault Clearing Method	Recycle VCCL					Resume Normal Operation when Condition Clears				
Error Amp Disabled	Yes									No
ROSC/OVP & IIN drive high until OV clears	No			Yes	No					
SS/DEL Discharge	Yes									No
Flags PGood	Yes									
Delay?	32 Clock Pulses	8 PHSOUT Pulses	No	No	1.3us Blank Time	250 ns Blank Time	No	PHSOUT Pulses. Count Programmed by ROSC value	SS/DEL Discharge Threshold	No

Figure 20 – Fault Table

APPLICATIONS INFORMATION

DESIGN PROCEDURE

Oscillator Resistor *Rosc*

The oscillator of IR500 generates square-wave pulses to synchronize the phase ICs. The switching frequency of each phase converter equals the PHSOUT frequency, which is set by the external resistor ROSC according to the curve in Figure 23. The CLKOUT frequency equals the switching frequency multiplied by the phase number. The Rosc sets the reference current used for the no load offset and OCSET which is given by Figure 5 and equals:

$$ISETPT = IOCSET = \frac{0.595}{Rosc} \qquad (1)$$

Soft Start Capacitor *CSS/DEL*

The soft start capacitor CSS/DEL programs five different time parameters. They include soft start delay time, soft start time, VID sample delay time, VR ready delay time and over-current fault latch delay time after VR ready.

The SS/DEL pin voltage controls the slew rate of the converter output voltage, as shown in Figure 12. After the ENABLE pin voltage rises above 0.85V, there is a soft-start delay time TD1, after which the error amplifier output is released to allow the soft start of output voltage. The soft start time TD2 represents the time during which converter voltage rises from zero to 1.1V. The VID sample delay time (TD3) is the time period when VID stays at boot voltage of 1.1V. VID rise or fall time (TD4) is the time when VID changes from boot voltage to the final voltage. The VR ready delay time (TD5) is the time period from VR reaching the final voltage to the VR ready signal being issued, which is determined by the delay comparator threshold.
CSS/DEL = 0.1uF meets all the specifications of TD1 to TD5, which are determined by (2) to (6) respectively.

$$TD1 = \frac{C_{SS/DEL} * 1.4}{I_{CHG}} = \frac{C_{SS/DEL} * 1.4}{52.5 * 10^{-6}} \qquad (2)$$

$$TD2 = \frac{C_{SS/DEL} * 1.1}{I_{CHG}} = \frac{C_{SS/DEL} * 1.1}{52.5 * 10^{-6}} \quad (3)$$

$$TD3 = \frac{C_{SS/DEL} * (3 - 1.4 - 1.1)}{I_{CHG}} = \frac{C_{SS/DEL} * 0.7}{52.5 * 10^{-6}} \quad (4)$$

$$TD4 = \frac{C_{SS/DEL} * |V_{DAC} - 1.1|}{I_{CHG}} = \frac{C_{SS/DEL} * |V_{DAC} - 1.1|}{52.5 * 10^{-6}} \quad (5)$$

$$TD5 = \frac{C_{SS/DEL} * (3.92 - 3)}{I_{CHG}} - TD4 = \frac{C_{SS/DEL} * 0.92}{52.5 * 10^{-6}} - TD4 \quad (6)$$

The minimum over-current fault latch delay time t_{OCDEL} is determined by the value of $C_{SS/DEL}$ and can be quantified as

$$t_{OCDEL} = \frac{C_{SS/DEL} * 0.12}{I_{DISCHG}} = \frac{C_{SS/DEL} * 0.12}{55 * 10^{-6}} \quad (7)$$

VDAC Slew Rate Programming Capacitor *CVDAC* and Resistor *RVDAC*

The slew rate of VDAC down-slope SR_{DOWN} can be programmed by the external capacitor C_{VDAC} as defined in (8), where I_{SINK} is the sink current of VDAC pin. The slew rate of VDAC up-slope is the same as that of down-slope.

$$C_{VDAC} = \frac{I_{SINK}}{SR_{DOWN}} = \frac{44 * 10^{-6}}{SR_{DOWN}} \quad (8)$$

The resistor R_{VDAC} is used to compensate VDAC circuit and can be calculated as follows

$$R_{VDAC} = 0.5 + \frac{3.2 * 10^{-15}}{C_{VDAC}^{\ 2}} \quad (9)$$

Over Current Setting Resistor *ROCSET*

The inductor DC resistance is utilized to sense the inductor current. The copper wire of inductor has a constant temperature coefficient of 3850 ppm/℃, and therefore the maximum inductor DCR can be calculated from (10), where R_{L_MAX} and R_{L_ROOM} are the inductor DCR at maximum temperature T_{L_MAX} and room temperature $T_{\_ROOM}$ respectively.

$$R_{L\_MAX} = R_{L\_ROOM} * [1 + 3850 * 10^{-6} * (T_{L\_MAX} - T_{ROOM})] \quad (10)$$

The total input offset voltage (V_{CS_TOFST}) of current sense amplifier in phase ICs is the sum of input offset (V_{CS_OFST}) of the amplifier itself and that created by the amplifier input bias current flowing through the current sense resistor R_{CS}.

$$V_{CS\_TOFST} = V_{CS\_OFST} + I_{CSIN+} * R_{CS} \quad (11)$$

The over-current limit is set by the external resistor R_{OCSET} and is given by (12). In a multiphase architecture the peak to peak ripple of the net inductor current is much smaller than the stand alone phase due to interleaving. The ratio of the peak to average current in this case can be approximated using (13).

$$R_{OCSET} = [\frac{I_{LIMIT}}{n} * R_{L\_MAX} * (1 + K_P) + V_{CS\_TOFST}] * G_{CS} / I_{OCSET} \quad (12)$$

$$K_P = \frac{\left[V_I \cdot D \cdot (1-D) \cdot n \cdot (D - \frac{m}{n}) \cdot (\frac{m+1}{n} - D)\right]}{(I_{LIMIT}/n) \cdot L \cdot f_{sw} \cdot 2 \cdot D \cdot (1-D)} \quad (13)$$

Where; I_{LIMIT}=Over current limit, n=Number of phases, K_P=Ratio of the peak to average current for the inductor, G_{CS}=Gain of the current sense amplifier, I_{OCSET}= Determined by the ROSC and given by Figure 10, D=Vo/V_I, m=Maximum integer that doesn't exceed (n*D)

No Load Output Voltage Setting Resistor *RVSETPT*,

A resistor between VSETPT pin and VDAC is used to create output voltage offset V_{O_NLOFST}, which is the difference between V_{DAC} voltage and output voltage at no load condition. R_{VSETPT} is determined by (14), where I_{VSETPT} is the current flowing out of VSETPT pin as shown in Figure 23.

$$R_{VSETPT} = \frac{V_{O\_NLOFST}}{I_{VSETPT}} \quad (14)$$

VCCL Capacitor *CVCCL*

The capacitor is selected based on the stability requirement of the linear regulator and the load current to be driven. The linear regulator supplies the bias and gate drive current of the phase ICs. A 4.7uF normally ensures stable VCCL performance.

VCCL Programming Resistor *RVCCLFB1* and *RVCCLFB2*

Since VCCL voltage is proportional to the MOSFET gate driver loss and inversely proportional to the MOSFET conduction loss, the optimum voltage should be chosen to maximize the converter efficiency. VCCL linear regulator consists of an external NPN transistor, a ceramic capacitor and a programmable resistor divider. Pre-select $R_{VCCLFB1}$, and calculate $R_{VCCLFB2}$ from (15).

$$R_{VCCLFB2} = \frac{R_{VCCLFB1} * 1.19}{VCCL - 1.19} \quad (15)$$

VCCL Regulator Drive Resistor *RVCCLDRV*

The drive resistor is primarily dependent on the load current requirement of the linear regulator and the minimum input voltage requirements. The following equation gives an estimate of the average load current of the switching phase ICs.

$$I_{drive\_avg} = \left[(Q_{gb} + Q_{gt}) \cdot f_{sw} + 10mA\right] \cdot n \quad (16)$$

Q_{gb} and Q_{gt} are the gate charge of the top and bottom FET. For a minimum input voltage and a maximum VCCL, the maximum $R_{VCCLDRV}$ required to use the full pull-down current of the VCCL driver is given by

$$R_{VCCLDRV} = \frac{V_I(\min) - 0.7 - VCCL(\max)}{I_{drive\_avg} / \beta_{\min}} \quad (17)$$

Due to limited pull down capability of the VCCLDRV pin, make sure the following condition is satisfied.

$$\frac{V_I(\max) - 0.7 - VCCL(\min)}{R_{VCCLDRV}} < 10mA \qquad (18)$$

In the above equation, V_I(min) and V_I(max) is the minimum and maximum anticipated input voltage. If the above condition is not satisfied there is a need to use a device with higher β_{min} or Darlington configuration can be used instead of a single NPN transistor.

Thermistor *RTHERM* and Over Temperature Setting Resistors *RHOTSET1* and *RHOTSET2*

The threshold voltage of VRHOT comparator is fixed at 1.6V, and a negative temperature coefficient (NTC) thermistor RTHERM is required to sense the temperature of the power stage. If we pre-select RTHERM, the NTC thermistor resistance at allowed maximum temperature TMAX is calculated from (19).

$$R_{TMAX} = R_{THERM} * EXP[B_{THERM} * (\frac{1}{T_{L\_MAX}} - \frac{1}{T_{\_ROOM}})] \qquad (19)$$

Select the series resistor RHOTSET2 to linearize the NTC thermistor, which has non-linear characteristics in the operational temperature range. Then calculate RHOTSET1 corresponding to the allowed maximum temperature TMAX from (20).

$$R_{HOTSET1} = \frac{(R_{TMAX} + R_{HOTSET2}) * (VCCL - 1.6)}{1.6} \qquad (20)$$

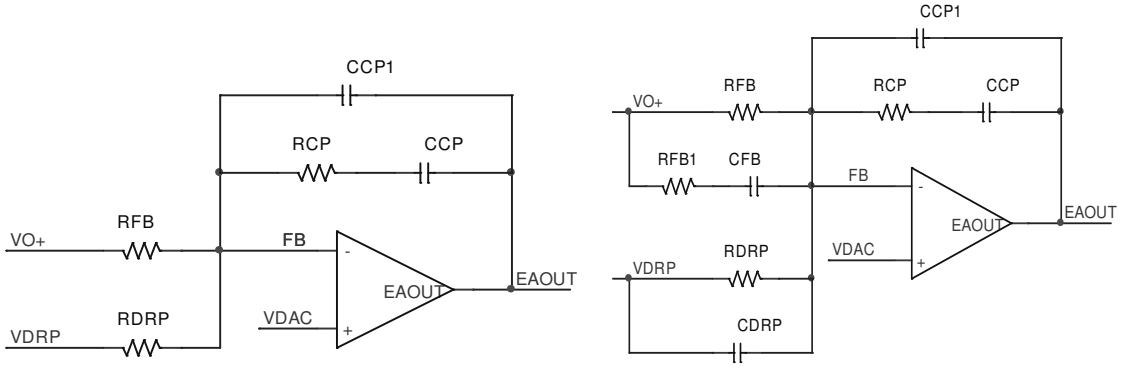
VOLTAGE LOOP COMPENSATION

The adaptive voltage positioning (AVP) is usually adopted in the computer applications to improve the transient response and reduce the power loss at heavy load. Like current mode control, the adaptive voltage positioning loop introduces an extra zero to the voltage loop and splits the double poles of the power stage, which makes the voltage loop compensation much easier.

Adaptive voltage positioning lowers the converter voltage by RO*IO, where RO is the required output impedance of the converter. Pre-select feedback resistor RFB, and calculate the droop resistor RDRP,

$$R_{DRP} = \frac{R_{FB} * R_{L\_MAX} * G_{CS}}{n * R_O} \qquad (21)$$

The selection of compensation types depends on the output capacitors used in the converter. For applications using Electrolytic, Polymer or AL-Polymer capacitors and running at lower frequency, type II compensation shown in Figure 21(a) is usually enough. While for the applications using only ceramic capacitors and running at higher frequency, type III compensation shown in Figure 21(b) is preferred.



(a) Type II compensation (b) Type III compensation

Figure 21 - Voltage loop compensation network

For applications where AVP is not required, the compensation is the same as for the regular voltage mode control. For converters using Polymer, AL-Polymer, and ceramic capacitors, which have much higher ESR zero frequency, type III compensation is required as shown in Figure 22(b) with RDRP and CDRP removed.

Type II Compensation for AVP Applications

Determine the compensation at no load, the worst case condition. Choose the crossover frequency fc between 1/10 and 1/5 of the switching frequency per phase. Assume the time constant of the resistor and capacitor across the output inductors matches that of the inductor, and determine RCP and CCP from (23) and (23), where LE and CE are the equivalent inductance of output inductors and the equivalent capacitance of output capacitors respectively.

$$R_{CP} = \frac{(2\pi * f_C)^2 * L_E * C_E * R_{FB} * 5}{V_I * \sqrt{1 + (2\pi * f_C * C * R_C)^2}} \quad (22)$$

$$C_{CP} = \frac{10 * \sqrt{L_E * C_E}}{R_{CP}} \quad (23)$$

CCP1 is optional and may be needed in some applications to reduce the jitter caused by the high frequency noise. A ceramic capacitor between 10pF and 220pF is usually enough.

Type III Compensation for AVP Applications

Determine the compensation at no load, the worst case condition. Assume the time constant of the resistor and capacitor across the output inductors matches that of the inductor, the crossover frequency and phase margin of the voltage loop can be estimated by (24) and (25), where RLE is the equivalent resistance of inductor DCR.

$$f_{C1} = \frac{R_{DRP}}{2\pi * C_E * G_{CS} * R_{FB} * R_{LE}} \quad (24)$$

$$\theta_{C1} = 90 - A\tan(0.5) * \frac{180}{\pi} \quad (25)$$

Choose the desired crossover frequency fc around fc1 estimated by (24) or choose fc between 1/10 and 1/5 of the switching frequency per phase, and select the components to ensure the slope of close loop gain is -20dB per decade around the crossover frequency. Choose resistor RFB1 according to (26), and determine CFB and CDRP from (27) and (28).

$$R_{FB1} = \frac{1}{2} R_{FB} \quad \text{to} \quad R_{FB1} = \frac{2}{3} R_{FB} \quad (26)$$

$$C_{FB} = \frac{1}{4\pi * f_C * R_{FB1}} \quad (27)$$

$$C_{DRP} = \frac{(R_{FB} + R_{FB1}) * C_{FB}}{R_{DRP}} \quad (28)$$

RCP and CCP have limited effect on the crossover frequency, and are used only to fine tune the crossover frequency and transient load response. Determine RCP and CCP from (29) and (30).

$$R_{CP} = \frac{(2\pi * f_C)^2 * L_E * C_E * R_{FB} * 5}{V_I} \quad (29)$$

$$C_{CP} = \frac{10 * \sqrt{L_E * C_E}}{R_{CP}} \quad (30)$$

C_{CP1} is optional and may be needed in some applications to reduce the jitter caused by the high frequency noise. A ceramic capacitor between 10pF and 220pF is usually enough.

Type III Compensation for Non-AVP Applications

Resistor R_{DRP} and capacitor C_{DRP} are not needed. Choose the crossover frequency fc between 1/10 and 1/5 of the switching frequency per phase and select the desired phase margin θc. Calculate K factor from (31), and determine the component values based on (32) to (36),

$$K = \tan[\frac{\pi}{4} * (\frac{\theta_C}{180} + 1.5)] \quad (31)$$

$$R_{CP} = R_{FB} * \frac{(2\pi * \sqrt{L_E * C_E} * f_C)^2 * 5}{V_I * K} \quad (32)$$

$$C_{CP} = \frac{K}{2\pi * f_C * R_{CP}} \quad (33)$$

$$C_{CP1} = \frac{1}{2\pi * f_C * K * R_{CP}} \quad (34)$$

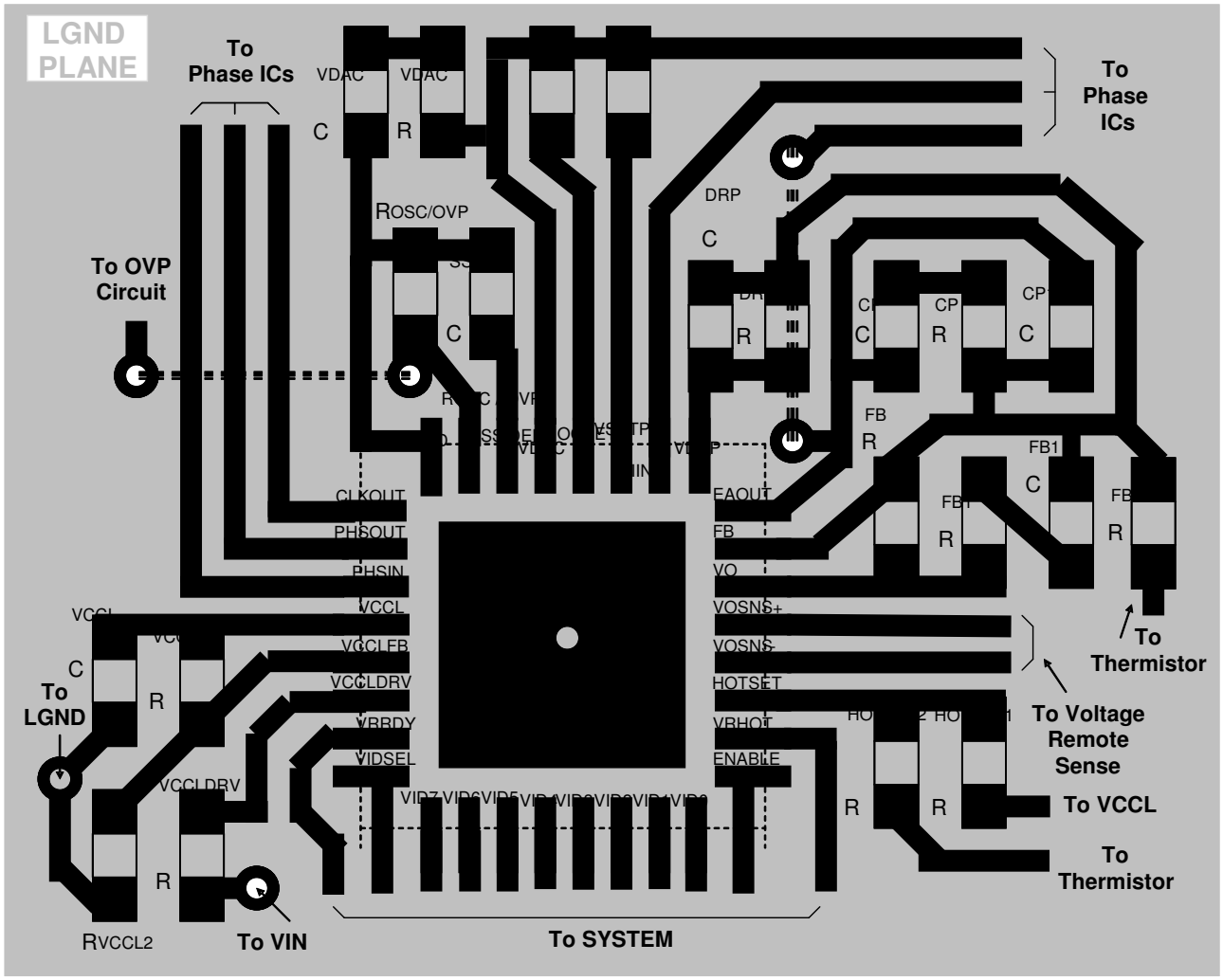
$$C_{FB} = \frac{K}{2\pi * f_C * R_{FB}} \quad (35)$$

$$R_{FB1} = \frac{1}{2\pi * f_C * K * C_{FB}} \quad (36)$$

PCB LAYOUT GUIDELINES

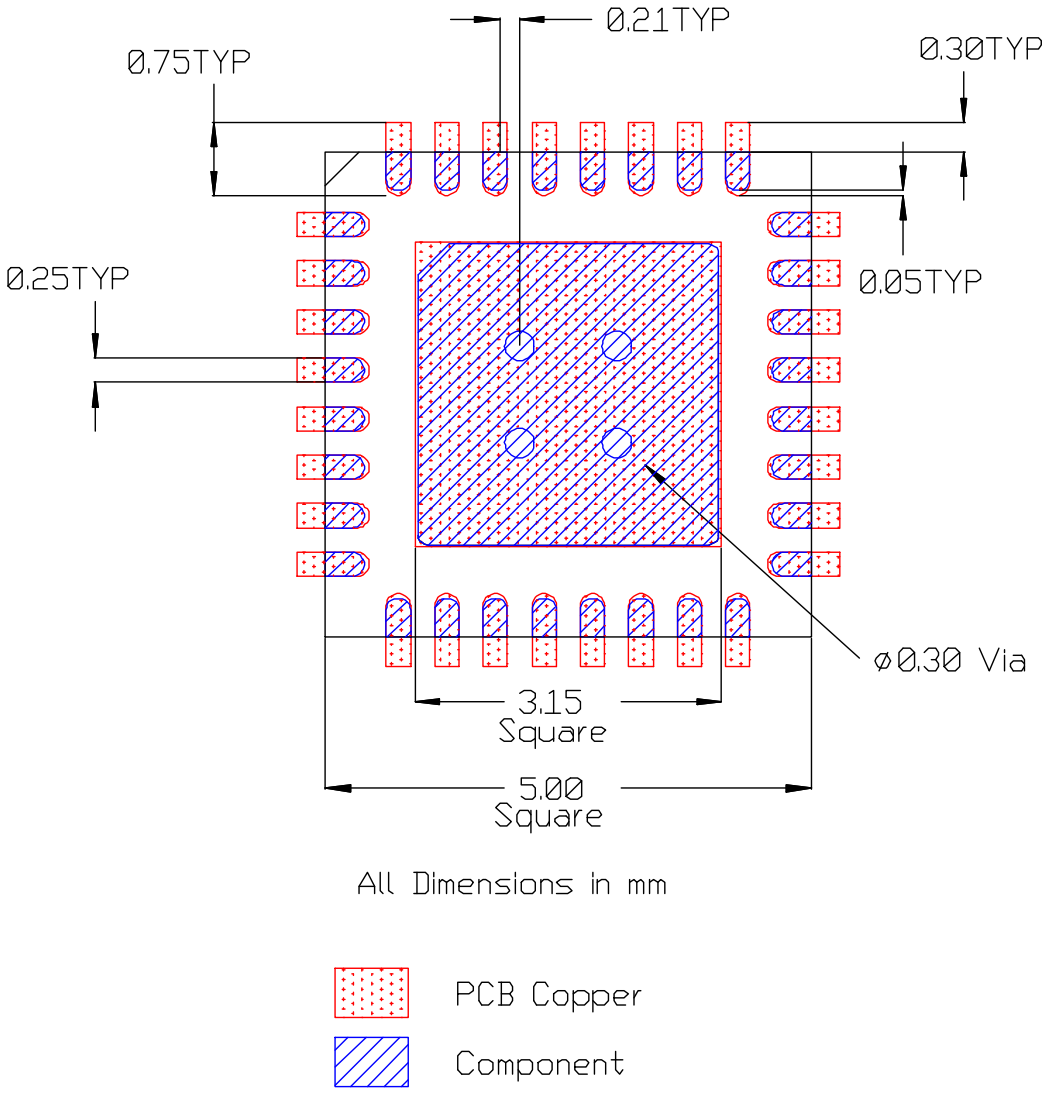
The following layout guidelines are recommended to reduce the parasitic inductance and resistance of the PCB layout, therefore minimizing the noise coupled to the IC.

- Dedicate at least one middle layer for a ground plane LGND.
- Connect the ground tab under the control IC to LGND plane through a via.
- Place VCCL decoupling capacitor VCCL as close as possible to VCCL and LGND pins.
- Place the following critical components on the same layer as control IC and position them as close as possible to the respective pins, ROSC, ROCSET, RVDAC, CVDAC, and CSS/DEL. Avoid using any via for the connection.
- Place the compensation components on the same layer as control IC and position them as close as possible to EAOUT, FB, VO and VDRP pins. Avoid using any via for the connection.
- Use Kelvin connections for the remote voltage sense signals, VOSNS+ and VOSNS-, and avoid crossing over the fast transition nodes, i.e. switching nodes, gate drive signals and bootstrap nodes.
- Avoid analog control bus signals, VDAC, IIN, and especially EAOUT, crossing over the fast transition nodes.
- Separate digital bus, CLKOUT, PHSOUT and PHSIN from the analog control bus and other compensation components.



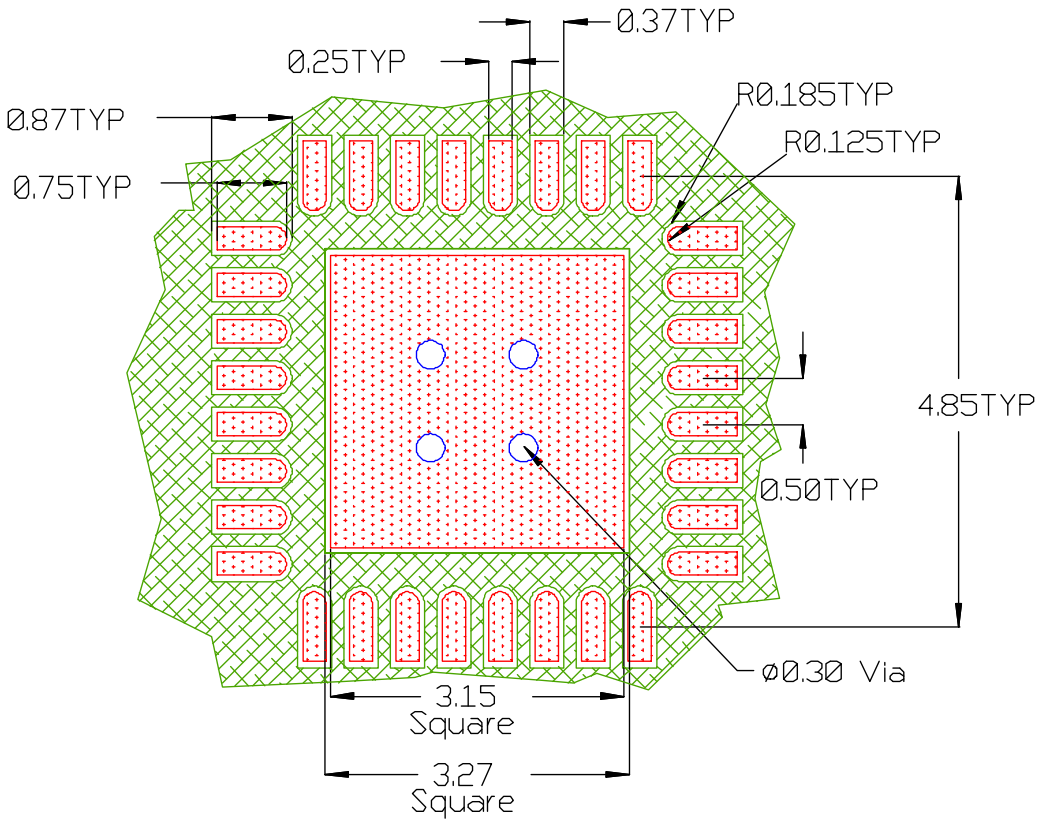
PCB METAL AND COMPONENT PLACEMENT

- Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to minimize shorting.
- Lead land length should be equal to maximum part lead length + 0.3 mm outboard extension + 0.05mm inboard extension. The outboard extension ensures a large and inspectable toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.
- Center pad land length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be ≥ 0.17mm for 2 oz. Copper (≥ 0.1mm for 1 oz. Copper and ≥ 0.23mm for 3 oz. Copper)
- Four 0.3mm diameter vias shall be placed in the pad land spaced at 1.2mm, and connected to ground to minimize the noise effect on the IC and to transfer heat to the PCB.
- No PCB traces should be routed nor vias placed under any of the 4 corners of the IC package. Doing so can cause the IC to rise up from the PCB resulting in poor solder joints to the IC leads.



SOLDER RESIST

- The solder resist should be pulled away from the metal lead lands by a minimum of 0.06mm. The solder resist mis-alignment is a maximum of 0.05mm and it is recommended that the lead lands are all Non Solder Mask Defined (NSMD). Therefore pulling the S/R 0.06mm will always ensure NSMD pads.
- The minimum solder resist width is 0.13mm.
- At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of ≥ 0.17mm remains.
- The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.06mm to accommodate solder resist mis-alignment. In 0.5mm pitch cases it is allowable to have the solder resist opening for the land pad to be smaller than the part pad.
- Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.
- The four vias in the land pad should be tented or plugged from bottom board side with solder resist.



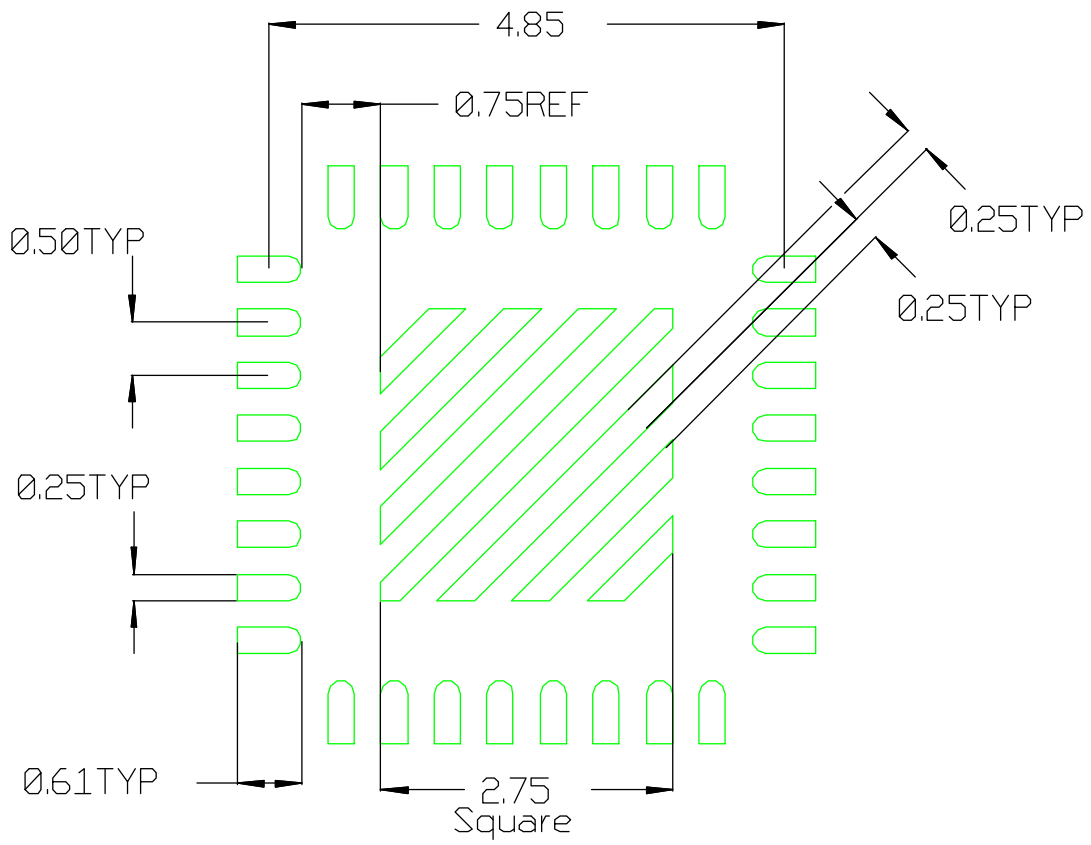
All Dimensions in mm

PCB Copper

PCB Solder Resist

STENCIL DESIGN

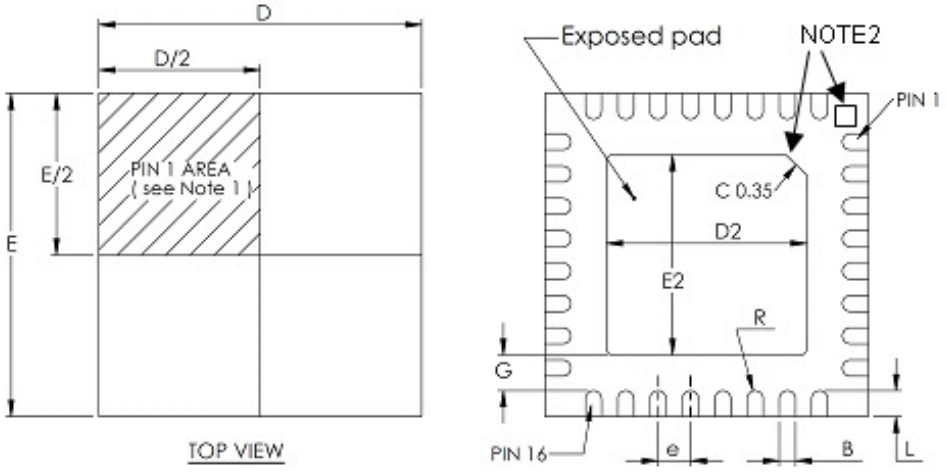
- The stencil apertures for the lead lands should be approximately 80% of the area of the lead lands. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
- The stencil lead land apertures should therefore be shortened in length by 80% and centered on the lead land.
- The land pad aperture should be striped with 0.25mm wide openings and spaces to deposit approximately 50% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.



Stencil Aperture
All Dimensions in mm

PACKAGE INFORMATION

32L MLPQ (5 x 5 mm Body) – θ_{JA} = 24.4°C/W, θ_{JC} =0.86 °C/W



Note 1: Top details of pin #1 are optional, but must be located within the zone indicated. The identifier may be molded, or marked features.
Note 2: Pin #1 will be indicated on the bottom by either a chamfer or a square island.

32-PIN 5x5 (unit: MM)			
DIM	MIN	NOM	MAX
A	0.8	0.85	0.9
A1	0.00		0.05
A3	0.20 REF		
B	0.20	0.25	0.30
D	4.95	5.00	5.05
D2	3.00	3.10	3.20
E	4.95	5.00	5.05
E2	3.00	3.10	3.20
e	0.5 REF		
G	0.55 REF		
L	0.30	0.40	0.50
R	0.125 TYP		

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

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