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March 1988
 Revised October 2000

74F646 • 74F646B • 74F648 Octal Transceiver/Register with 3-STATE Outputs

General Description

These devices consist of bus transceiver circuits with 3-STATE, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control \bar{G} and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control \bar{G} is Active LOW. In the isolation mode (control \bar{G} HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- 74F648 has inverting data paths
- 74F646/74F646B have non-inverting data paths
- 74F646B is a faster version of the 74F646
- 3-STATE outputs
- 300 mil slim DIP

Ordering Code:

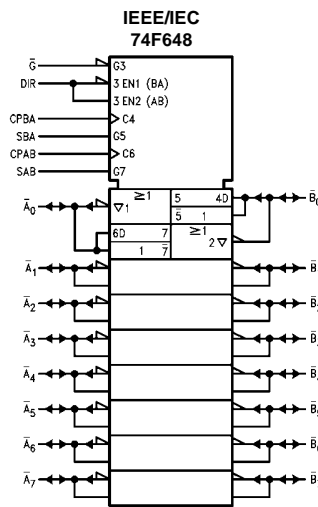
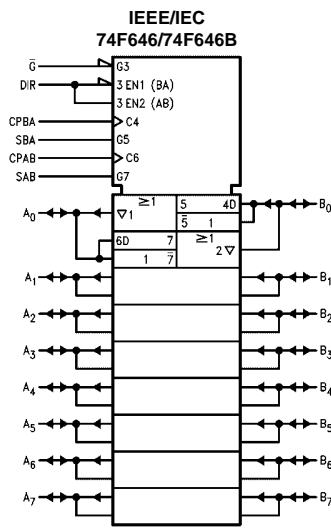
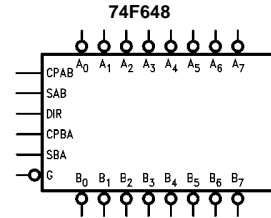
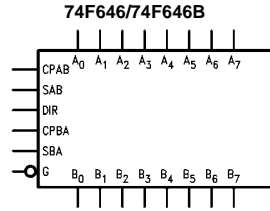
Order Number	Package Number	Package Description
74F646SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F646MSA	MSA24	24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74F646SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
74F646BSC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F646BSPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
74F648SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F648SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

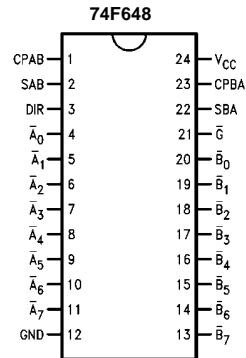
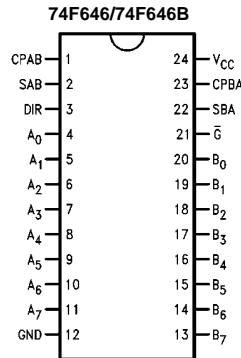
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Logic Symbols



Connection Diagrams



Unit Loading/Fan Out

Pin Names	Description	U.L.	
		HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A ₀ -A ₇	Data Register A Inputs/ 3-STATE Outputs	3.5/1.083 600/106.6 (80)	70 μ A/-650 μ A -12 mA/64 mA (48 mA)
B ₀ -B ₇	Data Register B Inputs/ 3-STATE Outputs	3.5/1.083 600/106.6 (80)	70 μ A/-650 μ A -12 mA/64 mA (48 mA)
CPAB, CPBA	Clock Pulse Inputs	1.0/1.0	20 μ A/-0.6 mA
SAB, SBA	Select Inputs	1.0/1.0	20 μ A/-0.6 mA
\bar{G}	Output Enable Input	1.0/1.0	20 μ A/-0.6 mA
DIR	Direction Control Input	1.0/1.0	20 μ A/-0.6 mA

Function Table

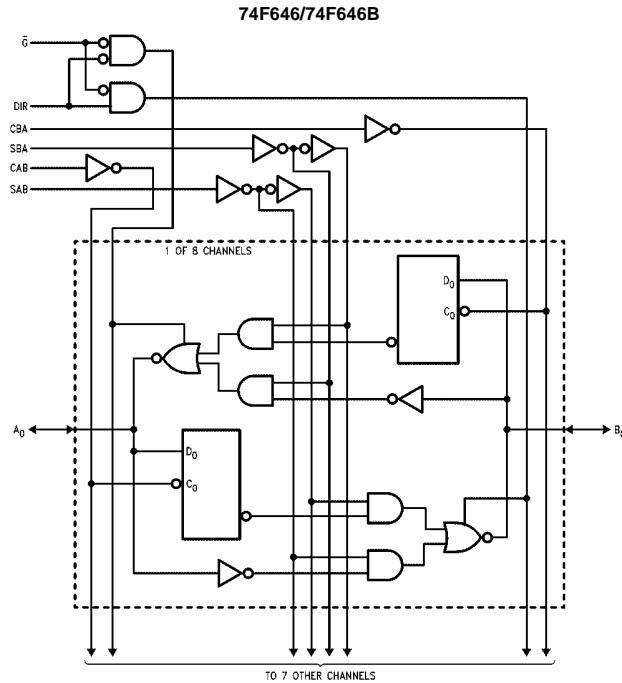
Inputs						Data I/O (Note 1)		Function
\bar{G}	DIR	CPAB	CPBA	SAB	SBA	A ₀ -A ₇	B ₀ -B ₇	
H	X	H or L	H or L	X	X			Isolation
H	X	\curvearrowright	X	X	X	Input	Input	Clock A _n Data into A Register
H	X	X	\curvearrowright	X	X			Clock B _n Data into B Register
L	H	X	X	L	X	Input	Output	A _n to B _n —Real Time (Transparent Mode)
L	H	\curvearrowright	X	L	X			Clock A _n Data into A Register
L	H	H or L	X	H	X			A Register to B _n (Stored Mode)
L	H	\curvearrowright	X	H	X			Clock A _n Data into A Register and Output to B _n
L	L	X	X	X	L	Output	Input	B _n to A _n —Real Time (Transparent Mode)
L	L	X	\curvearrowright	X	L			Clock B _n Data into B Register
L	L	X	H or L	X	H			B Register to A _n (Stored Mode)
L	L	X	\curvearrowright	X	H			Clock B _n Data into B Register and Output to A _n

H = HIGH Voltage Level
L = LOW Voltage Level
X = Irrelevant
 \curvearrowright = LOW-to-HIGH Transition

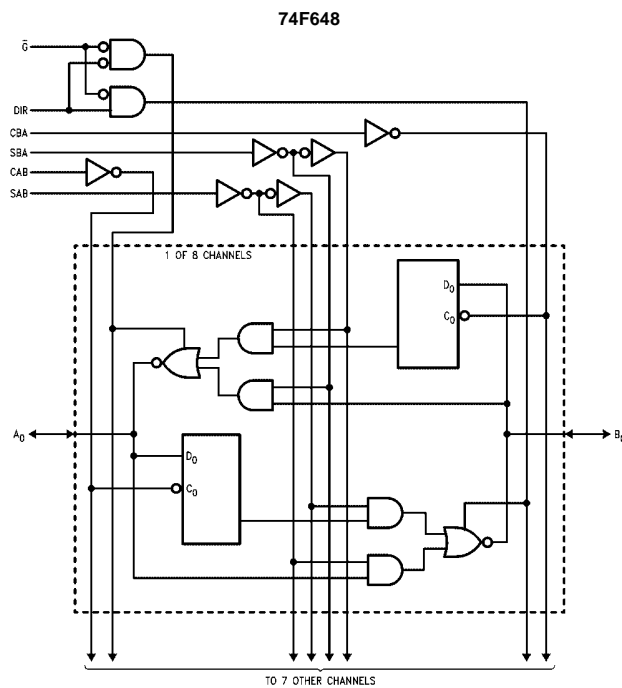
Note 1: The data output functions may be enabled or disabled by various signals at the \bar{G} and DIR Inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.

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Logic Diagrams



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



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Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA (Non I/O Pins)
V _{OH}	Output HIGH Voltage 10% V _{CC}	2.0			V	Min	I _{OH} = -15 mA (A _n , B _n)
V _{OL}	Output LOW Voltage 10% V _{CC}			0.55	V	Min	I _{OL} = 64 mA (A _n , B _n)
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V (Non I/O Pins)
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V (Non I/O Pins)
I _{BVIT}	Input HIGH Current Breakdown (I/O)			0.5	mA	Max	V _{IN} = 5.5V (A _n , B _n)
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V (Non I/O Pins)
I _{IH} + I _{OZH}	Output Leakage Current			70	μA	Max	V _{OUT} = 2.7V (A _n , B _n)
I _{IL} + I _{OZL}	Output Leakage Current			-650	μA	Max	V _{OUT} = 0.5V (A _n , B _n)
I _{OS}	Output Short-Circuit Current	-100		-225	mA	Max	V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V
I _{CCH}	Power Supply Current			135	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current			150	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current			150	mA	Max	V _O = HIGH Z

Absolute Maximum Ratings (Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

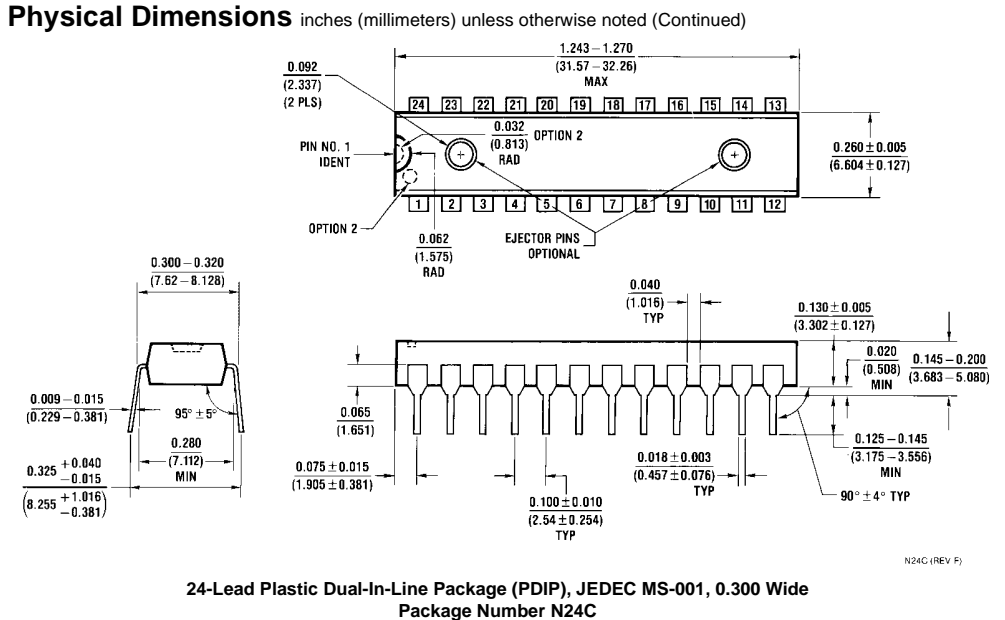
DC Electrical Characteristics

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AC Electrical Characteristics 74F646/74F648								
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF		T _A = -55°C to +125°C V _{CC} = +5.0V C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF		Units
		Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	90		75		90		MHz
t _{PLH}	Propagation Delay	2.0	7.0	2.0	8.5	2.0	8.0	ns
t _{PHL}	Clock to Bus	2.0	8.0	2.0	9.5	2.0	9.0	ns
t _{PLH}	Propagation Delay	1.0	7.0	1.0	8.0	1.0	7.5	ns
t _{PHL}	Bus to Bus (74F646)	1.0	6.5	1.0	8.0	1.0	7.0	ns
t _{PLH}	Propagation Delay	2.0	8.5	1.0	10.0	2.0	9.0	ns
t _{PHL}	Bus to Bus (74F648)	1.0	7.5	1.0	9.0	1.0	8.0	ns
t _{PLH}	Propagation Delay	2.0	8.5	2.0	11.0	2.0	9.5	ns
t _{PHL}	SBA or SAB to A or B	2.0	8.0	2.0	10.0	2.0	9.0	ns
t _{PZH}	Enable Time	2.0	8.5	2.0	10.0	2.0	9.0	ns
t _{PZL}	OE to A or B	2.0	12.0	2.0	13.5	2.0	12.5	ns
t _{PHZ}	Disable Time	1.0	7.5	1.0	9.0	1.0	8.5	ns
t _{PLZ}	OE to A or B	2.0	9.0	2.0	11.0	2.0	9.5	ns
t _{PZH}	Enable Time	2.0	14.0	2.0	16.0	2.0	15.0	ns
t _{PZL}	DIR to A or B	2.0	13.0	2.0	15.0	2.0	14.0	ns
t _{PHZ}	Disable Time	1.0	9.0	1.0	10.0	1.0	9.5	ns
t _{PLZ}	DIR to A or B	2.0	11.0	2.0	12.0	2.0	11.5	ns

AC Operating Requirements 74F646/74F648								
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V		T _A = -55°C to +125°C V _{CC} = +5.0V		T _A = 0°C to +70°C V _{CC} = +5.0V		Units
		Min	Max	Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	5.0		5.0		5.0		ns
t _S (L)	Bus to Clock	5.0		5.0		5.0		ns
t _H (H)	Hold Time, HIGH or LOW	2.0		2.5		2.0		ns
t _H (L)	Bus to Clock	2.0		2.5		2.0		ns
t _W (H)	Clock Pulse Width	5.0		5.0		5.0		ns
t _W (L)	HIGH or LOW	5.0		5.0		5.0		ns

AC Electrical Characteristics 74F646B								
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF		T _A = -55°C to +125°C V _{CC} = +5.0V C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF		Units
		Min	Max	Min	Max	Min	Max	
t _{MAX}	Maximum Clock Frequency	165				150		MHz
t _{PLH}	Propagation Delay	2.5	7.0			2.5	8.0	ns
t _{PHL}	Clock to Bus	3.0	7.5			3.0	8.0	
t _{PLH}	Propagation Delay	2.0	6.0			2.0	7.0	ns
t _{PHL}	Bus to Bus	2.0	6.0			2.0	7.0	
t _{PLH}	Propagation Delay	2.5	7.5			2.5	8.5	ns
t _{PHL}	SBA or SAB to A or B	2.5	7.5			2.5	8.5	
t _{PZH}	Enable Time	2.5	6.5			2.5	8.0	ns
t _{PZL}	$\overline{\text{OE}}$ to A or B	2.5	9.0			2.5	10.0	
t _{PHZ}	Disable Time	1.5	6.5			1.5	7.5	ns
t _{PLZ}	$\overline{\text{OE}}$ to A or B	2.0	7.0			2.0	8.5	
t _{PZH}	Enable Time	2.0	7.0			2.0	8.5	ns
t _{PZL}	DIR to A or B	3.0	9.5			3.0	10.0	
t _{PHZ}	Disable Time	1.5	7.5			1.5	8.5	ns
t _{PLZ}	DIR to A or B	2.5	8.5			2.5	9.5	
AC Operating Requirements 74F646B								
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V		T _A = -55°C to +125°C V _{CC} = +5.0V		T _A = 0°C to +70°C V _{CC} = +5.0V		Units
		Min	Max	Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	5.0				4.0		ns
t _S (L)	Bus to Clock	5.0				4.0		
t _H (H)	Hold Time, HIGH or LOW	1.5				1.5		ns
t _H (L)	Bus to Clock	1.5				1.5		
t _W (H)	Clock Pulse Width	5.0				5.0		ns
t _W (L)	HIGH or LOW	5.0				5.0		



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