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Maxim Integrated
MAX17120ETJ+

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EIS electronic components

Distributor of Maxim Integrated: Excellent Integrated System Limited
Datasheet of MAX17120ETJ+ - IC DRVR SCAN TFT LDC 32-TQFN
Contact us: sales@integrated-circuit.com Website: www.integrated-circuit.com

RELIABILITY REPORT

FOR

MAX17120ETJ+

PLASTIC ENCAPSULATED DEVICES

September 4, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
Richard Aburano
Quality Assurance
Manager, Reliability Operations

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Conclusion

The MAX17120ETJ+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX17120 includes three high-voltage, level-shifting scan drivers for TFT panel integrated gate logic. Each scan driver has two channels that switch complementarily. The scan driver outputs swing from +40V to -30V and can swiftly drive capacitive loads. To save power, the scan driver's complementary outputs share the charge of their capacitive load before they change states.

The MAX17120 is available in a 32-pin, 5mm x 5mm, thin QFN package with a maximum thickness of 0.8mm for ultra-thin LCD panels.

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II. Manufacturing Information

A. Description/Function:	Triple High-Voltage Scan Driver for TFT LCD
B. Process:	S4
C. Number of Device Transistors:	2800
D. Fabrication Location:	California
E. Assembly Location:	Thailand
F. Date of Initial Production:	July 25, 2009

III. Packaging Information

A. Package Type:	32-pin TQFN 5x5
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Non-conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3694
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	53.7°C/W
K. Single Layer Theta Jc:	19.9°C/W
L. Multi Layer Theta Ja:	40.2°C/W
M. Multi Layer Theta Jc:	19.9°C/W

IV. Die Information

A. Dimensions:	63 X 86 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are pending. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

λ = 22.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the S4 Process results in a FIT Rate of 0.28 @ 25C and 4.85 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The PF59 die type has been found to have all pins able to withstand a HBM transient pulse of:

HBM ESD: +/-2500V per JEDEC JESD22-A114
CDM ESD: +/-750V per JESD22-C101
MM ESD: +/-200V per JEDEC JESD22-A115

Latch-Up testing has shown that this device withstands a current of +/-100 mA, 1.5x VCCMax Overvoltage per JESD78.

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Table 1
Reliability Evaluation Test Results

MAX17120ETJ+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2) 85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2) Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

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