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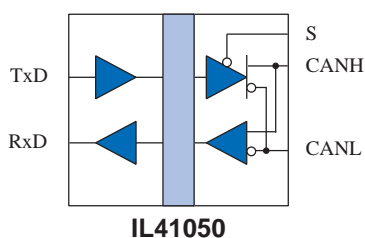
[NVE Corporation](#)
[IL41050TE](#)

For any questions, you can email us directly:

sales@integrated-circuit.com

Isolated High-Speed CAN Transceiver

Functional Diagram



| V _{DD2} (V) | TxD ⁽¹⁾ | S | CANH | CANL | Bus State | RxD |
|--------------------------|--------------------|--------------------|---------------------|---------------------|-----------|------|
| 4.75 to 5.25 | ↓ | Low ⁽²⁾ | High | Low | Dominant | Low |
| 4.75 to 5.25 | X | High | V _{DD2} /2 | V _{DD2} /2 | Recessive | High |
| 4.75 to 5.25 | ↑ | X | V _{DD2} /2 | V _{DD2} /2 | Recessive | High |
| <2V (no pwr) | X | X | 0<V<2.5 | 0<V<2.5 | Recessive | High |
| 2>V _{DD2} <4.75 | >2V | X | 0<V<2.5 | 0<V<2.5 | Recessive | High |

Table 1. Function table.

Notes:

1. TxD input is edge triggered: ↑ = Logic Lo to Hi, ↓ = Hi to Lo
 2. Valid for logic state as described or open circuit
- X = don't care

Features

- Single-chip isolated CAN/DeviceNet transceiver
- Fully compliant with the ISO 11898 CAN standard
- Best-in-class loop delay (180 ns typ.)
- 3.0 V to 5.5 V input power supplies
- >110-node fan-out
- High speed (up to 1 Mbps)
- 2,500 V_{RMS} isolation (1 minute)
- Very low Electromagnetic Emission (EME)
- Differential signaling for excellent Electromagnetic Immunity (EMI)
- 30 kV/μs transient immunity
- Silent mode to disable transmitter
- Unpowered nodes do not disturb the bus
- Transmit data (TxD) dominant time-out function
- Edge triggered, non-volatile input improves noise performance
- Bus pin transient protection for automotive environment
- Thermal shutdown protection
- Short-circuit protection for ground and bus power
- -55°C to +125°C operating temperature
- 0.15" and 0.3" and 16-pin JEDEC-standard SOIC packages
- UL1577 and IEC 61010-2001 approved

Applications

- Noise-critical CAN
- Partially-powered CAN
- DeviceNet
- Factory automation

Description

The IL41050 is a galvanically isolated, high-speed CAN (Controller Area Network) transceiver, designed as the interface between the CAN protocol controller and the physical bus. The IL41050 provides isolated differential transmit capability to the bus and isolated differential receive capability to the CAN controller via NVE's patented* IsoLoop spintronic Giant Magnetoresistance (GMR) technology.

Advanced features facilitate reliable bus operation. Unpowered nodes do not disturb the bus, and a unique non-volatile programmable power-up feature prevents unstable nodes. The devices also have a hardware-selectable silent mode that disables the transmitter.

Designed for harsh CAN and DeviceNet environments, IL41050T transceivers have transmit data dominant time-out, bus pin transient protection, thermal shutdown protection, and short-circuit protection. Unique edge-triggered inputs improve noise performance. Unlike optocouplers or other isolation technologies, IsoLoop isolators have indefinite life at high voltage.

Absolute Maximum Ratings^{(1) (2)}

| Parameters | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|-------------------------------------|---------------------|--------|------|----------------|-------|--|
| Storage temperature | T_S | -55 | | 150 | °C | |
| Ambient operating temperature | T_A | -55 | | 135 | °C | |
| DC voltage at CANH and CANL pins | $V_{CANH} V_{CANL}$ | -27 | | 40 | V | 0 V < V_{DD2} < 5.25 V; indefinite duration |
| Supply voltage | V_{DD1}, V_{DD2} | -0.5 | | 6 | V | |
| Digital input voltage | V_{TxD}, V_S | -0.3 | | $V_{DD} + 0.3$ | V | |
| Digital output voltage | V_{RxD} | -0.3 | | $V_{DD} + 0.3$ | V | |
| DC voltage at V_{REF} | V_{REF} | -0.3 | | $V_{DD} + 0.3$ | V | |
| Transient Voltage at CANH or CANL | $V_{TH(CAN)}$ | -200 | | 200 | V | |
| Electrostatic discharge at all pins | V_{esd} | -4,000 | | 4,000 | V | Human body model |
| Electrostatic discharge at all pins | V_{esd} | -200 | | 200 | V | Machine model |

Recommended Operating Conditions

| Parameters | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|--------------------------|-------------|------|------------------------|-------|--|
| Supply voltage | V_{DD1} V_{DD2} | 3.0 4.75 | | 5.5 5.25 | V | |
| Input voltage at any bus terminal (separately or common mode) | V_{CANH} V_{CANL} | -12 | | 12 | V | |
| High-level digital input voltage ^{(3) (4)} | V_{IH} | 2.0 2.4 | | V_{DD1} V_{DD1} | V | $V_{DD1} = 3.3$ V $V_{DD1} = 5.0$ V |
| Low-level digital input voltage ^{(3) (4)} | V_{IL} | 2.0 | | V_{DD2} | V | $V_{DD2} = 5.0$ V |
| Digital output current (RxD) | I_{OH} | 0 | | 0.8 | mA | $V_{DD1} = 3.3$ V to 5 V |
| Ambient operating temperature | T_A | -8 | | 8 | °C | |
| Digital input signal rise and fall times | t_{IR}, t_{IF} | -55 | | 125 | µs | |

Insulation Specifications

| Parameters | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|------------------------------|--------|------|-------------------------|------|-----------------------|-----------------------|
| Creepage distance (external) | | 8.08 | | | mm | |
| Barrier impedance | | | $> 10^{14} \parallel 7$ | | $\Omega \parallel pF$ | |
| Leakage current | | | 0.2 | | μA_{RMS} | 240 V_{RMS} , 60 Hz |

Safety and Approvals
IEC61010-2001

TUV Certificate Numbers: N1502812 (pending)

Classification: Reinforced Insulation

| Model | Package | Pollution Degree | Material Group | Max. Working Voltage |
|---------|-----------------------|------------------|----------------|----------------------|
| IL41050 | SOIC (0.15" and 0.3") | II | III | 300 V_{RMS} |

UL 1577

Component Recognition Program File Number: E207481

 Rated 2,500 V_{RMS} for 1 minute

Soldering Profile

Per JEDEC J-STD-020C

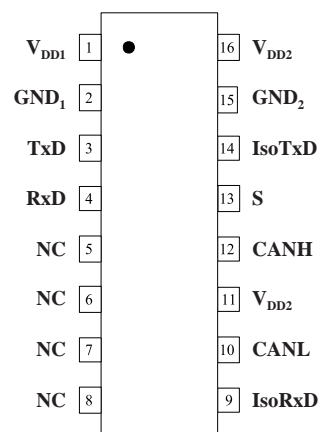
Moisture Sensitivity Level: MSL=2

Notes:

1. Absolute Maximum specifications mean the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. All voltages are with respect to network ground except differential I/O bus voltages.
3. The TxD input is edge sensitive. Voltage magnitude of the input signal is specified, but edge rate specifications must also be met.
4. The maximum time allowed for a logic transition at the TxD input is 1 µs.

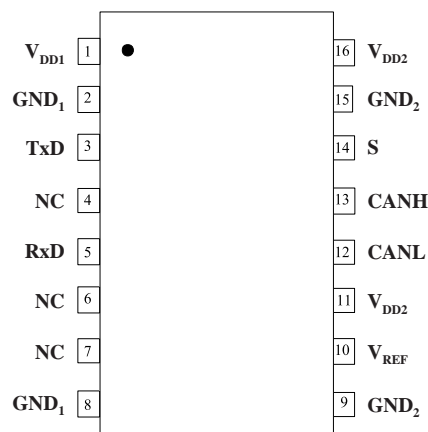
IL41050-3 Pin Connections (0.15" SOIC Package)

| | | |
|----|------------------|--|
| 1 | V _{DD1} | V _{DD1} power supply input |
| 2 | GND ₁ | V _{DD1} power supply ground return |
| 3 | TxD | Transmit Data input |
| 4 | RxD | Receive Data output |
| 5 | NC | No internal connection |
| 6 | NC | No internal connection |
| 7 | NC | No internal connection |
| 8 | NC | No internal connection |
| 9 | IsoRxD | Isolated RxD output. No connection should be made to this pin. |
| 10 | CANL | Low level CANbus line |
| 11 | V _{DD2} | V _{DD2} CAN I/O bus circuitry power supply input* |
| 12 | CANH | High level CANbus line |
| 13 | S | Mode select input. Leave open or set low for normal operation; set high for silent mode. |
| 14 | IsoTxD | Isolated TxD output. No connection should be made to this pin. |
| 15 | GND ₂ | V _{DD2} power supply ground return |
| 16 | V _{DD2} | V _{DD2} isolation power supply input* |



IL41050 Pin Connections (0.3" SOIC Package)

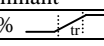
| | | |
|----|------------------|--|
| 1 | V _{DD1} | V _{DD1} power supply input |
| 2 | GND ₁ | V _{DD1} power supply ground return (pin 2 is internally connected to pin 8) |
| 3 | TxD | Transmit Data input |
| 4 | NC | No internal connection |
| 5 | RxD | Receive Data output |
| 6 | NC | No internal connection |
| 7 | NC | No internal connection |
| 8 | GND ₁ | V _{DD1} power supply ground return (pin 8 is internally connected to pin 2) |
| 9 | GND ₂ | V _{DD2} power supply ground return (pin 9 is internally connected to pin 15) |
| 10 | V _{REF} | Reference voltage output (nominally 50% of V _{DD2}) |
| 11 | V _{DD2} | V _{DD2} CAN I/O bus circuitry power supply input* |
| 12 | CANL | Low level CANbus line |
| 13 | CANH | High level CANbus line |
| 14 | S | Mode select input. Leave open or set low for normal operation; set high for silent mode. |
| 15 | GND ₂ | V _{DD2} power supply ground return (pin 15 is internally connected to pin 9) |
| 16 | V _{DD2} | V _{DD2} isolation power supply input* |



*NOTE: Pin 11 is not internally connected to pin 16; both should be connected to the V_{DD2} power supply for normal operation.

Specifications

Electrical Specifications are T_{min} to T_{max} and V_{DD1} , $V_{DD2} = 4.75\text{ V}$ to 5.25 V unless otherwise stated.

| Parameters | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|----------------------------|----------------|---------------|-----------------|---------------|--|
| Power Supply Current | | | | | | |
| Quiescent supply current (recessive) | I_{QVDD1} | 1 0.7 | 1.75 1.4 | 3.0 2.0 | mA | $dr = 0\text{ bps}$; $V_{DD1} = 5\text{ V}$ $dr = 0\text{ bps}$; $V_{DD1} = 3.3\text{ V}$ |
| Dynamic supply current (dominant) | I_{VDD1} | 1.2 0.9 | 2.0 1.6 | 3.2 2.2 | mA | $dr = 1\text{ Mbps}$, $R_L = 60\Omega$; $V_{DD1} = 5\text{ V}$ $dr = 1\text{ Mbps}$, $R_L = 60\Omega$; $V_{DD1} = 3.3\text{ V}$ |
| Quiescent supply current (recessive) | I_{QVDD2} | 3.5 | 6.75 | 13 | mA | 0 bps |
| Dynamic supply current (dominant) | I_{VDD2} | 26 | 52 | 78 | mA | 1 Mbps, $R_L = 60\Omega$ |
| Transmitter Data input (TxD)⁽¹⁾ | | | | | | |
| High level input voltage \uparrow | V_{IH} | 2.4 | | 5.25 | V | $V_{DD1} = 5\text{ V}$; recessive |
| High level input voltage \uparrow | V_{IH} | 2.0 | | 3.6 | V | $V_{DD1} = 3.3\text{ V}$; recessive |
| Low level input voltage \downarrow | V_{IL} | -0.3 | | 0.8 | V | Output dominant |
| TxD input rise and fall time ⁽²⁾ | t_r | | | 1 | μs | 10% to 90%  |
| High level input current | I_{IH} | -10 | | 10 | μA | $V_{TxD} = V_{DD1}$ |
| Low level input current | I_{IL} | 10 | | 10 | μA | $V_{TxD} = 0\text{ V}$ |
| Mode select input (S) | | | | | | |
| High level input voltage | V_{IH} | 2.0 | | $V_{DD2} + 0.3$ | V | Silent mode |
| Low level input voltage | V_{IL} | -0.3 | | 0.8 | V | High-speed mode |
| High level input current | I_{IH} | 20 | 30 | 45 | μA | $V_S = 2\text{ V}$ |
| Low level input current | I_{IL} | 15 | 30 | 10 | μA | $V_S = 0\text{ V}$ |
| Receiver Data output (RxD) | | | | | | |
| High level output current | I_{OH} | -2 | -8.5 | -20 | mA | $V_{RxD} = 0.8 V_{DD1}$ |
| Low level output current | I_{OL} | 2 | 8.5 | 20 | mA | $V_{RxD} = 0.45\text{ V}$ |
| Failsafe supply voltage⁽⁴⁾ | | | | | | |
| | V_{DD2} | 3.6 | | 3.9 | V | |
| Reference Voltage output (V_{REF}) | | | | | | |
| Reference Voltage output | V_{REF} | $0.45 V_{DD2}$ | $0.5 V_{DD2}$ | $0.55 V_{DD2}$ | V | $-50\ \mu\text{A} < I_{VREF} < +50\ \mu\text{A}$ |
| Bus lines (CANH and CANL) | | | | | | |
| Recessive voltage at CANH pin | $V_{O(reces)}\text{ CANH}$ | 2.0 | 2.5 | 3.0 | V | $V_{TxD} = V_{DD1}$, no load |
| Recessive voltage at CANL pin | $V_{O(reces)}\text{ CANL}$ | 2.0 | 2.5 | 3.0 | V | $V_{TxD} = V_{DD1}$, no load |
| Recessive current at CANH pin | $I_{O(reces)}\text{ CANH}$ | -2.0 | | +2.5 | mA | $-27\text{ V} < V_{CANH} < +32\text{ V}$; $0\text{ V} < V_{DD2} < 5.25\text{ V}$ |
| Recessive current at CANL pin | $I_{O(reces)}\text{ CANL}$ | -2.0 | | +2.5 | mA | $-27\text{ V} < V_{CANL} < +32\text{ V}$; $0\text{ V} < V_{DD2} < 5.25\text{ V}$ |
| Dominant voltage at CANH pin | $V_{O(dom)}\text{ CANH}$ | 3.0 | 3.6 | 4.25 | V | $V_{TxD} = 0\text{ V}$ |
| Dominant voltage at CANL pin | $V_{O(dom)}\text{ CANL}$ | 0.5 | 1.4 | 1.75 | V | $V_{TxD} = 0\text{ V}$ |
| Differential bus input voltage ($V_{CANH} - V_{CANL}$) | $V_{i(dif)(bus)}$ | 1.5 | 2.25 | 3.0 | V | $V_{TxD} = 0\text{ V}$; dominant $42.5\ \Omega < R_L < 60\ \Omega$ |
| | | -50 | 0 | +50 | mV | $V_{TxD} = V_{DD1}$; recessive; no load |
| Short-circuit output current at CANH | $I_{O(sc)}\text{ CANH}$ | -45 | -70 | -95 | mA | $V_{CANH} = 0\text{ V}$, $V_{TxD} = 0$ |
| Short-circuit output current at CANL | $I_{O(sc)}\text{ CANL}$ | 45 | 70 | 100 | mA | $V_{CANL} = 36\text{ V}$, $V_{TxD} = 0$ |
| Differential receiver threshold voltage | $V_{i(dif)(th)}$ | 0.5 | 0.7 | 0.9 | V | $-12\text{ V} < V_{CANL} < +12\text{ V}$; $-12\text{ V} < V_{CANH} < +12\text{ V}$ |
| Differential receiver input voltage hysteresis | $V_{i(dif)(hys)}$ | 50 | 70 | 100 | mV | $-12\text{ V} < V_{CANL} < +12\text{ V}$; $-12\text{ V} < V_{CANH} < +12\text{ V}$ |
| Common Mode input resistance at CANH | $R_{i(CM)(CANH)}$ | 15 | 25 | 35 | k Ω | |
| Common Mode input resistance at CANL | $R_{i(CM)(CANL)}$ | 15 | 25 | 35 | k Ω | |
| Matching between Common Mode input resistance at CANH, CANL | $R_{i(CM)(m)}$ | -3 | 0 | +3 | % | $V_{CANL} = V_{CANH}$ |
| Differential input resistance | $R_{i(dif)}$ | 25 | 50 | 75 | k Ω | |
| Input capacitance, CANH | $C_{i(CANH)}$ | | 7.5 | 20 | pF | $V_{TxD} = V_{DD1}$ |
| Input capacitance, CANL | $C_{i(CANL)}$ | | 7.5 | 20 | pF | $V_{TxD} = V_{DD1}$ |

Specifications (...cont.)

Electrical Specifications are T_{min} to T_{max} and V_{DD1} , $V_{DD2}=4.5\text{ V}$ to 5.5 V unless otherwise stated.

| | | | | | | |
|---------------------------------------|---------------------|-----|------|-----|--------------------|--|
| Differential input capacitance | $C_{i(dif)}$ | | 3.75 | 10 | pF | $V_{TxD} = V_{DD1}$ |
| Input leakage current at CANH | $I_{L(CANH)}$ | 100 | 170 | 250 | μA | $V_{CANH} = 5\text{ V}$, $V_{DD2} = 0\text{ V}$ |
| Input leakage current at CANL | $I_{L(CANL)}$ | 100 | 170 | 250 | μA | $V_{CANL} = 5\text{ V}$, $V_{DD2} = 0\text{ V}$ |
| Thermal Shutdown | | | | | | |
| Shutdown junction temperature | $T_{j(SD)}$ | 155 | 165 | 180 | $^{\circ}\text{C}$ | |
| Timing Characteristics | | | | | | |
| TxD to bus active delay | $t_{d(TxD-BUSon)}$ | 29 | 63 | 125 | ns | $V_S = 0\text{ V}$; $V_{DD1} = 5\text{ V}$ $V_S = 0\text{ V}$; $V_{DD1} = 3.3\text{ V}$ |
| | | 32 | 66 | 128 | | |
| TxD to bus inactive delay | $t_{d(TxD-BUSoff)}$ | 29 | 68 | 110 | ns | $V_S = 0\text{ V}$; $V_{DD1} = 5\text{ V}$ $V_S = 0\text{ V}$; $V_{DD1} = 3.3\text{ V}$ |
| | | 32 | 71 | 113 | | |
| Bus active to RxD delay | $t_{d(BUSon-RxD)}$ | 24 | 58 | 125 | ns | $V_S = 0\text{ V}$; $V_{DD1} = 5\text{ V}$ $V_S = 0\text{ V}$; $V_{DD1} = 3.3\text{ V}$ |
| | | 27 | 61 | 128 | | |
| Bus inactive to RxD delay | $t_{d(BUSoff-RxD)}$ | 49 | 103 | 170 | ns | $V_S = 0\text{ V}$; $V_{DD1} = 5\text{ V}$ $V_S = 0\text{ V}$; $V_{DD1} = 3.3\text{ V}$ |
| | | 52 | 106 | 173 | | |
| Loop delay low-to-high or high-to-low | T_{LOOP} | 53 | 180 | 210 | ns | $V_S = 0\text{ V}$ |
| TxD dominant time for timeout | $T_{dom(TxD)}$ | 250 | 457 | 765 | μs | $V_{TxD} = 0\text{ V}$ $3.0\text{ V} > V_{DD1} < 5.5\text{ V}$ |

Magnetic Field Immunity⁽³⁾

| $V_{DD1} = 5\text{ V}$, $V_{DD2} = 5\text{ V}$ | | | | | | |
|---|----------|-------|-------|--|-----|------------------------------|
| Power frequency magnetic immunity | H_{PF} | 2,500 | 3,000 | | A/m | 50 Hz/60 Hz |
| Pulse magnetic field immunity | H_{PM} | 3,000 | 3,500 | | A/m | $t_p = 8\text{ }\mu\text{s}$ |
| Cross-axis immunity multiplier | K_X | | 1.8 | | | Figure 1 |
| $V_{DD1} = 3.3\text{ V}$, $V_{DD2} = 5\text{ V}$ | | | | | | |
| Power frequency magnetic immunity | H_{PF} | 1,000 | 1,500 | | A/m | 50 Hz/60 Hz |
| Pulse magnetic field immunity | H_{PM} | 1,800 | 2,000 | | A/m | $t_p = 8\text{ }\mu\text{s}$ |
| Cross-axis immunity multiplier | K_X | | 1.5 | | | Figure 1 |

Notes:

1. The TxD input is edge sensitive. Voltage magnitude of the input signal is specified, but edge rate specifications must also be met.
2. The maximum time allowed for a logic transition at the TxD input is $1\text{ }\mu\text{s}$.
3. Uniform magnetic field applied across the pins of the device. Cross-axis multiplier effective when field is applied perpendicular to the pins.
4. If V_{DD2} falls below the specified failsafe supply voltage, RxD will go High.

Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Electromagnetic Compatibility

The IL41050 is fully compliant with generic EMC standards EN50081, EN50082-1 and the umbrella line-voltage standard for Information Technology Equipment (ITE) EN61000. The IsoLoop Isolator's Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards. NVE conducted compliance tests in the categories below:

EN50081-1

Residential, Commercial & Light Industrial
 Methods EN55022, EN55014

EN50082-2: Industrial Environment

Methods EN61000-4-2 (ESD), EN61000-4-3 (Electromagnetic Field Immunity), EN61000-4-4 (Electrical Transient Immunity), EN61000-4-6 (RFI Immunity), EN61000-4-8 (Power Frequency Magnetic Field Immunity), EN61000-4-9 (Pulsed Magnetic Field), EN61000-4-10 (Damped Oscillatory Magnetic Field)

ENV50204

Radiated Field from Digital Telephones (Immunity Test)

Immunity to external magnetic fields is higher if the field direction is "end-to-end" (rather than to "pin-to-pin") as shown in the diagram at right.

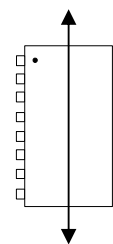


Fig. 1

Application Information

V_{DD2} Power Supply Pins

Both V_{DD2} power supply inputs (pins 11 and 16) must be connected to the bus-side power supply. Pin 11 powers the bus side of the CAN I/O circuitry, while pin 16 powers the bus-side isolation circuitry. For testing purposes, they are not internally connected, but the part will not operate without both pins powered, and operation without both pins powered can cause damage.

Power Supply Decoupling

Both V_{DD1} and V_{DD2} must be bypassed with 100 nF ceramic capacitors. These supply the dynamic current required for the isolator switching and should be placed as close as possible to V_{DD} and their respective ground return pins.

Input Configurations

The TxD input should not be left open as the state will be indeterminate. If connected to an open-drain or open collector output, a pull-up resistor (typically 16 kΩ) should be connected from the input to V_{DD1}.

The Mode Select (“S”) input has a nominal 150 kΩ internal pull-down resistor. It can be left open or set low for normal operation.

Dominant Mode Time-out and Failsafe Receiver Functions

CAN bus latch up is prevented by an integrated Dominant mode timeout function. If the TxD pin is forced permanently low by hardware or software application failure, the time-out returns the RxD output to the high state no more than 765 μs after TxD is asserted dominant. The timer is triggered by a negative edge on TxD. If the duration of the low is longer than the internal timer value, the transmitter is disabled, driving the bus to the recessive state. The timer is reset by a positive edge on pin TxD.

If power is lost on V_{DD2}, the IL41050 asserts the RxD output high when the supply voltage falls below 3.8 V. RxD will return to normal operation as soon as V_{DD2} rises above approximately 4.2 V.

Programmable Power-Up

A unique non-volatile programmable power-up feature prevents unstable nodes. A state that needs to be present at node power up can be programmed at the last power down. For example if a CAN node is required to “pulse” dominant at power up, TxD can be sent low by the controller immediately prior to power down. When power is resumed, the node will immediately go dominant allowing self-check code in the microcontroller to verify node operation. If desired, the node can also power up silently by presetting the TxD line high at power down. At the next power on, the IL41050 will remain silent, awaiting a dominant state from the bus.

The microcontroller can check that the CAN node powered down correctly before applying power at the next “power on” request. If the node powered down as intended, RxD will be set high and stored in IL41050’s non-volatile memory. The level stored in the RxD bit can be read before isolated node power is enabled, avoiding possible CAN bus disruption due to an unstable node.

Replacing Non-Isolated Transceivers

The IL41050 is designed to replace common non-isolated CAN transceivers such as the Philips/NXP TJA1050 with minimal circuit changes. Some notable differences:

- Some non-isolated CAN transceivers have internal TxD pull-up resistors, but the IL41050 TxD input should not be left open. If connected to an open-drain or open collector output, a pull-up resistor (typically 16 kΩ) should be connected from the input to V_{DD1}.
- Initialization behavior varies between CAN transceivers. To ensure the desired power-up state, the IL41050 should be initialized with a TxD pulse (low-to-high for recessive initialization), or shut down the transceiver in the desired power-up state (the “programmable power-up feature”).
- Many non-isolated CAN transceivers have a V_{REF} output. Such a reference is available on the IL41050 wide-body version.

The VREF Output

V_{REF} is a reference voltage output used to drive bus threshold comparators in some legacy systems and is provided on the IL41050 wide-body version. The output is half of the bus supply ±10% (*i.e.*, $0.45 V_{DD2} < V_{REF} < 0.55 V_{DD2}$), and can drive up to 50 μA.

IsoRxD / IsoTxD Outputs

The IsoRxD and IsoTxD outputs are isolated versions of the RxD and TxD signals. These outputs are provided on the narrow-body version for troubleshooting, but normally no connections should be made to the pins.

The Isolation Advantage

Battery fire caused by over or under charging of individual lithium ion cells is a major concern in multi-cell high voltage electric and hybrid vehicle batteries. To combat this, each cell is monitored for current flow, cell voltage, and in some advanced batteries, magnetic susceptibility. The IL41050 allows seamless connection of the monitoring electronics of every cell to a common CAN bus by electrically isolating inputs from outputs, effectively isolating each cell from all other cells. Cell status is then monitored via the CAN controller in the Battery Management System (BMS).

Another major advantage of isolation is the tremendous increase in noise immunity it affords the CAN node, even if the power source is a battery. Inductive drives and inverters can produce transient swings in excess of 20 kV/μs. The traditional, non-isolated CAN node provides some protection due to differential signaling and symmetrical driver/receiver pairs, but the IL41050 typically provides more than twice the dV/dt protection of a traditional CAN node.

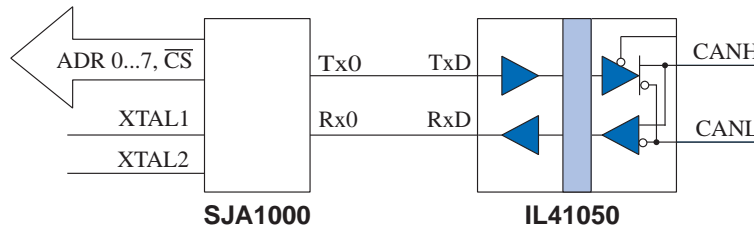
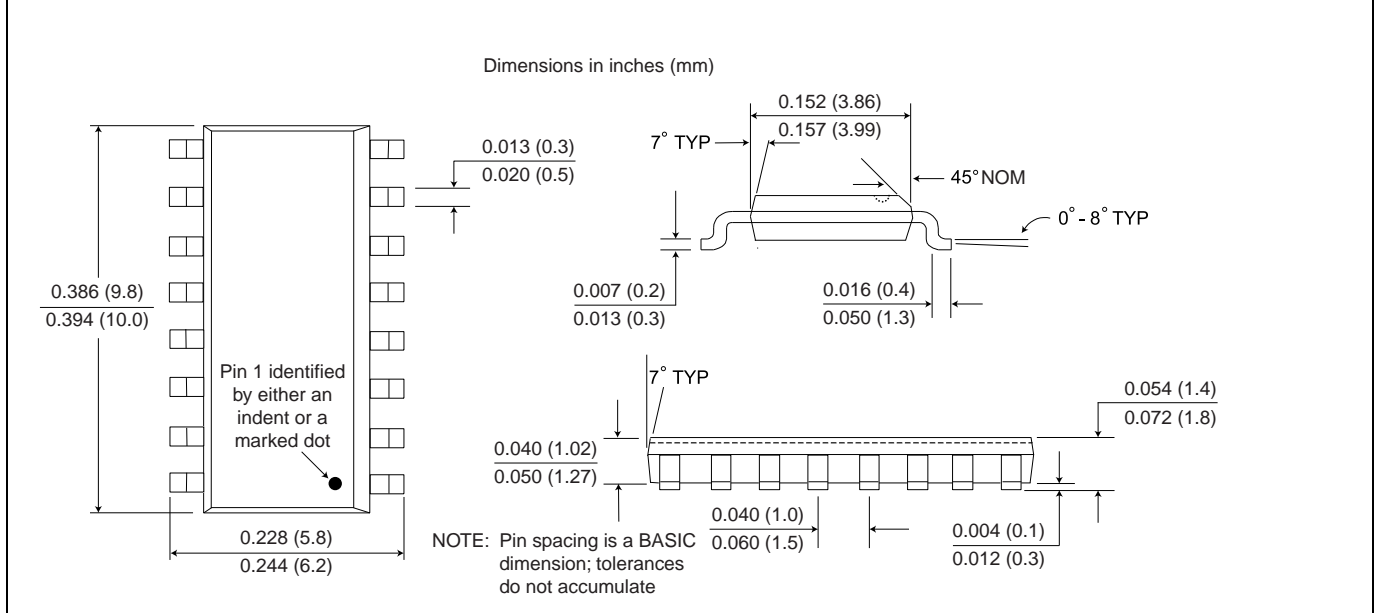


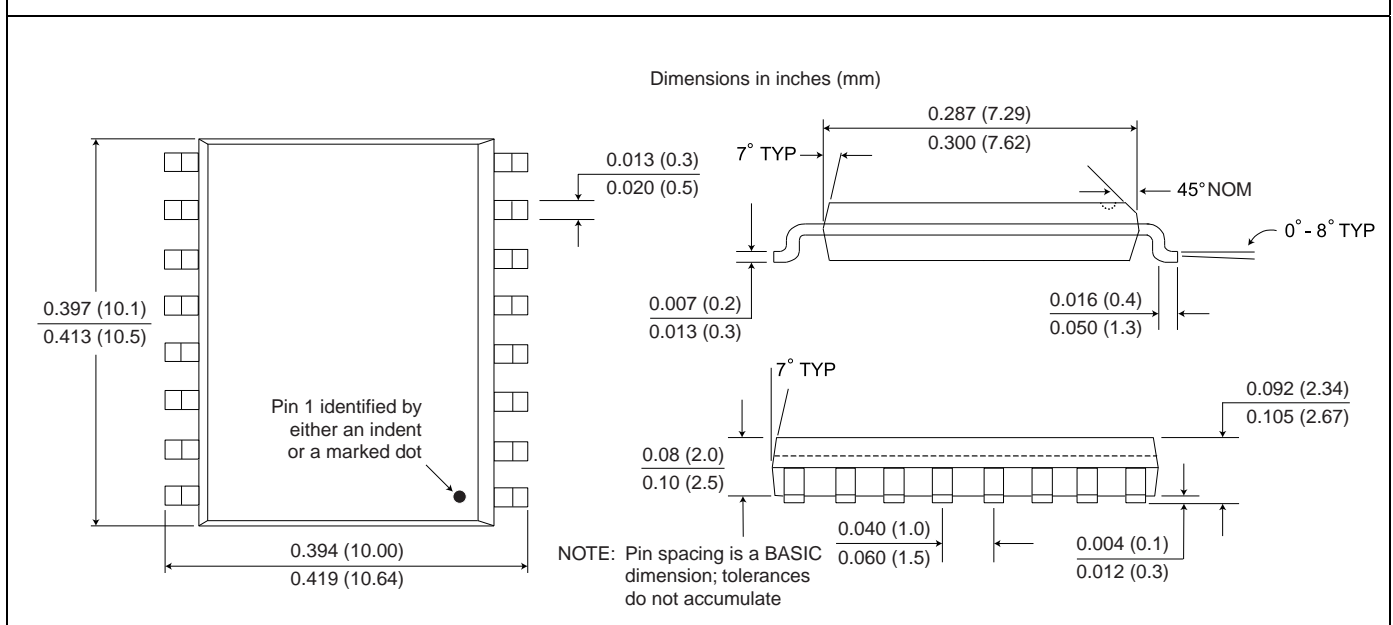
Fig. 2. Isolated CAN node using the IL41050 and an SJA1000 MCU.

Package Drawings, Dimensions and Specifications

0.15" 16-pin SOIC Package

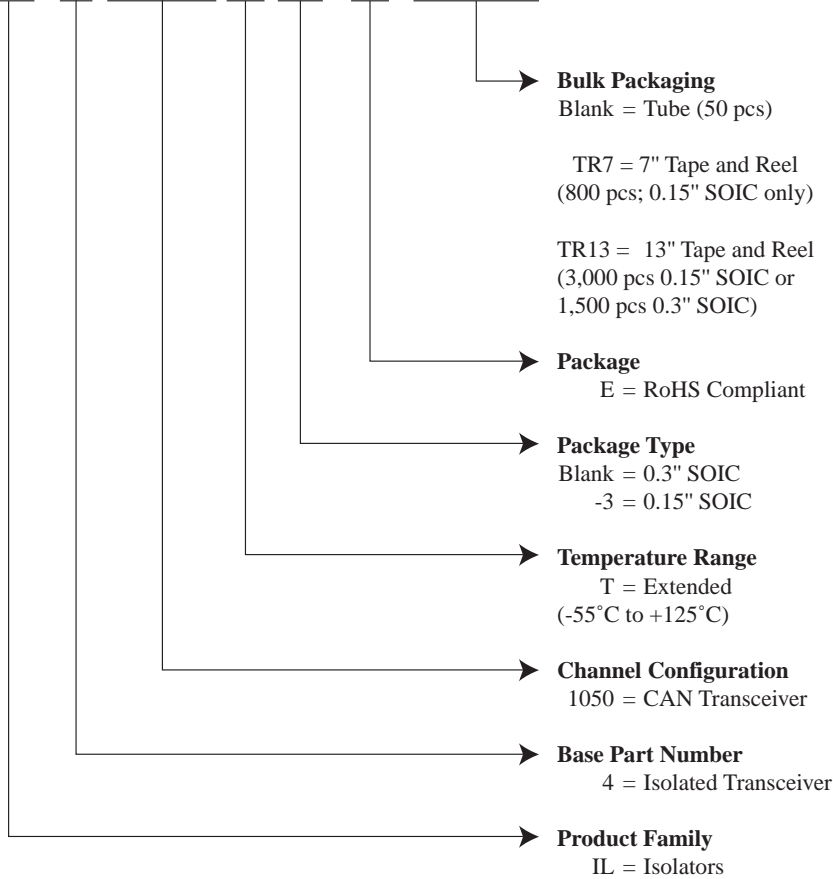


0.3" 16-pin SOIC Package



Ordering Information and Valid Part Numbers

IL 4 1050 T -3 E TR13



Valid Part Numbers

- IL41050TE
- IL41050TE TR13
- IL41050T-3E
- IL41050T-3E TR7
- IL41050T-3E TR13



Revision History**ISB-DS-001-IL41050-J**
February 2012**Changes**

- Update terms and conditions.

ISB-DS-001-IL41050-I
June 2011**Changes**

- Added loop delay specifications (p. 5).

ISB-DS-001-IL41050-H
June 2011**Changes**

- UL approval no longer “pending” (p. 2).
- Clarified V_{DD2} power supply connections with note on pinouts page (p. 3) and new explanatory “Application Information” paragraph (p. 6).

ISB-DS-001-IL41050-G
February 2011**Changes**

- Added “Input Configurations,” “Replacing Non-Isolated Transceivers,” “the VREF Output,” and “IsoRxD/IsoTxD Outputs” Application Information (p. 6).

ISB-DS-001-IL41050-F
April 2010**Changes**

- Added 7-inch tape-and-reel bulk packaging option (TR7) for narrow-body parts (p. 8).

ISB-DS-001-IL41050-E
March 2010**Changes**

- Changed narrow-body pinouts for pins 9, 10, 12, 13, and 14 (p. 3).

ISB-DS-001-IL41050-D
March 2010**Changes**

- Added 0.15" narrow-body SOIC package.
- Added failsafe supply voltage specification and related Note 4.

ISB-DS-001-IL41050-C
February 2010**Changes**

- Extended min. operating temperature to -55°C .
- Misc. changes and clarifications for final release.

ISB-DS-001-IL41050-B
January 2010**Change**

- Clarified TxD edge trigger mode. Added information to Applications section.
- Tightened timing specifications based on qualification data.

ISB-DS-001-IL41050-A
January 2010**Change**

- Initial release.

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An ISO 9001 Certified Company

NVE Corporation
11409 Valley View Road
Eden Prairie, MN 55344-3617 USA
Telephone: (952) 829-9217
Fax: (952) 829-9189
www.nve.com
e-mail: iso-info@nve.com

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