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CY2DP818

1:8 Clock Fanout Buffer

Features

- Low-voltage operation $V_{DD} = 3.3V$
- 1:8 fanout
- Operation to 350 MHz
- Single input configurable for LVDS, LVPECL, or LVTTTL
- 8 pair of LVPECL outputs
- Drives a 50 ohm load
- Low input capacitance
- Low output skew
- Low propagation delay ($t_{pd} = 4$ ns, typical)
- Commercial and Industrial temperature ranges
- 38-Pin TSSOP Package

Description

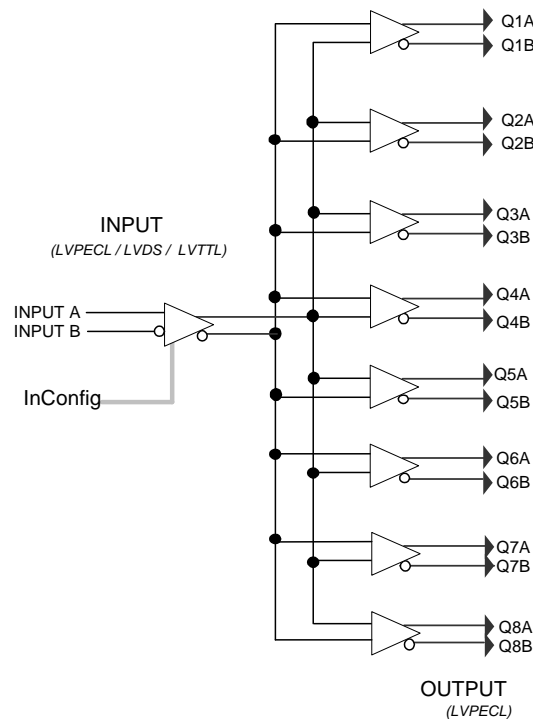
The Cypress CY2DP818 fanout buffer features a single LVDS or a single ended LVTTTL compatible input and eight LVPECL output pairs.

Designed for data-communications clock management applications, the large fanout from a single input reduces loading on the input clock.

The CY2DP818 is ideal for both level translations from single ended to LVPECL and/or for the distribution of LVPECL based clock signals.

The Cypress CY2DP818 has configurable input functions. The input is user configurable via the InConfig pin for single ended or differential input.

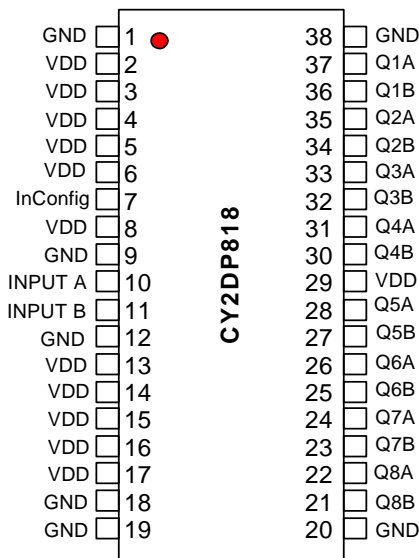
Logic Block Diagram



Pinouts

Pin Configuration

Figure 1. 38-Pin TSSOP



Pin Description

Pin Number	Pin Name	Type	Description
1, 9, 12, 18, 19, 20, 38	GND	POWER	Ground
2, 3, 4, 5, 6, 8, 13, 14, 15, 16, 17, 29	VDD	POWER	Power Supply
10, 11	Input A, Input B	Default: LVPECL/LDVS Optional: LVTTTL/LVCMOS single pin	Clock Input. Either differential LVPECL/LVDS or single-ended LVTTTL/LVCMOS, as determined by InConfig. See Table 1 and Table 2 for details.
37, 36, 35, 34, 33, 32, 31, 30, 28, 27, 26, 25, 24, 23, 22, 21	Q1(A,B), Q2(A,B), Q3(A,B), Q4(A,B), Q5(A,B), Q6(A,B), Q7(A,B), Q8(A,B)	LVPECL	Differential Output Clocks
7	InConfig	LVTTTL/LVCMOS	Control Input. Selects input type: either differential LVPECL/LVDS or single-ended LVTTTL/LVCMOS. See Table 1 and Table 2 for details.

Table 1. Input Receiver Configuration for Differential or LVTTTL/LVCMOS

InConfig (Pin 7)	Input Receiver Family	Input Receiver Type
1	LVTTTL or LVCMOS	Single ended, non-inverting or inverting, void of bias resistors
0	LVDS or LVPECL	Differential, void of internal termination

Table 2. Single ended LVTTTL/LVCMOS Input Logic (InConfig = 1)

Input A (+) Pin 10	Input B (-) Pin 11	Output Clock QnA Pins
Input	Ground	True
Input	VDD	Invert
Ground	Input	Invert
VDD	Input	True



Maximum Ratings^[1]

Storage Temperature:	-65°C to + 150°C	Supply Voltage to Ground Potential (Outputs only)	-0.3V to $V_{DD} + 0.3V$
Ambient Temperature:	-40°C to +85°C	DC Input Voltage	-0.3V to $V_{DD} + 0.3V$
Supply Voltage to Ground Potential (Inputs and V_{DD} only)	-0.3V to 4.6V	DC Output Voltage.....	-0.3V to $V_{DD} + 0.9V$
		Power Dissipation.....	0.75W.

Table 3. Power Supply Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
ICC	Dynamic Power Supply Current	$V_{DD} = \text{Max}$ Input toggling 50% Duty Cycle, Outputs Open		1.5	2.0	mA/ MHz
IC	Total Power Supply Current	$V_{DD} = \text{Max}$ Input toggling 50% Duty Cycle, Outputs 50 ohms $f_L = 100 \text{ MHz}$			350	mA
IC Core	Core current when output loads are disabled	$V_{DD} = \text{Max}$ Input toggling 50% Duty Cycle, Outputs not connected to VTT $f_L = 100 \text{ MHz}$			50	mA

DC Electrical Specifications

Table 4. LVDS Input, $V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ\text{C}$ to 70°C or -40°C to 85°C

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{ID}	Magnitude of Differential Input Voltage		100		600	mV
V_{IC}	Common-mode of Differential Input Voltage $ V_{ID} $ (min and max)		$ V_{ID} /2$	$2.4 - (V_{ID} /2)$		V
V_{IH}	Input High Voltage	Guaranteed Logic High Level	2			V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level			0.8	V
I_{IH}	Input High Current	$V_{DD} = \text{Max}$, $V_{IN} = V_{DD}$		± 10	± 20	μA
I_{IL}	Input Low Current	$V_{DD} = \text{Max}$, $V_{IN} = V_{SS}$		± 10	± 20	μA

Table 5. LVPECL Input, $V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ\text{C}$ to 70°C or -40°C to 85°C

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{ID}	Differential Input Voltage p-p	Guaranteed Logic High Level	400		2600	mV
V_{IH}	Input High Voltage	Guaranteed Logic High Level	2.15		2.4	V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level	1.5		1.8	V
I_{IH}	Input High Current	$V_{DD} = \text{Max}$, $V_{IN} = V_{DD}$		± 10	± 20	μA
I_{IL}	Input Low Current	$V_{DD} = \text{Max}$, $V_{IN} = V_{SS}$		± 10	± 20	μA
V_{CM}	Common-mode Voltage				225	mV

Table 6. LVTTTL/LVCMOS Input, $V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ\text{C}$ to 70°C or -40°C to 85°C

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Input High Voltage		2			V
V_{IL}	Input Low Voltage				0.8	V
I_{IH}	Input High Current	$V_{DD} = \text{Max}$, $V_{IN} = 2.7V$			1	μA
I_{IL}	Input Low Current	$V_{DD} = \text{Max}$, $V_{IN} = 0.5V$			-1	μA

Note

- Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 6. LVTTTL/LVCMOS Input, $V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$ or $-40^\circ C$ to $85^\circ C$

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_I	Input High Current	$V_{DD} = \text{Max}$, $V_{IN} = V_{DD}(\text{Max})$			20	μA
V_{IK}	Clamp Diode Voltage	$V_{DD} = \text{Min}$, $I_{IN} = -18\text{mA}$		-0.7	-1.2	V
V_H	Input Hysteresis			80		mV

Table 7. LVPECL Output, $V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$ or $-40^\circ C$ to $85^\circ C$

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{OD}	Driver Differential Output voltage p-p	$V_{DD} = \text{Min}$, $V_{IN} = V_{IH}$ or V_{IL} , $R_L = 50 \Omega$	1000		3600	mV
V_{OC}	Driver common-mode p-p	$V_{DD} = \text{Min}$, $V_{IN} = V_{IH}$ or V_{IL} , $R_L = 50 \Omega$			300	mV
t_R	Rise Time	Differential 20% to 80%, $C_L = 10 \text{ pF}$ to GND, $R_L = 50 \Omega$ to GND	300		1200	ps
t_F	Fall Time					
V_{OH}	Output High Voltage	$V_{DD} = \text{Min}$, $V_{IN} = V_{IH}$ or V_{IL} , $I_{OH} = -12 \text{ mA}$	2.1		3.0	V
$V_{OL}^{[2]}$	Output Low Voltage	$V_{DD} = \text{Min}$, $V_{IN} = V_{IH}$ or V_{IL}	0.8		1.3	V
I_{OS}	Short Circuit Current	$V_{DD} = \text{Max}$, $V_{OUT} = \text{GND}$	-125		-150	mA

AC Switching Characteristics

Table 8. $V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$ or $-40^\circ C$ to $85^\circ C$

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay – Low to High	$V_{ID} = 100 \text{ mV}$	3	4	5	ns
t_{PHL}	Propagation Delay – High to Low	$V_{ID} = 100 \text{ mV}$	3	4	5	ns
$t_{SK(0)}$	Output Skew: Skew between outputs of the same package (in phase)				0.2	ns
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output ($t_{PHL} - t_{PLH}$)			0.2		ns
$t_{SK(t)}$	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type. Same input signal level and output load.	$V_{ID} = 100 \text{ mV}$			1	ns

Table 9. High frequency Parametrics

Parameter	Description	Conditions	Min	Typ	Max	Unit
F_{max}	Maximum frequency $V_{DD} = 3.3V$	45%–55% duty cycle Standard load circuit			350	MHz

Note

2. V_{OL} levels are dependent on the termination voltage V_{TT} and termination resistance R_{TT} . Changing either of these values will affect V_{OL} .

Figure 2. Driver Design

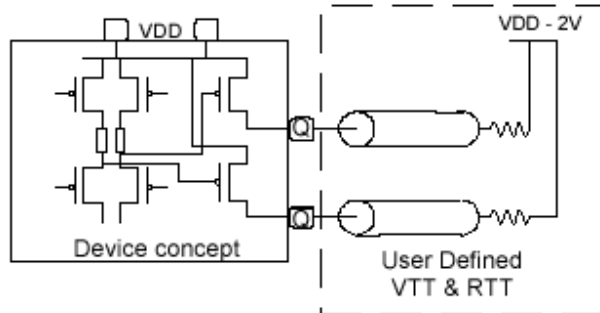


Figure 3. Standard Termination

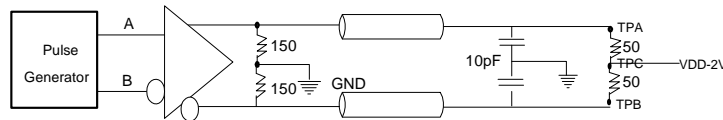


Figure 4. Differential Receiver to Driver Propagation Delay and Driver Transition Time^[3,4,5,6]

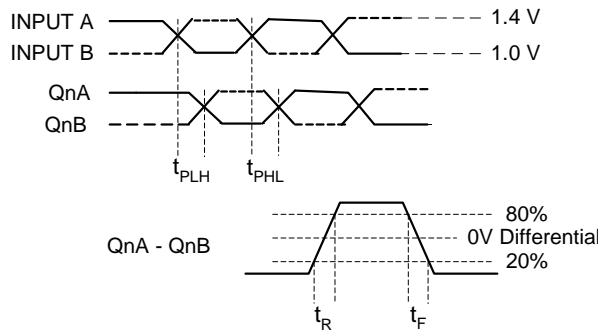
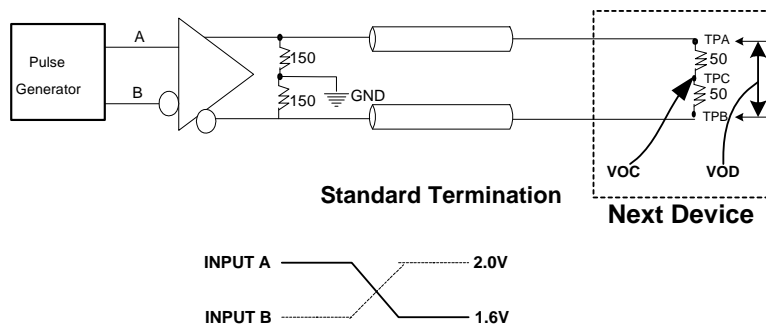


Figure 5. Test Circuit and Voltage Definitions for the Driver Common Mode Output Voltage^[3,4,5,6]



Notes

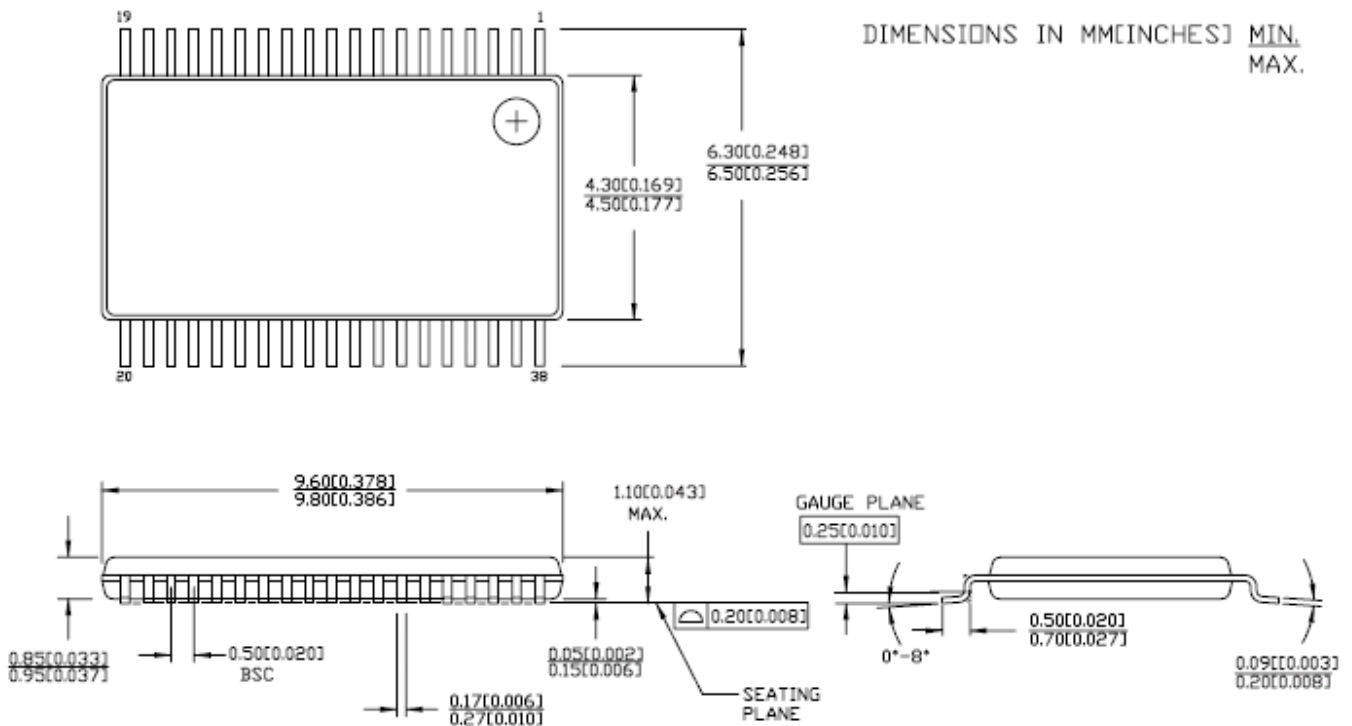
3. All input pulses are supplied by a frequency generator with the following characteristics: t_R and $t_F \leq 1$ ns; pulse rate = 50 Mpps; pulse width = 10 ± 0.2 ns.
4. $R_L = 50 \text{ ohm} \pm 1\%$; $Z_{line} = 50 \text{ ohm} \pm 6\%$.
5. CL includes instrumentation and fixture capacitance within 6 mm of the UT.
6. TPA and B are used for prop delay and Rise/Fall measurements. TPC is used for VOC measurements only and is otherwise connected to $V_{DD} - 2V$.

Ordering Information

Part Number	Package Type	Product Flow
CY2DP818ZI	38-pin TSSOP	Industrial, -40° to 85°C
CY2DP818ZIT	38-pin TSSOP–Tape and Reel	Industrial, -40° to 85°C
CY2DP818ZC	38-pin TSSOP	Commercial, 0°C to 70°C
CY2DP818ZCT	38-pin TSSOP–Tape and Reel	Commercial, 0°C to 70°C
Pb-Free		
CY2DP818ZXI	38-pin TSSOP	Industrial, -40° to 85°C
CY2DP818ZXIT	38-pin TSSOP–Tape and Reel	Industrial, -40° to 85°C
CY2DP818ZXC	38-pin TSSOP	Commercial, 0°C to 70°C
CY2DP818ZXCT	38-pin TSSOP–Tape and Reel	Commercial, 0°C to 70°C

Package Drawing and Dimensions

Figure 6. 38-Pin TSSOP (4.40 mm Body) Z38 and ZZ38



51-85151-*A



Document History Page

Document Title: CY2DP818 1:8 Clock Fanout Buffer Document Number: 38-07061				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	107086	06/07/01	IKA	New Data Sheet
*A	115913	07/11/02	CTK	IC, VCM, VOC, Rise/Fall Time Fmax (20)
*B	2748606	08/05/09	KVM	Deleted references to ComLink Minor edits to page 1 text Instances of VCC changed to VDD Changed table sequence to be more logical Edited Table 1 on page 2 and reformatted Table 2 on page 2 for clarity Added voltage and temperature specs to heading of all DC and AC tables Added commercial temp range to DC and AC table headings Clarified wording for IC Core Removed duplicate I _I (input high current) parameter from LVPECL & LVDS Removed T _{PE} and T _{PD} parameters from AC table Cleaned up waveform drawings Removed figures showing inputs for different InConfig values because Table 1 on page 2 and Table 2 on page 2 are more complete Added part numbers CY2DP818ZXC, CY2DP818ZXCT, CY2DP818ZXI and CY2DP818ZXIT to the ordering information table Revised Package Diagram

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