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## DG508B, DG509B

Vishay Siliconix

# Precision 8-Channel / Dual 4-Channel CMOS Analog Multiplexers

### DESCRIPTION

The DG508B is an 8-channel single-ended analog multiplexer designed to connect one of eight inputs to a common output as determined by a 3-bit binary address ( $A_0$ ,  $A_1$ ,  $A_2$ ). The DG509B is a dual 4-channel differential analog multiplexer designed to connect one of four differential inputs to a common dual output as determined by its 2-bit binary address ( $A_0$ ,  $A_1$ ). Break-before-make switching action protects against momentary crosstalk between adjacent channels.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer / demultiplexer to all switches off for stacking several devices. All control inputs, addresses ( $A_x$ ) and enable (EN) are TTL compatible over the full specified operating temperature range.

The DG508B and DG509B are fabricated on an enhanced SG-II CMOS process that achieves improved performance on: reduced charge injection, lower device leakage, and minimized parasitic capacitance.

As the DG508, DG509 has a long history in the industry with many suppliers offering copies - and in some cases improved variations - with the best in class improvements, the Vishay Siliconix new version of the DG508B, DG509B are the superior alternatives to what is currently available.

Applications for the DG508B, DG509B include high speed and high precision data acquisition, audio signal switching and routing, ATE systems, and avionics. High performance and low power dissipation make them ideal for battery operated and remote instrumentation applications.

The DG508B and DG509B have the absolute maximum voltage rating extended to 44 V. Additionally, single supply operation is also allowed. An epitaxial layer prevents latch-up.

The DG508B and DG509B are both available in 16-lead SOIC, TSSOP, PDIP, and miniQFN (1.8 mm x 2.6 mm) package options with extended temperature range of -40 °C to +125 °C.

For more information, refer to Vishay Siliconix DG508B, DG509B evaluation board note.

### FEATURES

- Operate with single or dual power supply
- V+ to V- analog signal swing range
- 44 V power supply maximum rating
- Extended operate temperature range: -40 °C to +125 °C
- Low leakage typically < 3 pA
- Low charge injection -  $Q_{INJ} = 2$  pC
- Low power -  $I_{SUPPLY} = 10$   $\mu$ A
- TTL compatible logic
- > 250 mA latch-up current per JESD78
- Available in SOIC16, TSSOP16, PDIP, and miniQFN16 packages
- Superior alternative to:
  - ADG508A, DG508A, HI-508
  - ADG509A, DG509A, HI-509
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



RoHS  
 COMPLIANT  
 HALOGEN  
 FREE

### BENEFITS

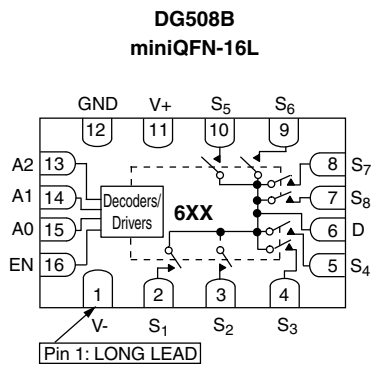
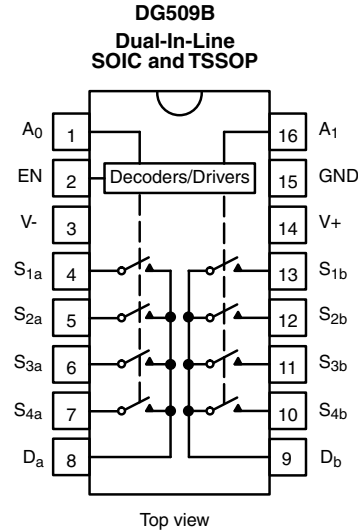
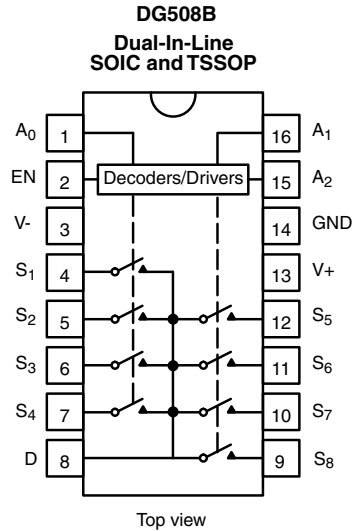
- Reduced switching errors
- Reduced glitching
- Improved data throughput
- Reduced power consumption
- Increased ruggedness
- Wide supply ranges ( $\pm 5$  V to  $\pm 20$  V)

### APPLICATIONS

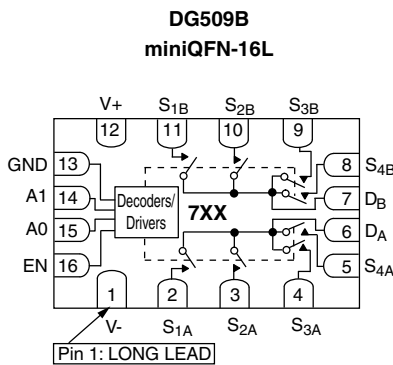
- Data acquisition systems
- Audio and video signal routing
- ATE systems
- Medical instrumentation



**FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION**



Device Marking: **6XX**  
 Traceability Code:  
 6 is DG508BEN  
 XX = Date/Lot



Device Marking: **7XX**  
 Traceability Code:  
 7 is DG509BEN  
 XX = Date/Lot

**TRUTH TABLES AND ORDERING INFORMATION**

TRUTH TABLE (DG508B)				
A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	ON SWITCH
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TRUTH TABLE (DG509B)			
A <sub>1</sub>	A <sub>0</sub>	EN	ON SWITCH
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" = V<sub>IL</sub> ≤ 0.8 V  
 Logic "1" = V<sub>IH</sub> ≥ 2 V  
 X = Do not care



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## DG508B, DG509B

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ORDERING INFORMATION (DG508B)		
TEMP. RANGE	PACKAGE	PART NUMBER
-40 °C to +125 °C <sup>a</sup>	16-Pin SOIC	DG508BEY-T1-E3
	16-Pin TSSOP	DG508BEQ-T1-E3
	16-Pin PDIP	DG508BEJ-E3
	16-Pin MiniQFN	DG508BEN-T1-GE4

ORDERING INFORMATION (DG509B)		
TEMP. RANGE	PACKAGE	PART NUMBER
-40 °C to +125 °C <sup>a</sup>	16-Pin SOIC	DG509BEY-T1-E3
	16-Pin TSSOP	DG509BEQ-T1-E3
	16-Pin PDIP	DG509BEJ-E3
	16-Pin MiniQFN	DG509BEN-T1-GE4

**Note**

a. -40 °C to +85 °C datasheet limits apply.

ABSOLUTE MAXIMUM RATINGS			
PARAMETER		LIMIT	UNIT
Voltages Referenced to V-	V+	44	V
	GND	25	
Digital Inputs <sup>a</sup> , V <sub>S</sub> , V <sub>D</sub>		(V-) - 2 to (V+) + 2 or 20 mA, whichever occurs first	
Current (Any terminal)		30	mA
Peak Current, S or D (Pulsed at 1 ms, 10 % duty cycle max.)		100	
Storage Temperature	(EY, EQ, EJ, EN suffix)	-65 to +150	°C
Power Dissipation (Packages) <sup>b</sup>	16-Pin Narrow SOIC <sup>c</sup>	600	mW
	16-Pin TSSOP <sup>d</sup>	450	
	16-Pin PDIP <sup>e</sup>	510	
	16-Pin miniQFN <sup>f</sup>	525	
Thermal Resistance (θJA) <sup>b</sup>	16-Pin Narrow SOIC <sup>c</sup>	125	°C/W
	16-Pin TSSOP <sup>d</sup>	178	
	16-Pin PDIP <sup>e</sup>	159.6	
	16-Pin miniQFN <sup>f</sup>	152	

**Notes**

- a. Signals on SX, DX or INX exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads soldered or welded to PC board.
- c. Derate 8 mW/°C above 70 °C.
- d. Derate 5.6 mW/°C above 70 °C.
- e. Derate 6.3 mW/°C above 70 °C.
- f. Derate 6.6 mW/°C above 70 °C.



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## DG508B, DG509B

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SPECIFICATIONS										
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED $V_+ = 15\text{ V}$ , $V_- = -15\text{ V}$ ( $\pm 10\%$ ) $V_{AX}$ , $V_{EN} = 2\text{ V}$ , $0.8\text{ V}^a$	TEMP. <sup>b</sup>	TYP. <sup>c</sup>	-40 °C to +125 °C		-40 °C to +85 °C		UNIT	
					MIN. <sup>d</sup>	MAX. <sup>d</sup>	MIN. <sup>d</sup>	MAX. <sup>d</sup>		
<b>Analog Switch</b>										
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full	-	-15	15	-15	15	V	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_D = \pm 10\text{ V}$ , $I_S = -1\text{ mA}$	Room	180	-	380	-	380	$\Omega$	
			Full	-	-	480	-	450		
$R_{DS(on)}$ Matching	$\Delta R_{DS(on)}$	$V_D = \pm 10\text{ V}$	Room	10	-	-	-	-		
Source Off Leakage Current	$I_{S(off)}$	$V_D = \pm 10\text{ V}$ $V_S = \mp 10\text{ V}$ $V_{EN} = 0\text{ V}$	Room	-	-1	1	-1	1	nA	
Drain Off Leakage Current	$I_{D(off)}$		DG508B	Full	-	-50	50	-50		50
				Room	-	-1	1	-1		1
			DG509B	Room	-	-1	1	-1		1
				Full	-	-50	50	-50		50
Drain On Leakage Current	$I_{D(on)}$		DG508B	Room	-	-1	1	-1		1
				Full	-	-100	100	-100		100
			DG509B	Room	-	-1	1	-1		1
		Full		-	-50	50	-50	50		
<b>Digital Control</b>										
Logic High Input Voltage	$V_{INH}$		Full	-	2	-	2	-	V	
Logic Low Input Voltage	$V_{INL}$		Full	-	-	0.8	-	0.8		
Logic High Input Current	$I_{IH}$	$V_{AX}$ , $V_{EN} = 2\text{ V}$	Full	-	-1	1	-1	1	$\mu\text{A}$	
Logic Low Input Current	$I_{IL}$	$V_{AX}$ , $V_{EN} = 0.8\text{ V}$	Full	-	-1	1	-1	1		
Logic Input Capacitance <sup>e</sup>	$C_{IN}$	$f = 1\text{ MHz}$	Room	4	-	-	-	-	pF	
<b>Dynamic Characteristics</b>										
Transition Time	$t_{TRANS}$	$V_{S1} = +10\text{ V}/-10\text{ V}$ , $V_{S8} = -10\text{ V}/+10\text{ V}$ , $R_L = 1\text{ M}\Omega$ , $C_L = 35\text{ pF}$	Room	145	-	300	-	300		
			Full	-	-	400	-	400		
Break-Before-Make Interval	$t_{OPEN}$	$V_{S1} = V_{S8} = 5\text{ V}$ , $C_L = 35\text{ pF}$ , $R_L = 1\text{ k}\Omega$	Room	37	15	-	15	-	ns	
			Full	-	1	-	1	-		
Enable Turn-On Time	$t_{ON(EN)}$	$V_{S1} = 5\text{ V}$ , $V_{S2}$ to $V_{S8} = 0\text{ V}$ , $R_L = 1\text{ k}\Omega$ , $C_L = 35\text{ pF}$	Room	100	-	250	-	250		
			Full	-	-	340	-	340		
Enable Turn-Off Time	$t_{OFF(EN)}$		Room	90	-	240	-	240		
			Full	-	-	300	-	300		
Charge Injection <sup>e</sup>	$Q_{INJ}$	$C_L = 1\text{ nF}$ , $R_{GEN} = 0\text{ W}$ , $V_{GEN} = 0\text{ V}$	Full	2	-	-	-	-	pC	
Off Isolation <sup>e</sup>	OIRR	$C_L = 5\text{ pF}$ , $R_L = 50\text{ }\Omega$ , $f = 1\text{ MHz}$	Room	-81	-	-	-	-	dB	
Crosstalk <sup>e</sup>	$X_{TALK}$		Room	-88	-	-	-	-		
-3 dB Bandwidth <sup>e</sup>	BW	$R_L = 50\text{ }\Omega$	Room	250	-	-	-	-	MHz	
Total Harmonic Distortion <sup>e</sup>	THD	$R_L = 10\text{ k}\Omega$ , $5\text{ V}_{rms}$ $f = 20\text{ Hz}$ to $20\text{ kHz}$	Room	0.04	-	-	-	-	%	
Source Off Capacitance <sup>e</sup>	$C_{S(off)}$	$f = 1\text{ MHz}$	Room	3	-	-	-	-	pF	
Drain Off Capacitance <sup>e</sup>	$C_{D(off)}$		DG508B	Room	13	-	-	-		-
			DG509B	Room	8	-	-	-		-
Drain On Capacitance <sup>e</sup>	$C_{D(on)}$		DG508B	Room	18	-	-	-		-
			DG509B	Room	11	-	-	-		-
<b>Power Supply</b>										
Positive Supply Current	I+	$V_{AX}$ , $V_{EN} = 0.8\text{ V}$ or $2.4\text{ V}$	Room	0.01	-	0.2	-	0.2	mA	
			Full	-	-	0.3	-	0.3		
Negative Supply Current	I-		Full	0.06	-10	-	-10	-	$\mu\text{A}$	



SPECIFICATIONS (Single Supply 12 V)										
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V <sub>+</sub> = 12 V, V <sub>-</sub> = 0 V (± 10 %) V <sub>AX</sub> , V <sub>EN</sub> = 2 V, 0.8 V <sup>a</sup>	TEMP. <sup>b</sup>	TYP. <sup>c</sup>	-40 °C to +125 °C		-40 °C to +85 °C		UNIT	
					MIN. <sup>d</sup>	MAX. <sup>d</sup>	MIN. <sup>d</sup>	MAX. <sup>d</sup>		
<b>Analog Switch</b>										
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full	-	0	12	0	12	V	
On-Resistance	R <sub>DS(on)</sub>	V <sub>D</sub> = 10 V/0 V, I <sub>S</sub> = 1 mA	Room	265	-	500	-	500	Ω	
R <sub>DS(on)</sub> Matching	ΔR <sub>DS(on)</sub>		Full	-	-	650	-	600		
Switch Off Leakage Current	I <sub>S(off)</sub>	V <sub>+</sub> = 12 V, V <sub>-</sub> = 0 V V <sub>D</sub> = 0 V/10 V, V <sub>S</sub> = 10 V/0 V	Room	-	-1	1	-1	1	nA	
			Full	-	-50	-50	-50	50		
	I <sub>D(off)</sub>		DG508B	Room	-	-1	1	-1		1
			DG508B	Full	-	-100	100	-100		100
	I <sub>D(off)</sub>		DG509B	Room	-	-1	1	-1		1
			DG509B	Full	-	-50	50	-50		50
Channel On Leakage Current	I <sub>D(on)</sub>	DG508B	Room	-	-1	1	-1	1	nA	
		DG508B	Full	-	-100	100	-100	100		
		DG509B	Room	-	-1	1	-1	1		
		DG509B	Full	-	-50	50	-50	50		
<b>Digital Control</b>										
Logic High Input Voltage	V <sub>INH</sub>		Full	-	2	-	2	-	V	
Logic Low Input Voltage	V <sub>INL</sub>		Full	-	-	0.8	-	0.8		
Logic High Input Current	I <sub>IH</sub>	V <sub>AX</sub> , V <sub>EN</sub> = 2 V	Full	-	-1	1	-1	1	μA	
Logic Low Input Current	I <sub>IL</sub>	V <sub>AX</sub> , V <sub>EN</sub> = 0.8 V	Full	-	-1	1	-1	1		
Logic Input Capacitance <sup>e</sup>	C <sub>IN</sub>	f = 1 MHz	Room	4	-	-	-	-	pF	
<b>Dynamic Characteristics</b>										
Transition Time	t <sub>TRANS</sub>	V <sub>S1</sub> = 10 V/0 V, V <sub>S8</sub> = 0 V/10 V, R <sub>L</sub> = 1 MΩ, C <sub>L</sub> = 35 pF	Room	165	-	400	-	400	ns	
			Full	-	-	550	-	500		
Break-Before-Make Interval	t <sub>OPEN</sub>	V <sub>S1</sub> = V <sub>S8</sub> = 5 V, C <sub>L</sub> = 35 pF, R <sub>L</sub> = 1 kΩ	Room	37	15	-	15	-		
			Full	-	1	-	1	-		
Enable Turn-On Time	t <sub>ON(EN)</sub>	V <sub>S1</sub> = 5 V, V <sub>S2</sub> to V <sub>S8</sub> = 0 V, R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 35 pF	Room	125	-	300	-	300		
			Full	-	-	550	-	425		
Enable Turn-Off Time	t <sub>OFF(EN)</sub>		Room	75	-	250	-	250		
			Full	-	-	350	-	300		
Charge Injection <sup>e</sup>	Q <sub>INJ</sub>		C <sub>L</sub> = 1 nF, R <sub>GEN</sub> = 0 Ω, V <sub>GEN</sub> = 0 V	Full	2.5	-	-	-	pC	
Off Isolation <sup>e</sup>	OIRR		C <sub>L</sub> = 5 pF, R <sub>L</sub> = 50 Ω f = 1 MHz	Room	-80	-	-	-	-	dB
Crosstalk <sup>e</sup>	X <sub>TALK</sub>	Room		-88	-	-	-	-		
-3 dB Bandwidth <sup>e</sup>	BW	R <sub>L</sub> = 50 Ω	Room	200	-	-	-	-	MHz	
Total Harmonic Distortion <sup>e</sup>	THD	R <sub>L</sub> = 10 kΩ, 5 V <sub>RMS</sub> , f = 20 Hz to 20 kHz	Room	0.26	-	-	-	-	%	
Source Off Capacitance <sup>e</sup>	C <sub>S(off)</sub>	f = 1 MHz	Room	2	-	-	-	-	pF	
Drain Off Capacitance <sup>e</sup>	C <sub>D(off)</sub>			DG508B	13	-	-	-		-
				DG509B	8	-	-	-		-
Channel On Capacitance <sup>e</sup>	C <sub>D(on)</sub>			DG508B	17	-	-	-		-
				DG509B	12	-	-	-		-



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**DG508B, DG509B**

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SPECIFICATIONS (Single Supply 12 V)									
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED $V_+ = 12\text{ V}, V_- = 0\text{ V} (\pm 10\%)$ $V_{AX}, V_{EN} = 2\text{ V}, 0.8\text{ V}^a$	TEMP. <sup>b</sup>	TYP. <sup>c</sup>	-40 °C to +125 °C		-40 °C to +85 °C		UNIT
					MIN. <sup>d</sup>	MAX. <sup>d</sup>	MIN. <sup>d</sup>	MAX. <sup>d</sup>	
<b>Power Supply</b>									
Positive Supply Current	I+	$V_{AX}, V_{EN} = 0.8\text{ V or }2.4\text{ V}$	Room	0.01	-	0.2	-	0.2	mA
			Full	-	-	0.3	-	0.3	

**Notes**

- a.  $V_{AX}, V_{EN}$  = input voltage perform proper function.
- b. Room = 25 °C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
- e. Guaranteed by design, not subject to production test.
- f.  $\Delta R_{DS(on)} = R_{DS(on)} \text{ max.} - R_{DS(on)} \text{ min.}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**SCHEMATIC DIAGRAM (Typical Channel)**

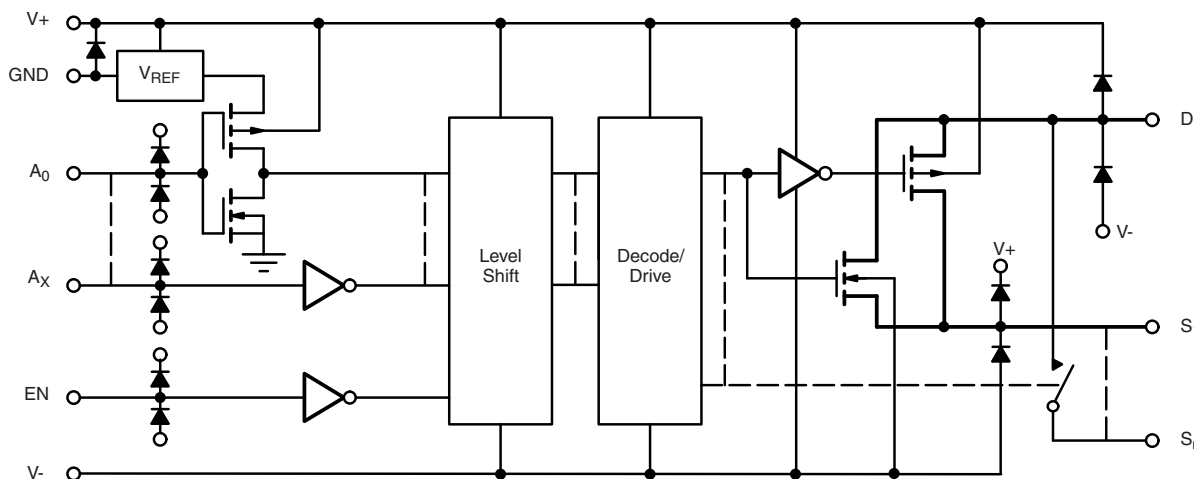


Fig. 1

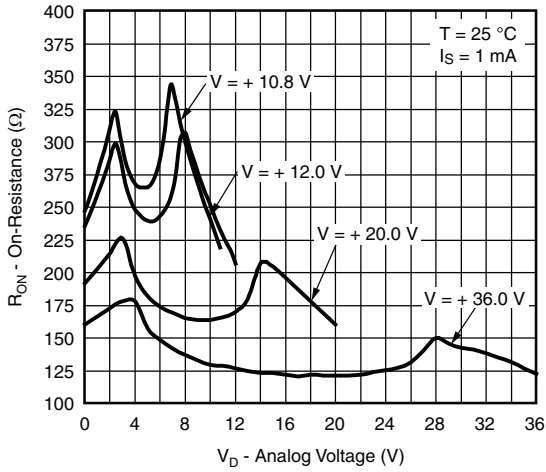


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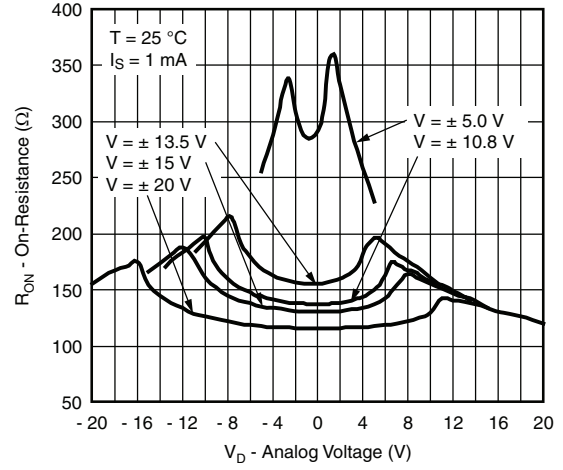
**DG508B, DG509B**

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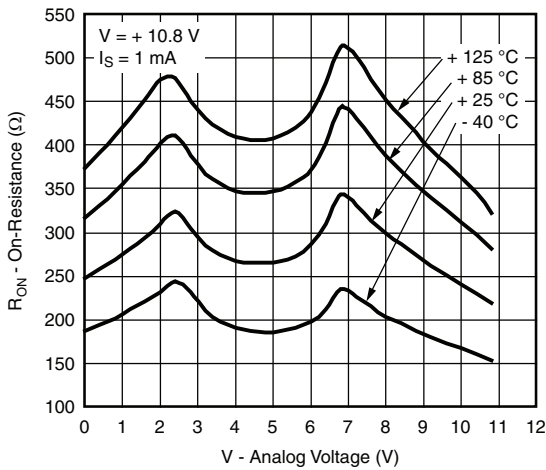
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



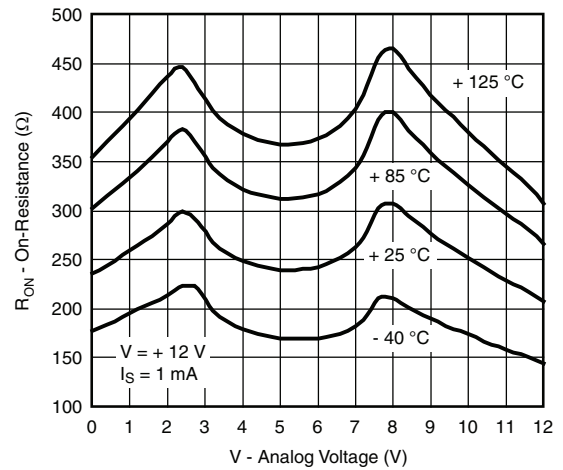
**On-Resistance vs.  $V_D$  and Single Supply Voltage**



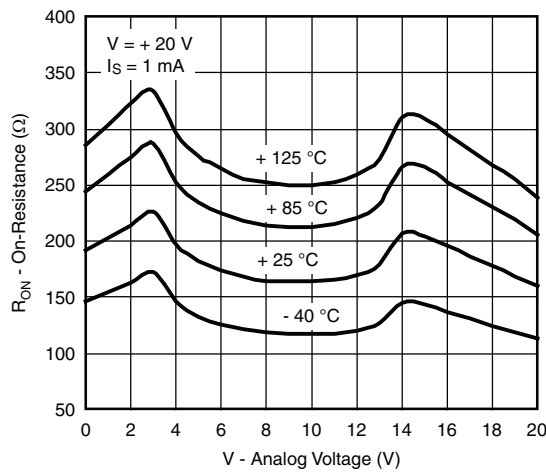
**On-Resistance vs.  $V_D$  and Dual Supply Voltage**



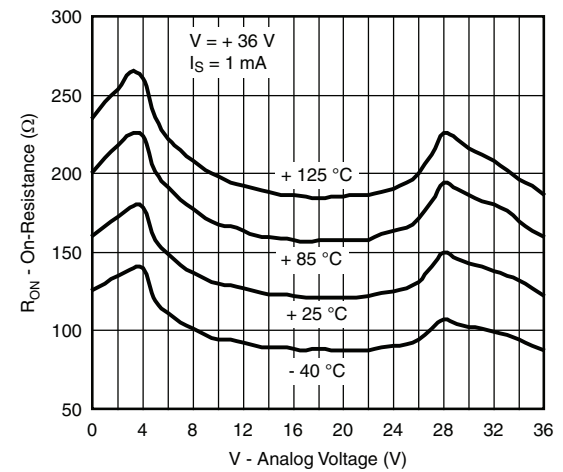
**On-Resistance vs. Analog Voltage and Temperature**



**On-Resistance vs. Analog Voltage and Temperature**



**On-Resistance vs. Analog Voltage and Temperature**



**On-Resistance vs. Analog Voltage and Temperature**



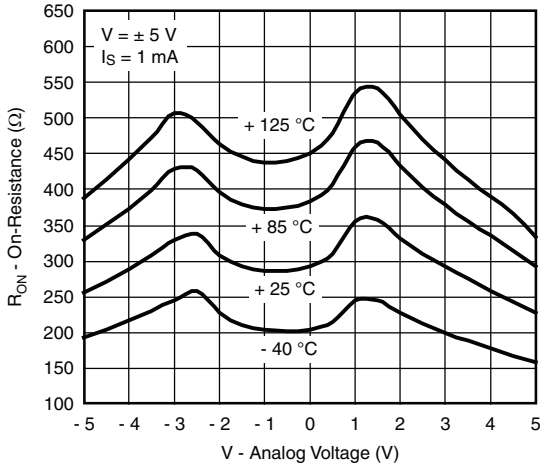


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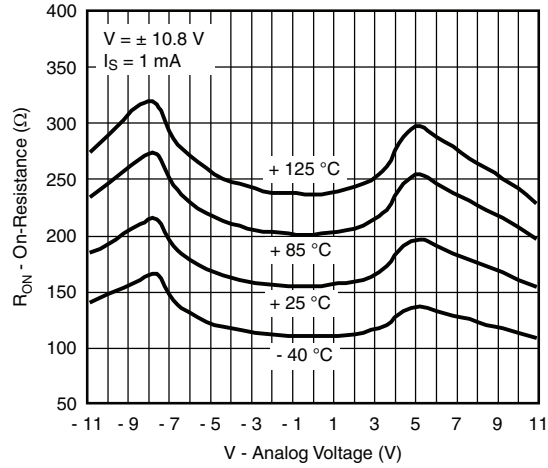
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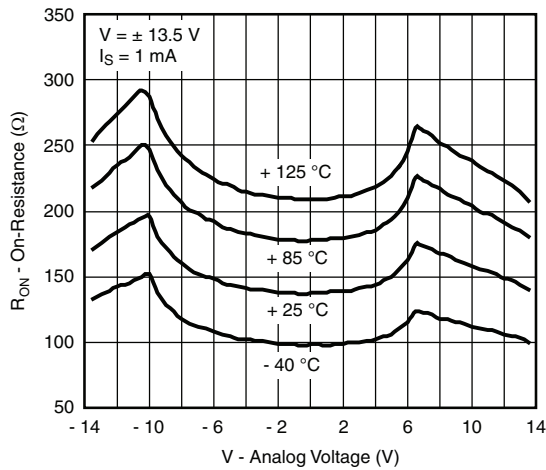
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



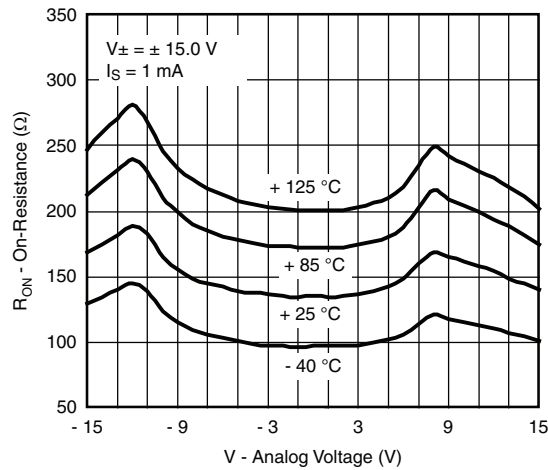
**On-Resistance vs. Analog Voltage and Temperature**



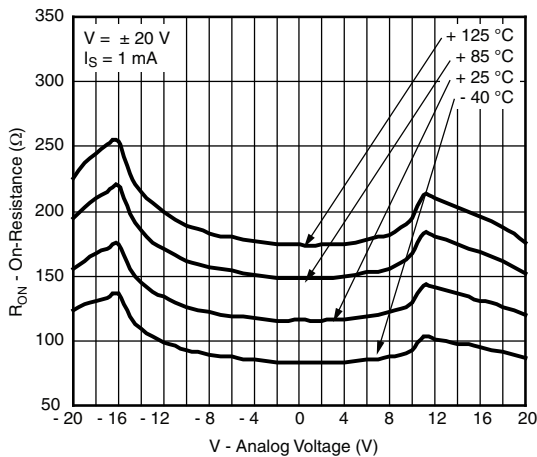
**On-Resistance vs. Analog Voltage and Temperature**



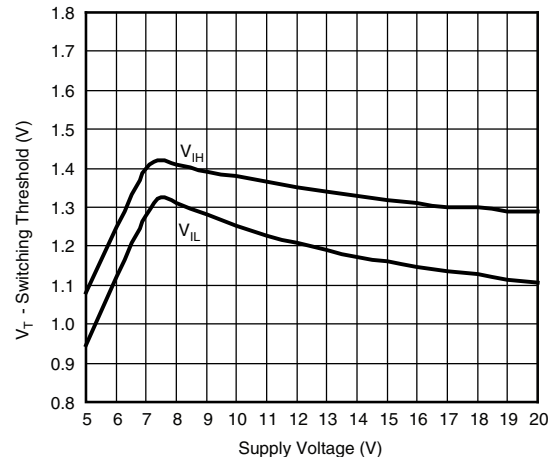
**On-Resistance vs. Analog Voltage and Temperature**



**On-Resistance vs. Analog Voltage and Temperature**



**On-Resistance vs. Analog Voltage and Temperature**



**Switching Threshold vs. Supply Voltage**

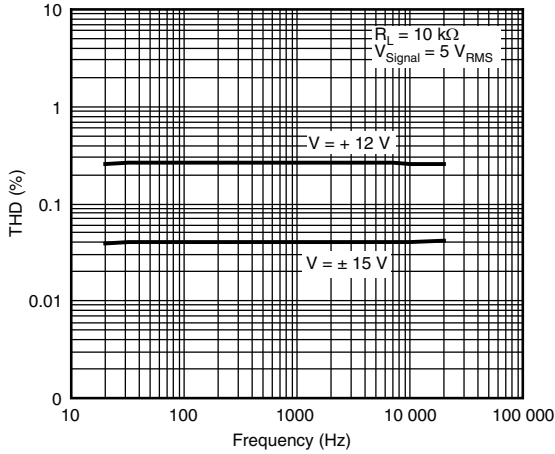


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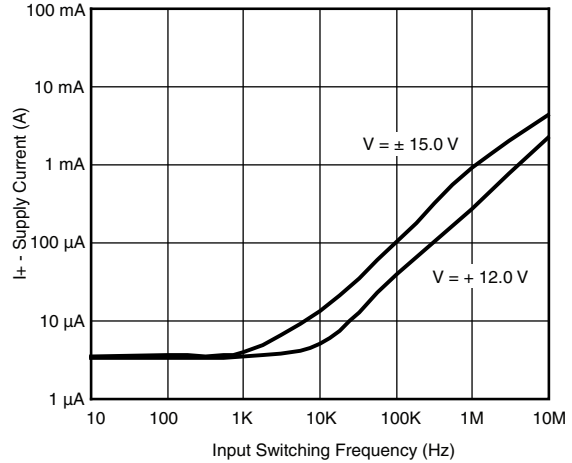
**DG508B, DG509B**

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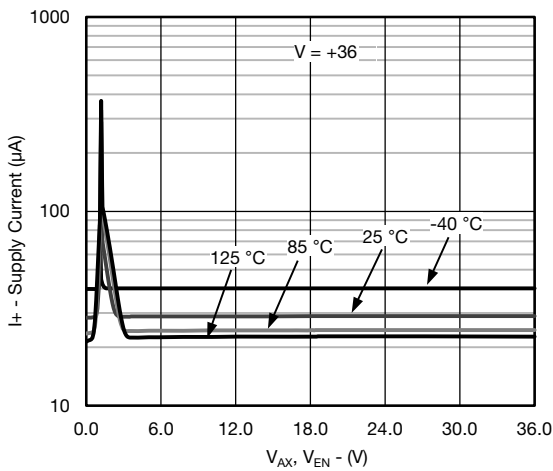
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



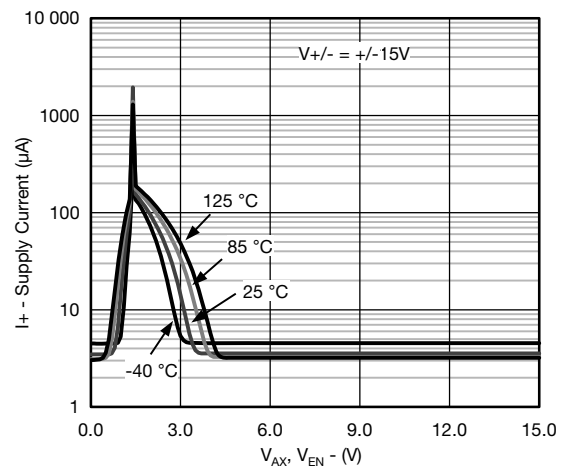
**THD vs. Frequency**



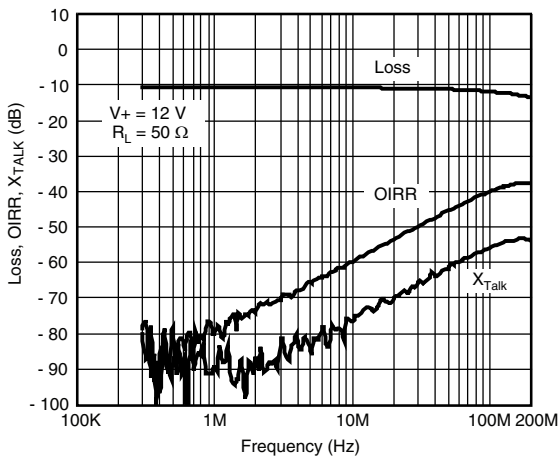
**Supply Current vs. Input Switching Frequency**



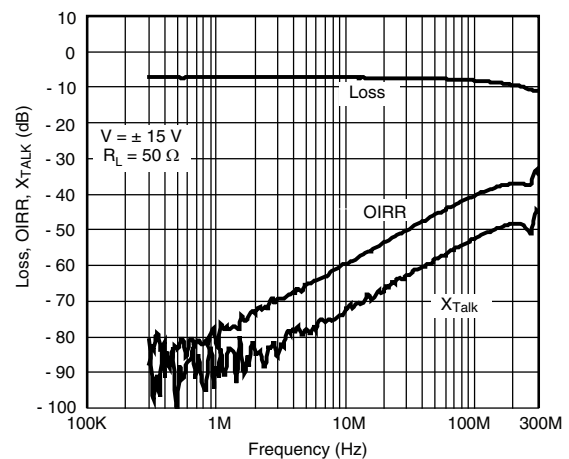
**Supply Current vs.  $V_{\text{AX}}, V_{\text{EN}}$**



**Supply Current vs.  $V_{\text{AX}}, V_{\text{EN}}$**



**Insertion Loss, Off-Isolation, Crosstalk vs. Frequency**



**Insertion Loss, Off-Isolation, Crosstalk vs. Frequency**

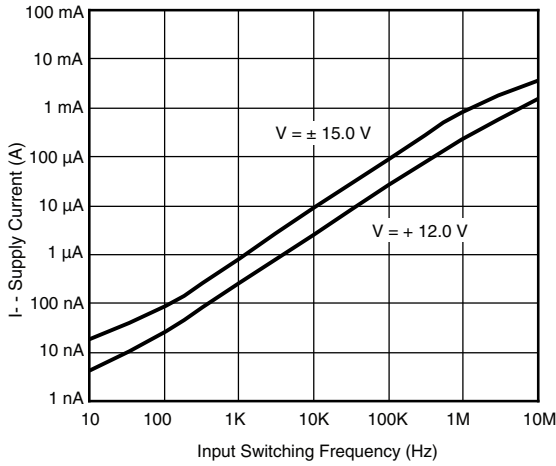


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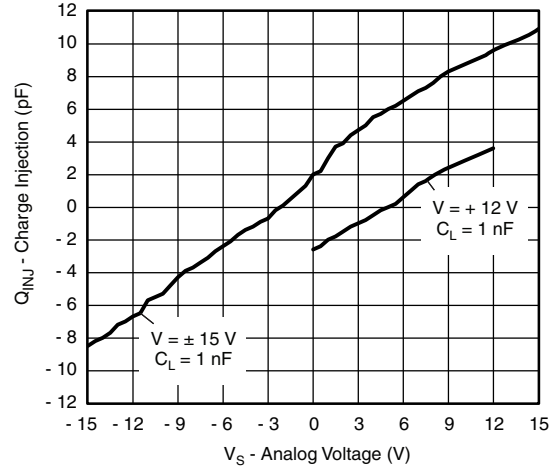
**DG508B, DG509B**

Vishay Siliconix

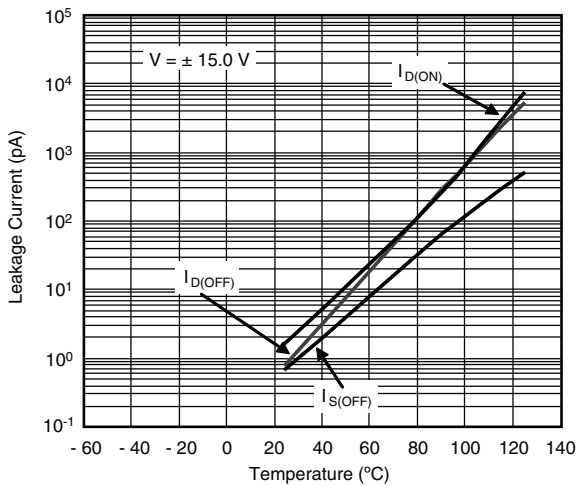
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



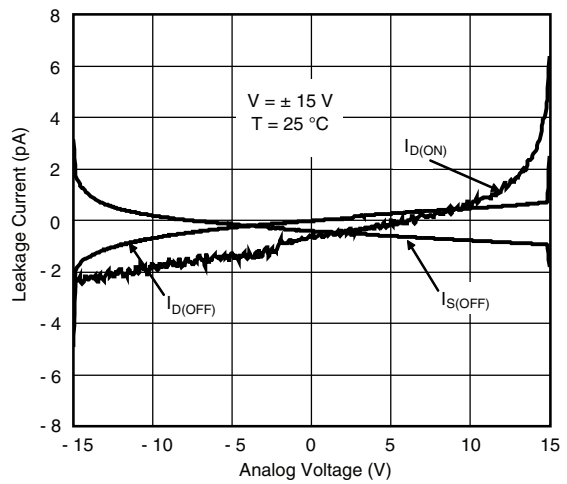
**Supply Current vs. Input Switching Frequency**



**Charge Injection vs. Analog Voltage**



**Leakage Current vs. Temperature**



**Leakage Current vs. Analog Voltage**

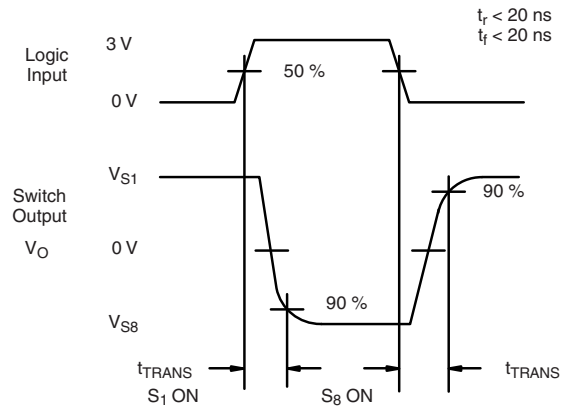
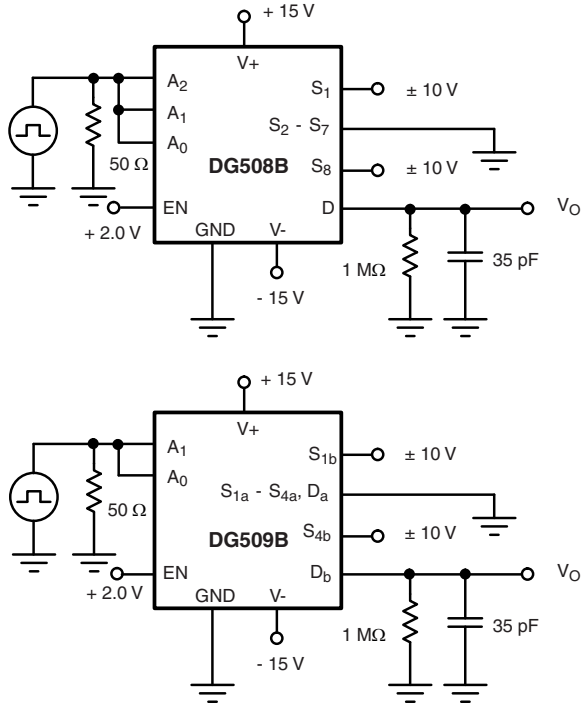


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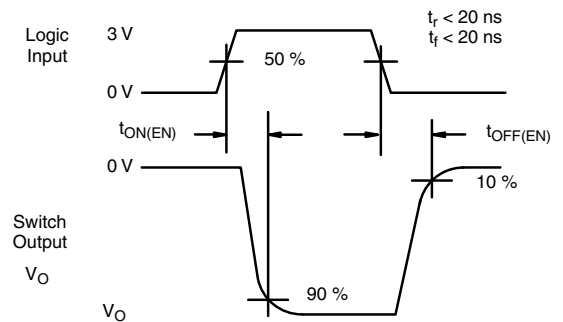
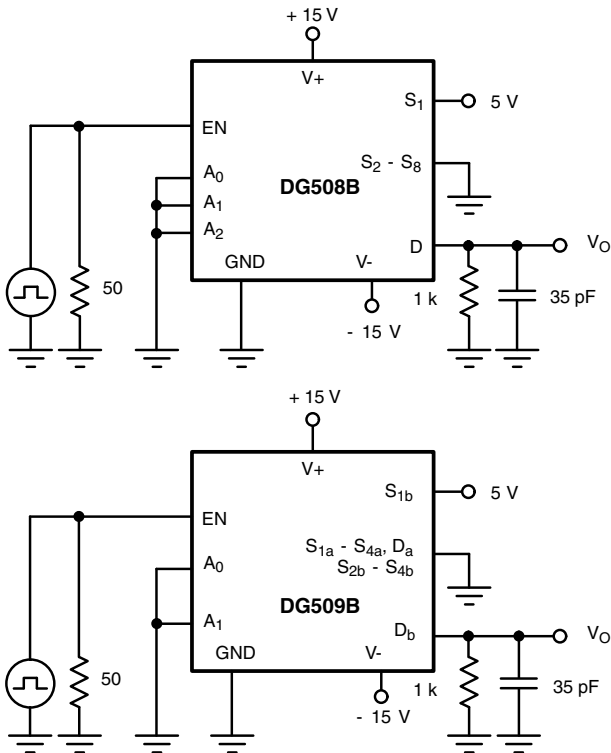
**DG508B, DG509B**

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**TEST CIRCUITS**



**Fig. 2 - Transition Time**



**Fig. 3 - Enable Switching Time**

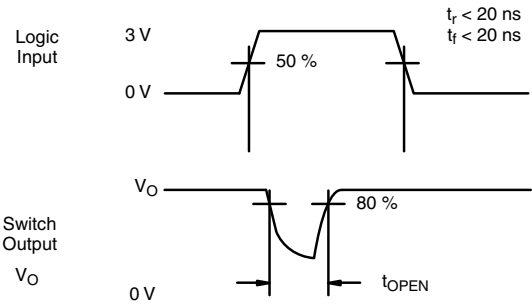
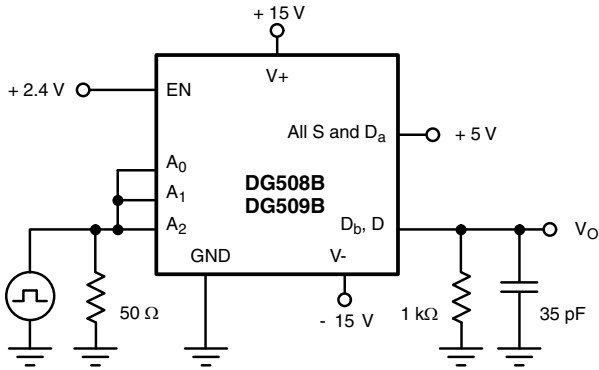


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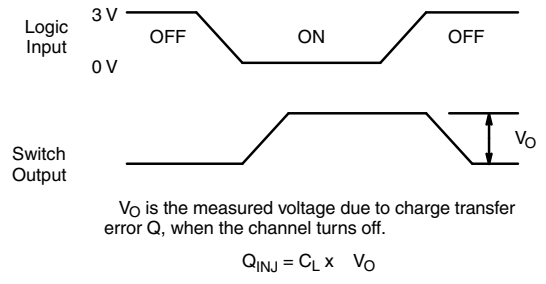
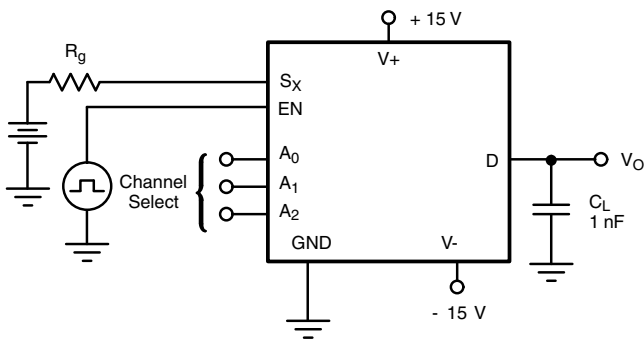
**DG508B, DG509B**

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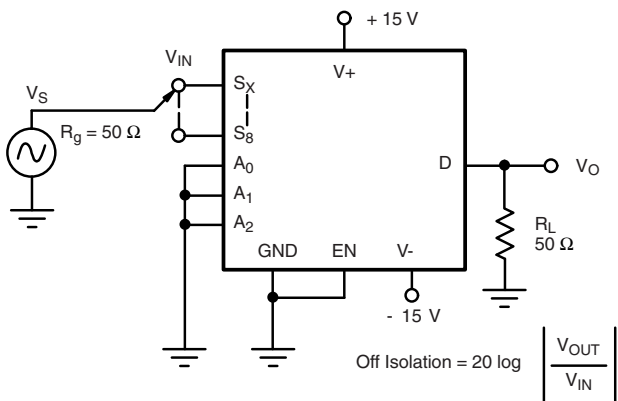
**TEST CIRCUITS**



**Fig. 4 - Break-Before-Make Interval**

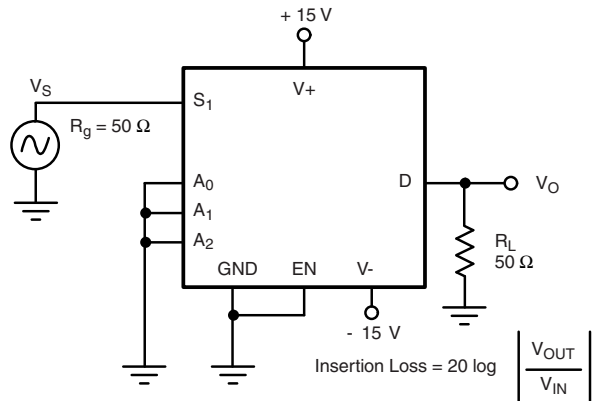


**Fig. 5 - Charge Injection**



**Fig. 6 - Off Isolation**

$$\text{Off Isolation} = 20 \log \left| \frac{V_{OUT}}{V_{IN}} \right|$$



**Fig. 7 - Insertion Loss**

$$\text{Insertion Loss} = 20 \log \left| \frac{V_{OUT}}{V_{IN}} \right|$$

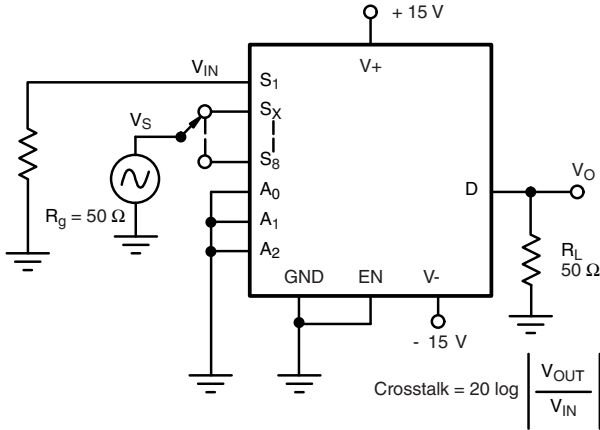


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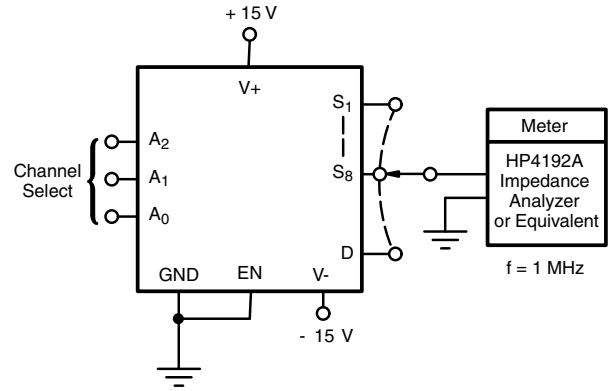
**DG508B, DG509B**

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**TEST CIRCUITS**



**Fig. 8 - Crosstalk**



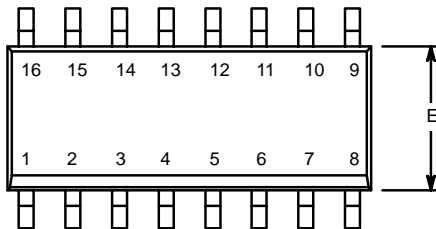
**Fig. 9 - Source Drain Capacitance**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?64821](http://www.vishay.com/ppg?64821).



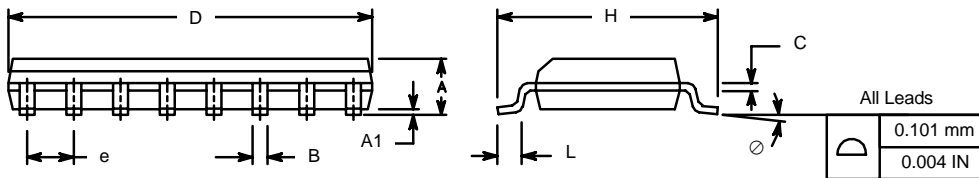
## Package Information Vishay Siliconix

**SOIC (NARROW): 16-LEAD**  
 JEDEC Part Number: MS-012



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
∅	0°	8°	0°	8°

ECN: S-03946—Rev. F, 09-Jul-01  
 DWG: 5300

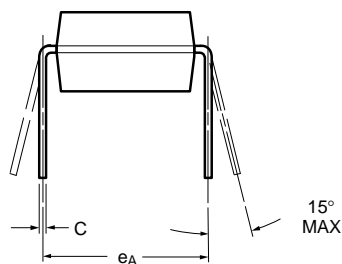
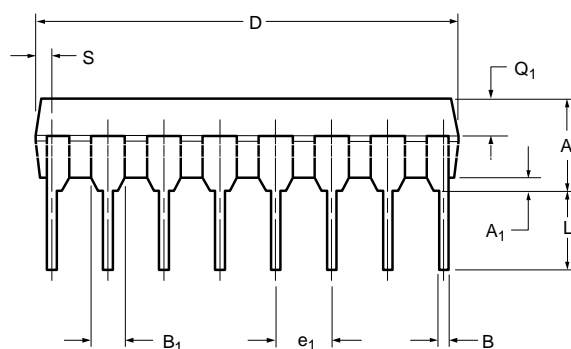
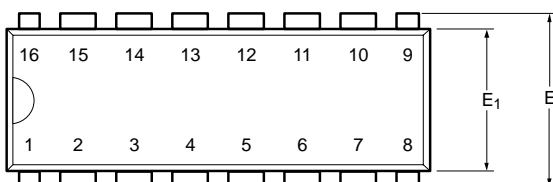




## Package Information

### Vishay Siliconix

#### PDIP: 16-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
<b>A</b>	3.81	5.08	0.150	0.200
<b>A<sub>1</sub></b>	0.38	1.27	0.015	0.050
<b>B</b>	0.38	0.51	0.015	0.020
<b>B<sub>1</sub></b>	0.89	1.65	0.035	0.065
<b>C</b>	0.20	0.30	0.008	0.012
<b>D</b>	18.93	21.33	0.745	0.840
<b>E</b>	7.62	8.26	0.300	0.325
<b>E<sub>1</sub></b>	5.59	7.11	0.220	0.280
<b>e<sub>1</sub></b>	2.29	2.79	0.090	0.110
<b>e<sub>A</sub></b>	7.37	7.87	0.290	0.310
<b>L</b>	2.79	3.81	0.110	0.150
<b>Q<sub>1</sub></b>	1.27	2.03	0.050	0.080
<b>S</b>	0.38	1.52	.015	0.060

ECN: S-03946—Rev. D, 09-Jul-01  
DWG: 5482



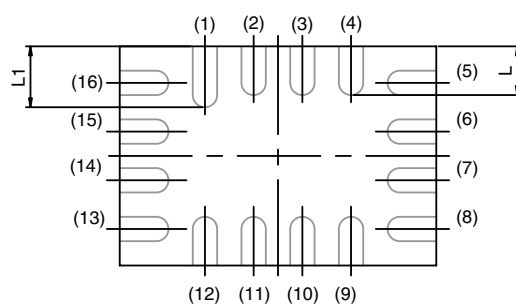
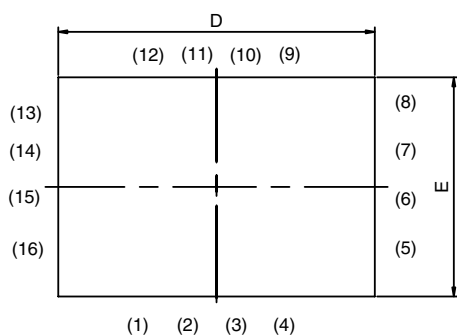


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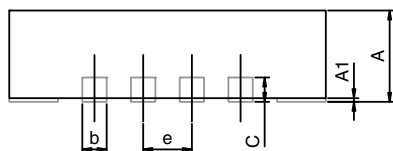
## Package Information

Vishay Siliconix

### miniQFN-16L



BACK SIDE VIEW



DIM	MILLIMETERS			INCHES		
	MIN.	NAM	MAX.	MIN.	NAM	MAX.
A	0.70	0.75	0.80	0.0275	0.0295	0.0315
A1	0	-	0.05	0	-	0.002
b	0.15	0.20	0.25	0.0059	0.0078	0.0098
C	0.15	0.20	0.25	0.0059	0.0078	0.0098
D	2.50	2.60	2.70	0.0984	0.1023	0.1063
E	1.70	1.80	1.90	0.0669	0.0708	0.0748
e	0.40 BSC			0.0157 BSC		
L	0.35	0.40	0.45	0.0137	0.0157	0.0177
L1	0.45	0.50	0.55	0.0177	0.0196	0.0216

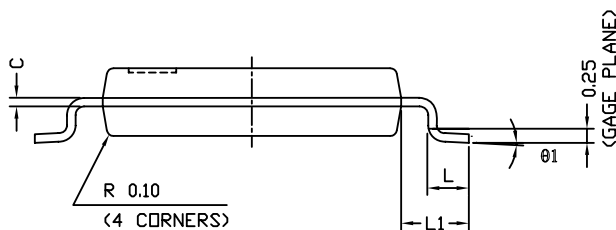
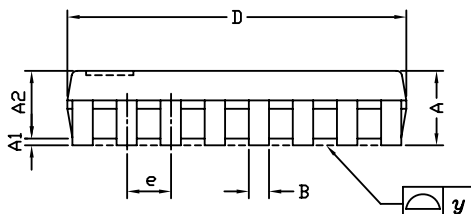
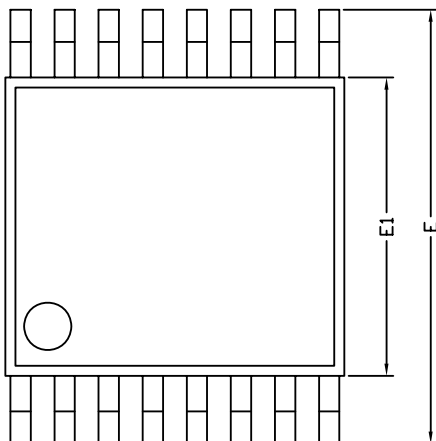
ECN T16-0234-Rev. B, 09-May-16  
 DWG: 5954



## Package Information

Vishay Siliconix

### TSSOP: 16-LEAD



Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
theta 1	0°	3°	6°

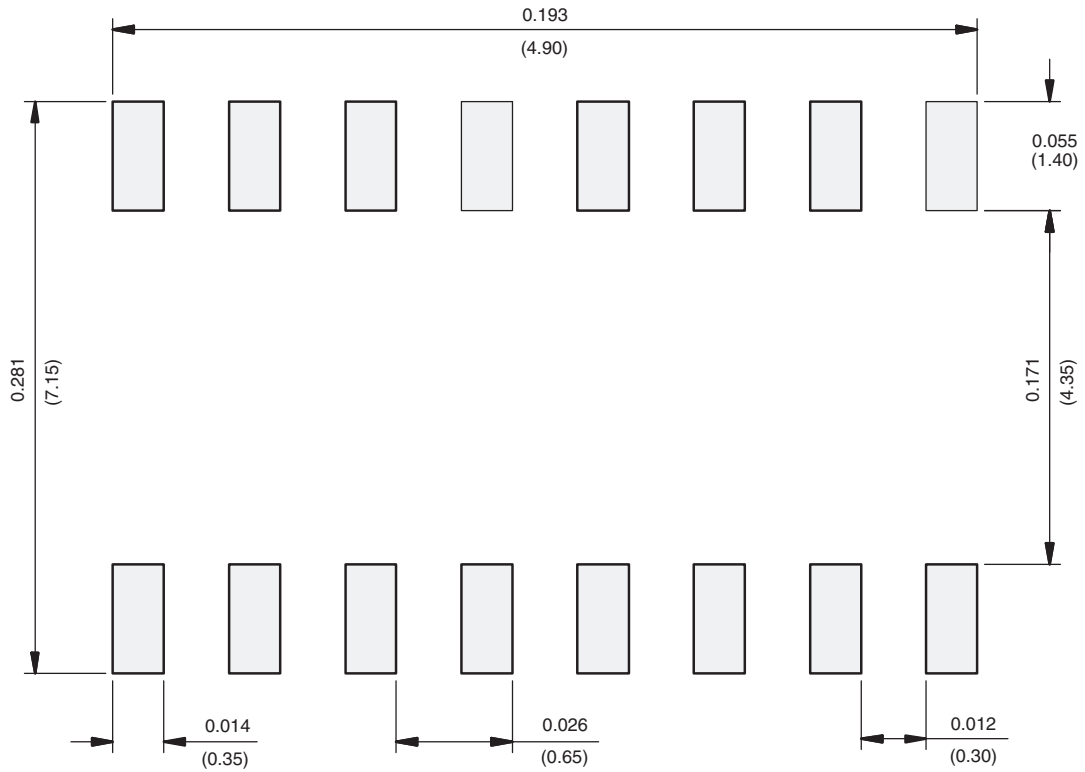
ECN: S-61920-Rev. D, 23-Oct-06  
DWG: 5624



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**PAD Pattern**  
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**RECOMMENDED MINIMUM PAD FOR TSSOP-16**



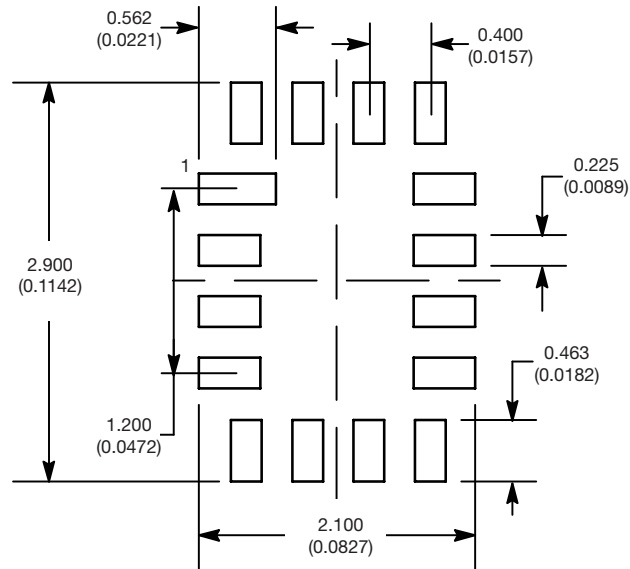
Recommended Minimum Pads  
 Dimensions in inches (mm)



# PAD Pattern

Vishay Siliconix

## RECOMMENDED MINIMUM PADS FOR MINI QFN 16L



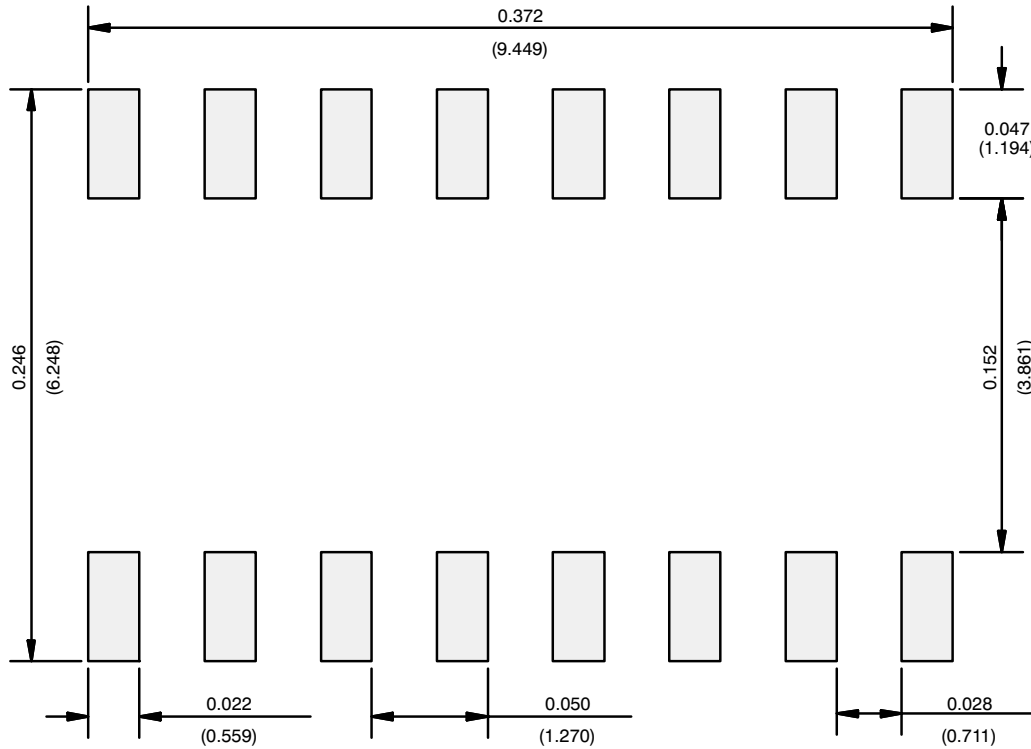
Mounting Footprint  
Dimensions in mm (inch)

# Application Note 826

Vishay Siliconix



## RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads  
 Dimensions in Inches/(mm)

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APPLICATION NOTE



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