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[ON Semiconductor](#)  
[NTMD6601NR2G](#)

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# NTMD6601NR2G

## Power MOSFET

80 V, 2.2 A, Dual N-Channel, SO-8

### Features

- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- Dual SO-8 Surface Mount Package Saves Board Space
- This is a Pb-Free Device

### Applications

- LCD Displays

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	80	V
Gate-to-Source Voltage - Continuous	$V_{GS}$	$\pm 15$	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	$I_D$	$T_A = 25^\circ\text{C}$	1.4
		$T_A = 70^\circ\text{C}$	1.2
Power Dissipation $R_{\theta JA}$ (Note 1)	$P_D$	$T_A = 25^\circ\text{C}$	1.0
		$T_A = 70^\circ\text{C}$	0.6
Continuous Drain Current $R_{\theta JA}$ (Note 2)	$I_D$	$T_A = 25^\circ\text{C}$	1.1
		$T_A = 70^\circ\text{C}$	0.9
Power Dissipation $R_{\theta JA}$ (Note 2)	$P_D$	$T_A = 25^\circ\text{C}$	0.6
		$T_A = 70^\circ\text{C}$	0.6
Continuous Drain Current $R_{\theta JA} t < 5$ s (Note 1)	$I_D$	$T_A = 25^\circ\text{C}$	2.2
		$T_A = 70^\circ\text{C}$	1.7
Pulsed Drain Current	$T_A = 25^\circ\text{C}$ , $t_p = 10 \mu\text{s}$	$I_{DM}$	9.0
Operating Junction and Storage Temperature	$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$
Source Current (Body Diode)	$I_S$	1.3	A
Single Pulse Drain-to-Source Avalanche Energy $T_J = 25^\circ\text{C}$ , $V_{DD} = 50$ V, $V_{GS} = 10$ V, $I_L = 7.0$ A <sub>pk</sub> , $L = 1.0$ mH, $R_G = 25 \Omega$	EAS	2.5	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$

### THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	120	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - $t \leq 5$ s (Note 1)	$R_{\theta JA}$	48	
Junction-to-FOOT (Drain)	$R_{\theta JF}$	40	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	200	

1. Surface-mounted on 2 inch sq FR4 board using 1 inch sq pad size, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size.

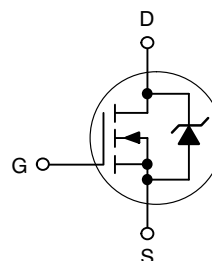


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$V_{(BR)DSS}$	$R_{DS(on)}$ Max	$I_D$ Max
80 V	215 m $\Omega$ @ 10 V	2.2 A
	245 m $\Omega$ @ 4.5 V	

### N-Channel



### MARKING DIAGRAM & PIN ASSIGNMENT



6601N = Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ■ = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping†
NTMD6601NR2G	SO-8 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

## NTMD6601NR2G

**ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			99.8		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		25	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 15\text{ V}$			$\pm 100$	nA

**ON CHARACTERISTICS** (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.0	1.9	3.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			4.6		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 2.2\text{ A}$		190	215	m $\Omega$
		$V_{GS} = 5.0\text{ V}, I_D = 1.0\text{ A}$		215	245	

**CHARGES, CAPACITANCES AND GATE RESISTANCE**

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 25\text{ V}$		220	400	pF
Output Capacitance	$C_{OSS}$			55	100	
Reverse Transfer Capacitance	$C_{RSS}$			16	30	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 5.0\text{ V}, V_{DS} = 40\text{ V}, I_D = 1.0\text{ A}$		5.0	9.0	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.4		
Gate-to-Source Charge	$Q_{GS}$			1.0		
Gate-to-Drain Charge	$Q_{GD}$			2.75		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 40\text{ V}, I_D = 1.0\text{ A}$		9.0	15	nC

**SWITCHING CHARACTERISTICS** (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DD} = 40\text{ V}, I_D = 1.0\text{ A}, R_G = 27\ \Omega$		21	35	ns
Rise Time	$t_r$			62	105	
Turn-Off Delay Time	$t_{d(OFF)}$			52	85	
Fall Time	$t_f$			50	85	
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DD} = 40\text{ V}, I_D = 2.5\text{ A}, R_G = 47\ \Omega$		15		ns
Rise Time	$t_r$			95		
Turn-Off Delay Time	$t_{d(OFF)}$			50		
Fall Time	$t_f$			105		

**BODY - DRAIN DIODE RATINGS** (Note 3)

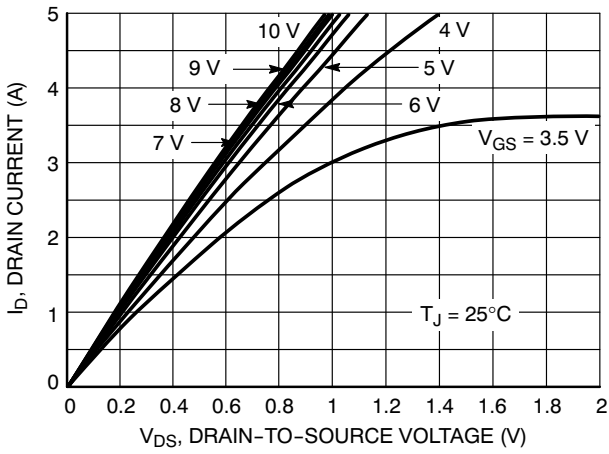
Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_D = 1.0\text{ A}$	$T_J = 25^\circ\text{C}$		0.8	1.0	V
			$T_J = 150^\circ\text{C}$		0.6		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 1.0\text{ A}$		44		ns	
Charge Time	$T_a$			21			
Discharge Time	$T_b$			23			
Reverse Recovery Time	$Q_{RR}$			43	86		nC

 3. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

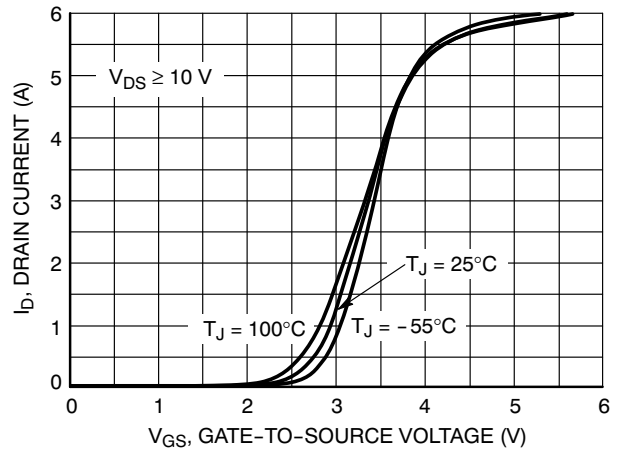
4. Switching characteristics are independent of operating junction temperatures.

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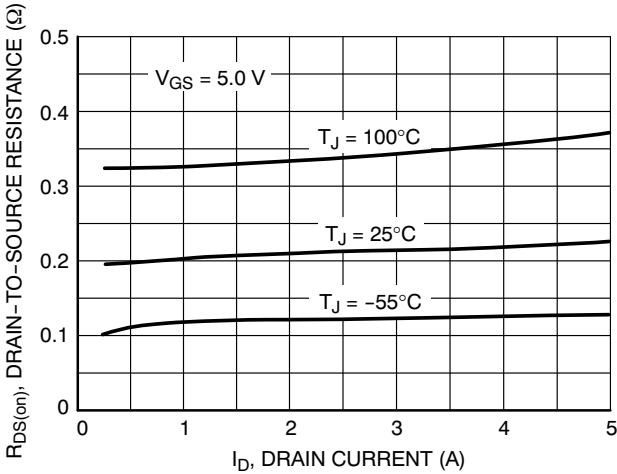
**TYPICAL ELECTRICAL CHARACTERISTICS**



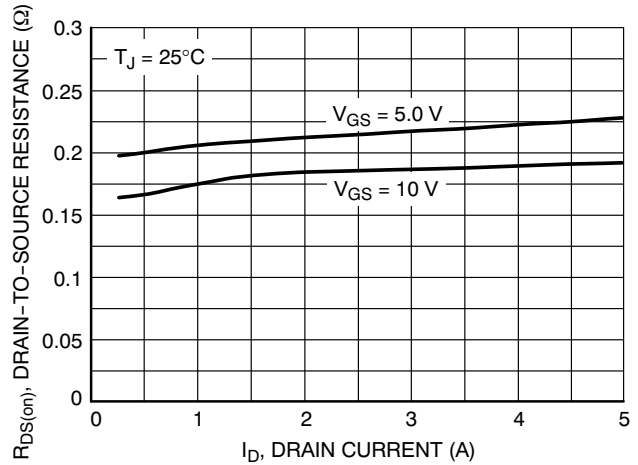
**Figure 1. On-Region Characteristics**



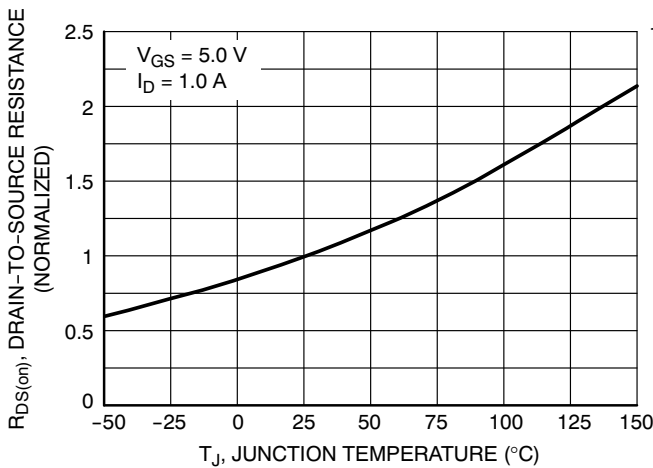
**Figure 2. Transfer Characteristics**



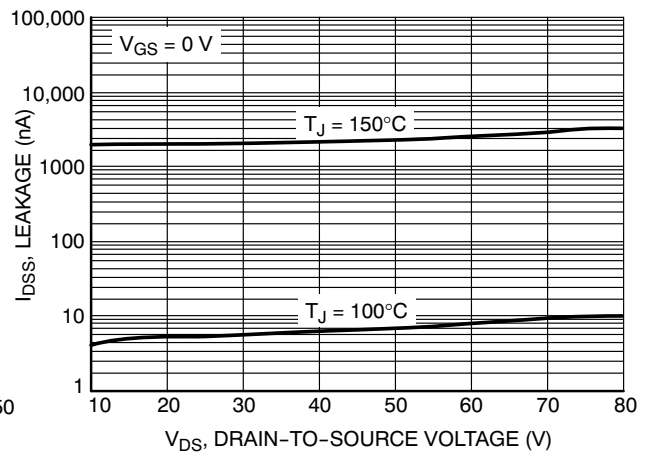
**Figure 3. On-Resistance versus Drain Current and Temperature**



**Figure 4. On-Resistance versus Drain Current and Gate Voltage**



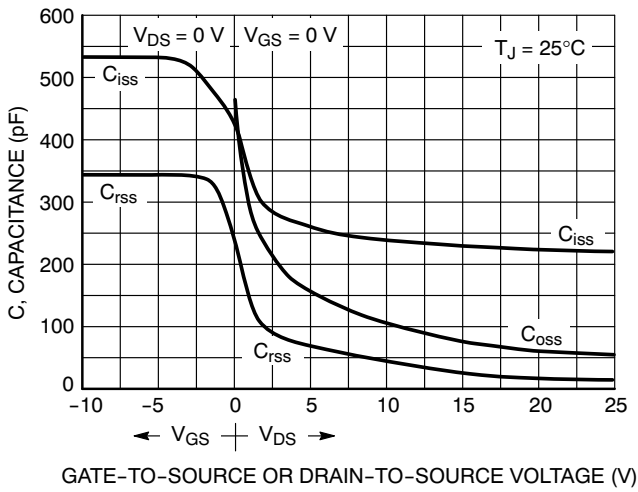
**Figure 5. On-Resistance Variation with Temperature**



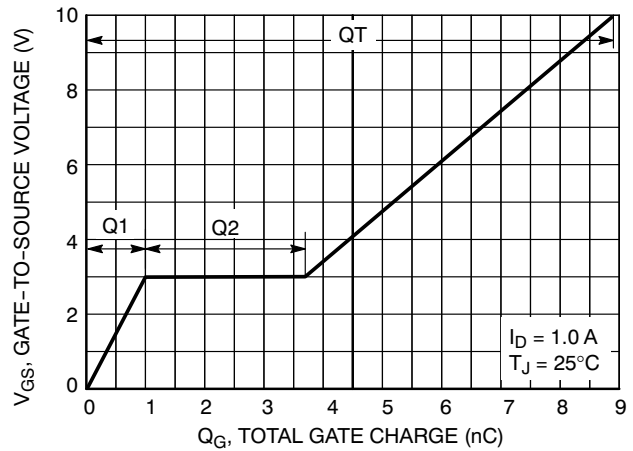
**Figure 6. Drain-to-Source Leakage Current versus Voltage**

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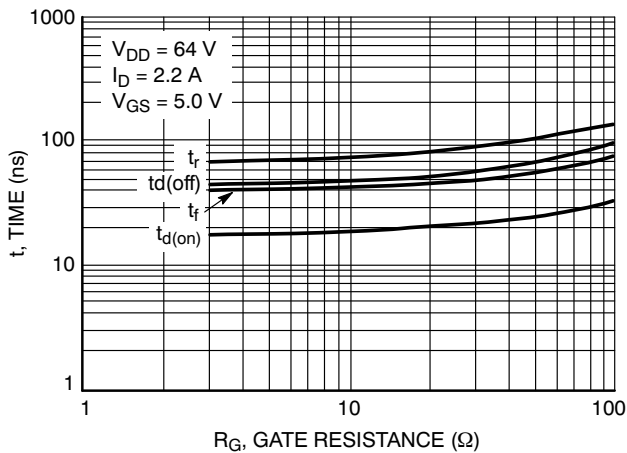
**TYPICAL ELECTRICAL CHARACTERISTICS**



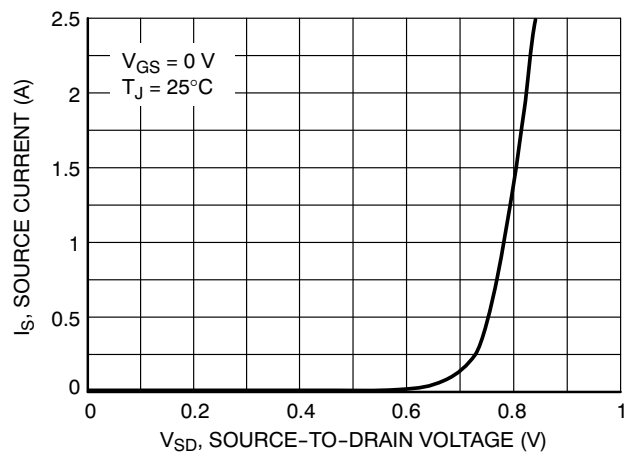
**Figure 7. Capacitance Variation**



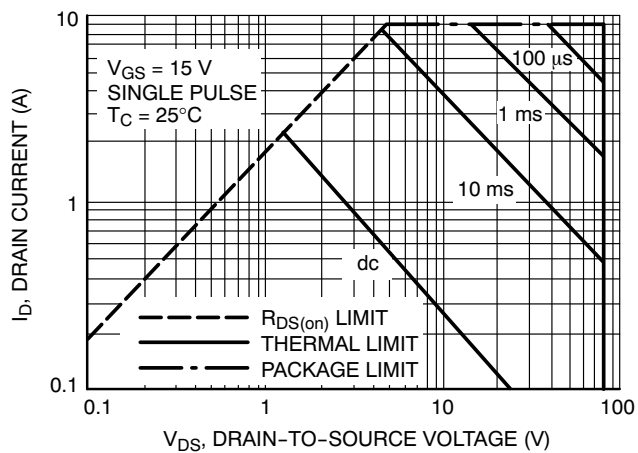
**Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge**



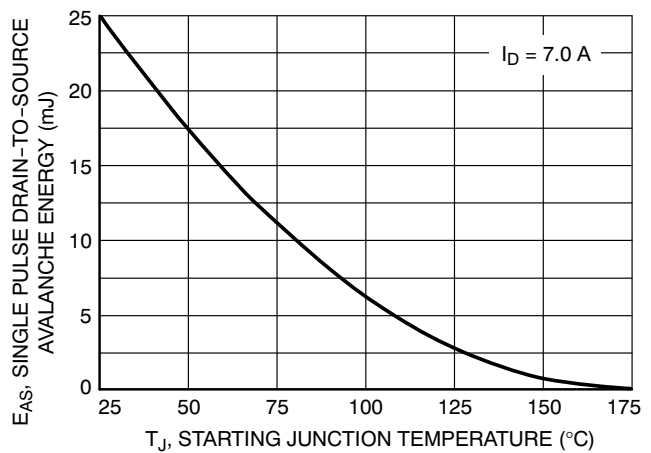
**Figure 9. Resistive Switching Time Variation versus Gate Resistance**



**Figure 10. Diode Forward Voltage versus Current**



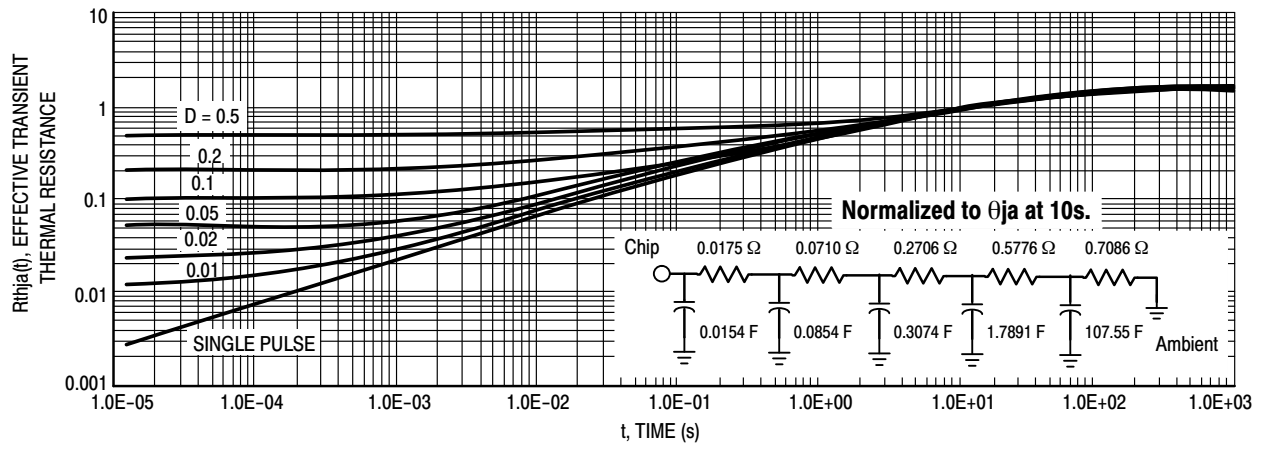
**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



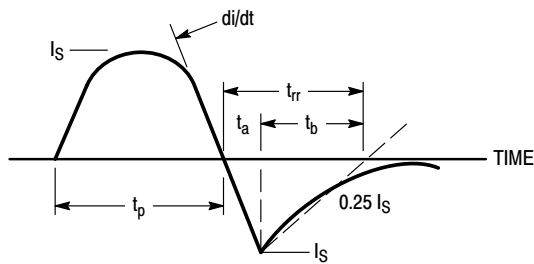
**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

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**TYPICAL ELECTRICAL CHARACTERISTICS**



**Figure 13. Thermal Response**

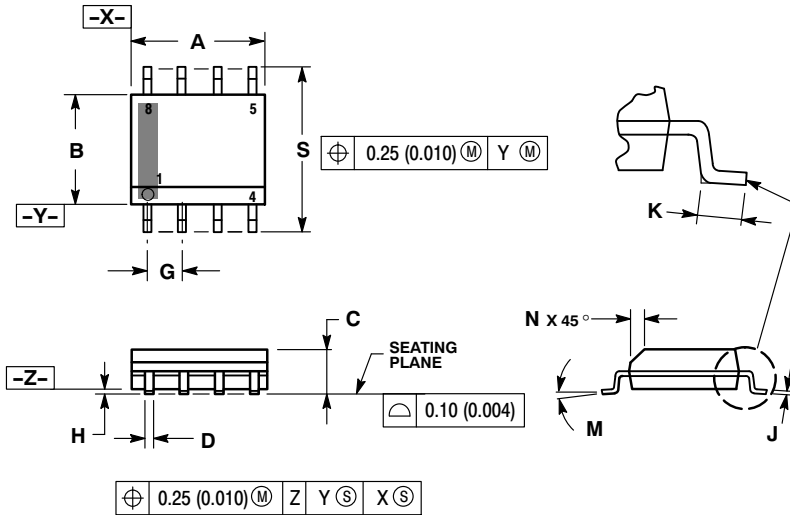


**Figure 14. Diode Reverse Recovery Waveform**

## NTMD6601NR2G

### PACKAGE DIMENSIONS

SO-8 NB  
CASE 751-07  
ISSUE AJ

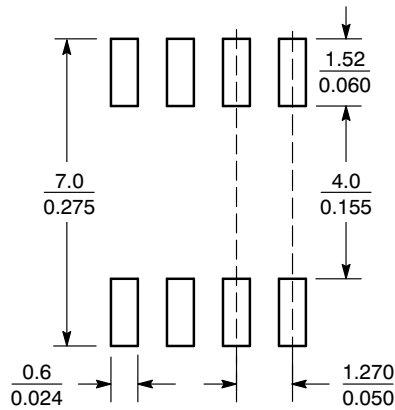


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



SCALE 6:1 (mm/inches)

STYLE 11:

- PIN 1. SOURCE 1  
2. GATE 1  
3. SOURCE 2  
4. GATE 2  
5. DRAIN 2  
6. DRAIN 2  
7. DRAIN 1  
8. DRAIN 1

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

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