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MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

General Description

The MAX7060 frequency and power-programmable ASK/FSK transmitter operates at 280MHz to 450MHz frequencies. This device incorporates a fully integrated fractional-N synthesizer, which allows the user to set the RF operating frequency to a large fraction of the 280MHz to 450MHz frequency range with a single crystal. For example, the MAX7060 can be tuned from 285MHz to 420MHz with a 15MHz crystal. The RF output power is user-controlled between +14dBm and -14dBm, with a 5V supply or with battery voltages as low as 3.2V. At the minimum specified battery voltage of 2.1V, the RF output power-control range is between +10dBm and -14dBm. To maintain a good output power match across a broad range of frequencies, the MAX7060 also contains a programmable matching capacitor connected in parallel with the power amplifier (PA) output.

ASK modulation is accomplished by switching the PA on and off, so excellent modulation (on/off) ratios are achieved. ASK amplitude shaping is available to reduce the width of the transmission spectrum. FSK modulation is accomplished by changing the coefficients of the high-resolution fractional-N synthesizer, so FSK deviation is extremely accurate. Data rates up to 50kbps Manchester coded for ASK and 70kbps Manchester coded for FSK can be maintained while still satisfying regulatory emission-bandwidth standards. The full set of configuration functions are handled by an on-chip serial peripheral interface (SPI). There is also a manual mode where a limited number of settings can be made directly through selected pins.

The startup time is very short, and data can be transmitted 250µs after the enable command. The MAX7060 operates from a 2.1V to 3.6V supply, or internal regulators can be used for supply voltages between 4.5V and 5.5V. The standby current in the 3V mode is 400nA at room temperature, and can be reduced to 5nA using the low-power shutdown (LSHDN) pin.

The MAX7060 is available in a 24-pin (4mm x 4mm) thin QFN package and is specified for the automotive temperature range from -40°C to +125°C.

Features

- ◆ Fully Integrated, Fast Fractional-N PLL
 280MHz to 450MHz RF Frequency
 Frequency Range 100% Tested at +125°C
 < 250µs Startup Time
 Adjustable FSK Mark and Space Frequencies
 Ultra-Clean FSK Modulation
 50kbps Manchester Data Rate ASK
 70kbps Manchester Data Rate FSK
- ◆ Programmable Power Amplifier
 +14dBm Tx Power with 5V Supply
 +10dBm Tx Power at 2.1V Supply
 28dB Power-Control Range in 1dB Steps
- ◆ Tunable PA Matching Capacitor
- ◆ Control Through SPI or Manual Settings
- ◆ Low Shutdown Current for 2.1V to 3.6V Supply
 400nA Standby Current, Power-On-Reset (POR) Active
 5nA Shutdown Current, POR Inactive
- ◆ Supply Flexibility
 2.1V to 3.6V Single-Supply Operation or
 4.5V to 5.5V Supply Operation with Internal Regulators
- ◆ 24-Pin (4mm x 4mm) TQFN Package
- ◆ FCC Part 15, ETSI EN 300 220 Compliant*

*ETSI compliance up to +6dBm EIRP.

Applications

Garage-Door Openers
 Remote Controls
 Home and Industrial Automation
 Sensor Networks
 Security Systems

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---------------|-----------------|-------------|
| MAX7060ATG+ | -40°C to +125°C | 24 TQFN-EP* |
| MAX7060ATG/V+ | -40°C to +125°C | 24 TQFN-EP* |

+Denotes a lead(Pb)-free/RoHS-compliant package.

/V denotes an automotive qualified part.

*EP = Exposed pad.

MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

ABSOLUTE MAXIMUM RATINGS

| | | |
|--|--------------------------------------|---|
| GPOVDD, V _{DD5} to GND..... | -0.3V to +6.0V | Continuous Power Dissipation (T _A = +70°C) |
| DVDD, PAVDD, and AVDD to GND..... | -0.3V to +4.0V | 24-Pin Thin QFN |
| ENABLE, SCLK_PWR0, SDI_PWR1, DIN, CS_DEV, LSHDN, FREQ0, FREQ1, FREQ2, GPO1, and GPO2_MOD to GND..... | -0.3V to (V _{DD5} + 0.3V) | (derate 20.8mW/°C above +70°C)..... |
| PAOUT, ROUT, and PAVOUT to GND..... | -0.3V to (V _{PAVDD} + 0.3V) | 1666.7mW |
| XTAL1 and XTAL2 to GND..... | -0.3V to (V _{AVDD} + 0.3V) | Operating Temperature Range..... |
| | | Storage Temperature Range..... |
| | | Lead Temperature (soldering, 10s)..... |
| | | Soldering Temperature (reflow)..... |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (5V OPERATION)

(Typical Application Circuit, 50Ω system impedance, tuned for 315MHz to 434MHz operation. V_{DD5} = V_{GPOVDD} = 4.5V to 5.5V, f_{RF} = 280MHz to 450MHz, f_{XTAL} = 15MHz to 16MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD5} = V_{GPOVDD} = +5V, T_A = +25°C, PA matched for optimum output power, unless otherwise noted. All min and max values are 100% tested at T_A = +125°C and guaranteed by design and characterization over temperature, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | |
|--|-----------------------------|--|-----------------------------|-----|-------------------------|-------|------|
| Supply Voltage | V _{DD} | | 4.5 | 5 | 5.5 | V | |
| Regulated Analog Supply Voltage | AVDD | | | 3.2 | | V | |
| Active Supply Current | I _{DD} | PLL on, PA off | f _{RF} = 315MHz | 4.7 | 6.0 | mA | |
| | | | f _{RF} = 433.92MHz | 5.3 | 6.9 | | |
| | | PLL on, PA on, data at 50% duty cycle (ASK), +10dBm (P _{Apwr} = 0x19) output power (Notes 1, 2) | f _{RF} = 315MHz | | 12.5 | | |
| | | | f _{RF} = 433.92MHz | | 14.2 | | |
| | | PLL on, PA on, data at 100% duty cycle, +10dBm (P _{Apwr} = 0x19) output power (Note 1) | f _{RF} = 315MHz | | 19 | | 26 |
| | | | f _{RF} = 433.92MHz | | 25 | | 31.6 |
| PLL on, PA on, data at 100% duty cycle, max (P _{Apwr} = 0x1E) output power (Note 1) | f _{RF} = 315MHz | | | 28 | | | |
| | f _{RF} = 433.92MHz | | | 34 | | | |
| Standby Current | I _{STDBY} | V _{ENABLE} < V _{IL} , V _{LSHDN} < V _{IL} | T _A = +25°C | 1.1 | | μA | |
| | | | T _A = +85°C | 1.3 | | | |
| | | | T _A = +125°C | 3.8 | 6.1 | | |
| DIGITAL I/O | | | | | | | |
| Input High Threshold | V _{IH} | | 0.9 x V _{DVDD} | | | V | |
| Input Low Threshold | V _{IL} | | | | 0.1 x V _{DVDD} | V | |

MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

DC ELECTRICAL CHARACTERISTICS (5V OPERATION) (continued)

(Typical Application Circuit, 50Ω system impedance, tuned for 315MHz to 434MHz operation. VDD5 = VGPOVDD = 4.5V to 5.5V, f_{RF} = 280MHz to 450MHz, f_XTAL = 15MHz to 16MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at VDD5 = VGPOVDD = +5V, T_A = +25°C, PA matched for optimum output power, unless otherwise noted. All min and max values are 100% tested at T_A = +125°C and guaranteed by design and characterization over temperature, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------------------------|-----------------|---|-----|----------------------------|-----|-------|
| Input Pulldown Sink Current | I _{IH} | | | 6 | | μA |
| Input Pullup Source Current | I _{IL} | | | 5 | | μA |
| Output-Voltage High | V _{OH} | I _{SINK} = 100μA (GPO1 and GPO2_MOD, gp1bst bit = 0) | | V _{GP0VDD} - 0.10 | | V |
| | | I _{SINK} = 200μA (GPO1), boost = on (gp1bst bit = 1) | | V _{GP0VDD} - 0.14 | | |
| Output-Voltage Low | V _{OL} | I _{SOURCE} = 100μA (GPO1 and GPO2_MOD, gp1bst bit = 0) | | 0.10 | | V |
| | | I _{SOURCE} = 200μA (GPO1), boost = on (gp1bst bit = 1) | | 0.14 | | |

DC ELECTRICAL CHARACTERISTICS (3V OPERATION)

(Typical Application Circuit, 50Ω system impedance, tuned for 315MHz to 434MHz operation. VDD5 = VGPOVDD = VAVDD = VD_{VDD} = VPAVDD = 2.1V to 3.6V, f_{RF} = 280MHz to 450MHz, f_XTAL = 15MHz to 16MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at VDD5 = VGPOVDD = VAVDD = VD_{VDD} = VPAVDD = 2.7V, T_A = +25°C, PA matched for optimum output power, unless otherwise noted. All min and max values are 100% tested at T_A = +125°C and guaranteed by design and characterization over temperature, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-----------------------------|--|-----------------------------|-------|-----|-------|
| Supply Voltage | V _{DD} | | 2.1 | 2.7 | 3.6 | V |
| Active Supply Current | I _{DD} | PLL on, PA off | f _{RF} = 315MHz | 4.2 | 6.2 | mA |
| | | | f _{RF} = 433.92MHz | 4.8 | 7.2 | |
| | | PLL on, PA on, data at 50% duty cycle (ASK), +10dBm (P _{Apwr} = 0x19) output power (Notes 1, 2) | f _{RF} = 315MHz | 11 | | |
| | | | f _{RF} = 433.92MHz | 13 | | |
| PLL on, PA on, data at 100% duty cycle, +10dBm (P _{Apwr} = 0x19) output power (Note 1) | f _{RF} = 315MHz | 17.2 | 27 | | | |
| | f _{RF} = 433.92MHz | 22 | 31.6 | | | |
| Standby Current | I _{STDBY} | V _{ENABLE} < V _{IL} , V _L SHDN < V _{IL} | T _A = +25°C | 0.4 | | μA |
| | | | T _A = +85°C | 0.5 | | |
| | | | T _A = +125°C | 2.5 | 6.0 | |
| Shutdown Current | I _{SHDN} | V _{ENABLE} < V _{IL} , V _L SHDN > V _{IH} | T _A = +25°C | 0.005 | | μA |
| | | | T _A = +85°C | 0.3 | | |
| | | | T _A = +125°C | 2.6 | 6.0 | |

MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

DC ELECTRICAL CHARACTERISTICS (3V OPERATION) (continued)

(Typical Application Circuit, 50Ω system impedance, tuned for 315MHz to 434MHz operation. VDD5 = VGPOVDD = VAVDD = VD VDD = VPAVDD = 2.1V to 3.6V, f_{RF} = 280MHz to 450MHz, f_{XTAL} = 15MHz to 16MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at VDD5 = VGPOVDD = VAVDD = VD VDD = VPAVDD = 2.7V, T_A = +25°C, PA matched for optimum output power, unless otherwise noted. All min and max values are 100% tested at T_A = +125°C and guaranteed by design and characterization over temperature, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------------------------|-----------------|---|-----------------|-------------------|-----------------|-------|
| DIGITAL I/O | | | | | | |
| Input High Threshold | V _{IH} | | 0.9 x VD VDD | | | V |
| Input Low Threshold | V _{IL} | | | | 0.1 x VD VDD | V |
| Input Pulldown Sink Current | I _{IH} | | | 5 | | μA |
| Input Pullup Source Current | I _{IL} | | | 1.3 | | μA |
| Output-Voltage High | V _{OH} | I _{SINK} = 100μA (GPO1 and GPO2_MOD, gp1bst bit = 0) | | VGPOVDD - 0.10 | | V |
| | | I _{SINK} = 200μA (GPO1), boost = on (gp1bst bit = 1) | | VGPOVDD - 0.14 | | |
| Output-Voltage Low | V _{OL} | I _{SOURCE} = 100μA (GPO1 and GPO2_MOD, gp1bst bit = 0) | | 0.10 | | V |
| | | I _{SOURCE} = 200μA (GPO1), boost = on (gp1bst bit = 1) | | 0.14 | | |

AC ELECTRICAL CHARACTERISTICS (5V OPERATION)

(Typical Application Circuit, 50Ω system impedance, tuned for 315MHz to 434MHz operation, VDD5 = VGPOVDD = 4.5V to 5.5V, f_{RF} = 280MHz to 450MHz, f_{XTAL} = 15MHz to 16MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at VDD5 = VGPOVDD = +5V, T_A = +25°C, PA matched for optimum output power, unless otherwise noted. All min and max values are 100% tested at T_A = +125°C and guaranteed by design and characterization over temperature, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------------|---|--------------------|-----|-----|-------|
| GENERAL CHARACTERISTICS | | | | | | |
| Frequency Range | | | 280 | | 450 | MHz |
| Power-On Time | t _{ON} | ENABLE low-to-high transition, frequency settled to within 50kHz of the desired carrier (includes time for V _{PAVOUT} to settle) | | 130 | | μs |
| | | ENABLE low-to-high transition, frequency settled to within 5kHz of the desired carrier (includes time for V _{PAVOUT} to settle) | | 185 | | |
| Maximum Data Rate (PA _{pwr} = 0x1E) | | ASK mode (no shaping) | Manchester encoded | 50 | | kbps |
| | | | Nonreturn to zero | 100 | | |
| | | FSK mode | Manchester encoded | 70 | | |
| | | | Nonreturn to zero | 140 | | |

MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

AC ELECTRICAL CHARACTERISTICS (5V OPERATION) (continued)

(Typical Application Circuit, 50Ω system impedance, tuned for 315MHz to 434MHz operation, VDD5 = VGPOVDD = 4.5V to 5.5V, f_{RF} = 280MHz to 450MHz, f_{X TAL} = 15MHz to 16MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at VDD5 = VGPOVDD = +5V, T_A = +25°C, PA matched for optimum output power, unless otherwise noted. All min and max values are 100% tested at T_A = +125°C and guaranteed by design and characterization over temperature, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------------------|--------------------|---|--------------|-----------|------|-------------------|
| Carrier-Frequency Switching Time | | Time from end of SPI write or change of FREQ0, FREQ1, or FREQ2 pins, to frequency settled to within 5kHz of desired carrier | | 60 | | μs |
| PLL | | | | | | |
| VCO Gain | K _{VCO} | | | 340 | | MHz/V |
| PLL Phase Noise | | f _{RF} = 315MHz | 10kHz offset | -78 | | dBc/Hz |
| | | | 1MHz offset | -97 | | |
| | | f _{RF} = 433.92MHz | 10kHz offset | -74 | | |
| | | | 1MHz offset | -97 | | |
| Loop Bandwidth | | | 300 | | kHz | |
| Reference Frequency Input Level | | | | 500 | | mV _{P-P} |
| Frequency Divider Range | | | 19 | | 28 | |
| Frequency Deviation (FSK) | | | ±2 | | ±100 | kHz |
| CRYSTAL OSCILLATOR | | | | | | |
| Crystal Frequency | f _{X TAL} | | | 15 to 16 | | MHz |
| Crystal Load Capacitance (Note 3) | | | | 10 | | pF |
| POWER AMPLIFIER | | | | | | |
| Output Transmit Power (Note 1) | P _{OUT} | Maximum output transmit power: P _{Apwr} = 0x1E | | +14.5 | | dBm |
| | | Minimum output transmit power: P _{Apwr} = 0x00 | | -14 | | |
| Power-Control Step Size | | | | 0.95 | | dB |
| Modulation Depth (Note 1) | | | | 70 | | dB |
| Maximum Carrier Harmonics (Note 1) | | | | -24 | | dBc |
| Reference Spur | | | | -42 | | dBc |
| PAOUT Capacitor Tuning Range | | | | 0 to 7.75 | | pF |

MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

AC ELECTRICAL CHARACTERISTICS (3V OPERATION)

(Typical Application Circuit, 50Ω system impedance, tuned for 315MHz to 434MHz operation. V_{DD5} = V_{GPOVDD} = V_{AVDD} = V_{DVDD} = V_{PAVDD} = 2.1V to 3.6V, f_{RF} = 280MHz to 450MHz, f_{XTAL} = 15MHz to 16MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD5} = V_{GPOVDD} = V_{AVDD} = V_{DVDD} = V_{PAVDD} = 2.7V, T_A = +25°C, PA matched for optimum output power, unless otherwise noted. All min and max values are 100% tested at T_A = +125°C and guaranteed by design and characterization over temperature, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|--|-------------------|---|--------------------|-----|----------|------|-------------------|
| GENERAL CHARACTERISTICS | | | | | | | |
| Frequency Range | | | | 280 | | 450 | MHz |
| Power-On Time | t _{ON} | ENABLE low-to-high transition, frequency settled to within 50kHz of the desired carrier (includes time for V _{PAVOUT} to settle) | | | 120 | | μs |
| | | ENABLE low-to-high transition, frequency settled to within 5kHz of the desired carrier (includes time for V _{PAVOUT} to settle) | | | 200 | | |
| Maximum Data Rate (P _{Apwr} = 0x19) | | ASK mode (no shaping) | Manchester encoded | | 50 | | kbps |
| | | | Nonreturn to zero | | 100 | | |
| | | FSK mode | Manchester encoded | | 70 | | |
| | | | Nonreturn to zero | | 140 | | |
| Carrier-Frequency Switching Time | | Time from end of SPI write or change of FREQ0, FREQ1, or FREQ2 pins, to frequency settled to within 5kHz of desired carrier | | | 60 | | μs |
| PLL | | | | | | | |
| VCO Gain | K _{VCO} | | | | 340 | | MHz/V |
| PLL Phase Noise | | f _{RF} = 315MHz | 10kHz offset | | -78 | | dBc/Hz |
| | | | 1MHz offset | | -97 | | |
| | | f _{RF} = 433.92MHz | 10kHz offset | | -74 | | |
| | | | 1MHz offset | | -97 | | |
| Loop Bandwidth | | | | | 300 | | kHz |
| Reference Frequency Input Level | | | | | 500 | | mV _{P-P} |
| Frequency Divider Range | | | | 19 | | 28 | |
| CRYSTAL OSCILLATOR | | | | | | | |
| Frequency Deviation (FSK) | | | | ±2 | | ±100 | kHz |
| Crystal Frequency | f _{XTAL} | | | | 15 to 16 | | MHz |
| Frequency Pulling by Power Supply | | | | | 4 | | ppm/V |
| Crystal Load Capacitance (Note 3) | | | | | 10 | | pF |
| POWER AMPLIFIER | | | | | | | |
| Output Transmit Power (Note 1) | P _{OUT} | V _{PAVDD} = 2.1V, P _{Apwr} = 0x1E | | | +10 | | dBm |
| | | V _{PAVDD} = 3.6V, P _{Apwr} = 0x1E | | | +15 | | |
| | | P _{Apwr} = 0x00 | | | -14.5 | | |
| Power-Control Step Size | | | | | 0.95 | | dB |
| Modulation Depth (Note 1) | | | | | 70 | | dB |

MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

AC ELECTRICAL CHARACTERISTICS (3V OPERATION) (continued)

(Typical Application Circuit, 50Ω system impedance, tuned for 315MHz to 434MHz operation. V_{DD5} = V_{GPOVDD} = V_{AVDD} = V_{DVDD} = V_{PAVDD} = 2.1V to 3.6V, f_{RF} = 280MHz to 450MHz, f_{X TAL} = 15MHz to 16MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD5} = V_{GPOVDD} = V_{AVDD} = V_{DVDD} = V_{PAVDD} = 2.7V, T_A = +25°C, PA matched for optimum output power, unless otherwise noted. All min and max values are 100% tested at T_A = +125°C and guaranteed by design and characterization over temperature, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------------------|--------|------------|-----|-----------|-----|-------|
| Maximum Carrier Harmonics (Note 1) | | | | -24 | | dBc |
| Reference Spur | | | | -43 | | dBc |
| PAOUT Capacitor Tuning Range | | | | 0 to 7.75 | | pF |

SERIAL PERIPHERAL INTERFACE (SPI) TIMING CHARACTERISTICS

(SPI timing characteristics are valid for both 3V and 5V modes. SPI timing is production tested at worst-case temperature and supply with a clock frequency of 3MHz.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------------|--|-----|-----|-----|-------|
| Minimum SCLK_PWR0 Low to Falling-Edge of $\overline{CS_DEV}$ Setup Time | t _{SC} | | | 30 | | ns |
| Minimum $\overline{CS_DEV}$ Low to Rising Edge of SCLK_PWR0 Setup Time | t _{CSS} | | | 15 | | ns |
| Minimum SCLK_PWR0 Low to Rising Edge of $\overline{CS_DEV}$ Setup Time | t _{HCS} | | | 60 | | ns |
| Minimum SCLK_PWR0 Low After Rising Edge of $\overline{CS_DEV}$ Hold Time | t _{HS} | | | 15 | | ns |
| Minimum Data Valid to SCLK_PWR0 Rising-Edge Setup Time | t _{DS} | | | 30 | | ns |
| Minimum Data Valid to SCLK_PWR0 Rising-Edge Hold Time | t _{DH} | | | 15 | | ns |
| Minimum SCLK_PWR0 High Pulse Width | t _{CH} | | | 120 | | ns |
| Minimum SCLK_PWR0 Low Pulse Width | t _{CL} | | | 120 | | ns |
| Minimum $\overline{CS_DEV}$ High Pulse Width | t _{CSH} | | | 120 | | ns |
| Maximum Transition Time from Falling-Edge of $\overline{CS_DEV}$ to Valid GPO2_MOD | t _{CSG} | C _L = 10pF load capacitance from GPO2_MOD to ground | | 400 | | ns |
| Maximum Transition Time from Falling Edge of SCLK_PWR0 to Valid GPO2_MOD | t _{CG} | C _L = 10pF load capacitance from GPO2_MOD to ground | | 400 | | ns |

Note 1: Supply current and output power are greatly dependent on board layout and PAOUT match.

Note 2: 50% duty cycle at 10kHz ASK data (Manchester coded).

Note 3: Dependent on PCB trace capacitance.

MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

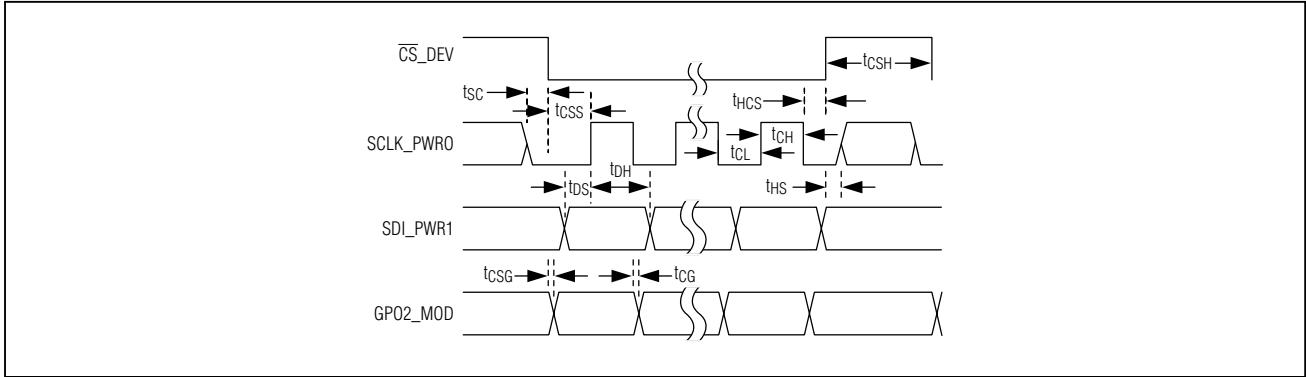
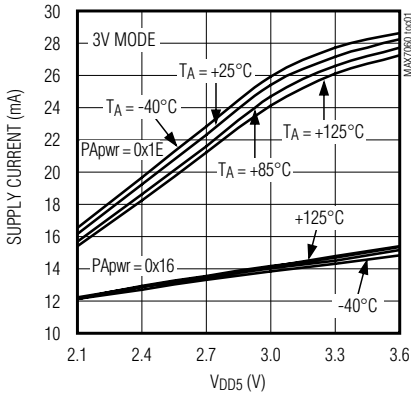


Figure 1. SPI Timing Diagram

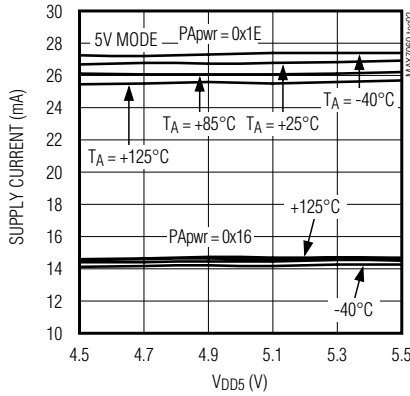
Typical Operating Characteristics

(Typical Application Circuit, 50Ω system impedance, V_{DD5} = V_{GPIOVDD} = V_{AVDD} = V_{DVDD} = V_{PAVDD} = 2.1V to 3.6V, f_{RF} = 280MHz to 450MHz, f_{XTAL} = 16MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD5} = V_{GPIOVDD} = V_{AVDD} = V_{DVDD} = V_{PAVDD} = 2.7V, T_A = +25°C, PA matched for optimum output power, unless otherwise noted. Supply current and output power are greatly dependent on board layout and PAOUT match.)

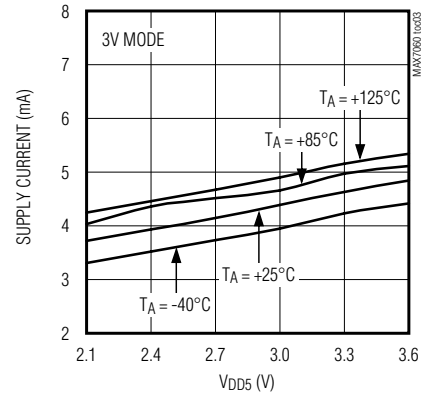
SUPPLY CURRENT vs. SUPPLY VOLTAGE
(f_{RF} = 315MHz, PA ON)



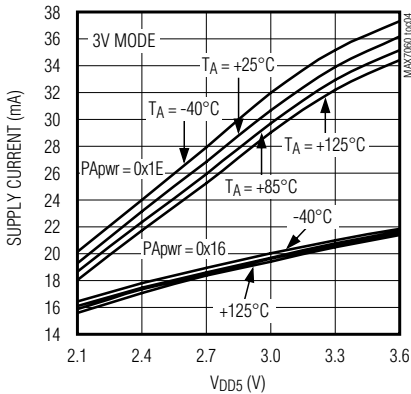
SUPPLY CURRENT vs. SUPPLY VOLTAGE
(f_{RF} = 315MHz, PA ON)



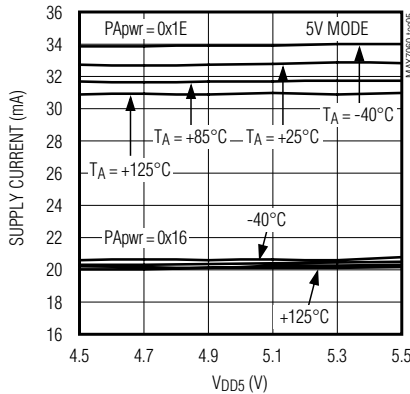
SUPPLY CURRENT vs. SUPPLY VOLTAGE
(f_{RF} = 315MHz, PA OFF)



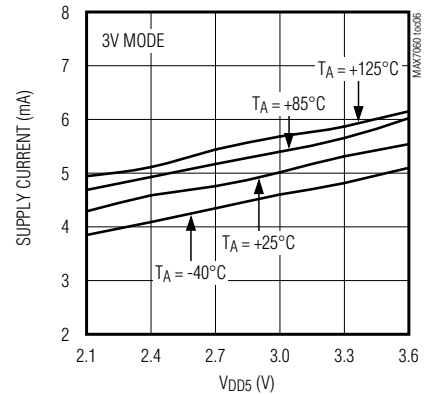
SUPPLY CURRENT vs. SUPPLY VOLTAGE
(f_{RF} = 433.92MHz, PA ON)



SUPPLY CURRENT vs. SUPPLY VOLTAGE
(f_{RF} = 433.92MHz, PA ON)



SUPPLY CURRENT vs. SUPPLY VOLTAGE
(f_{RF} = 433.92MHz, PA OFF)

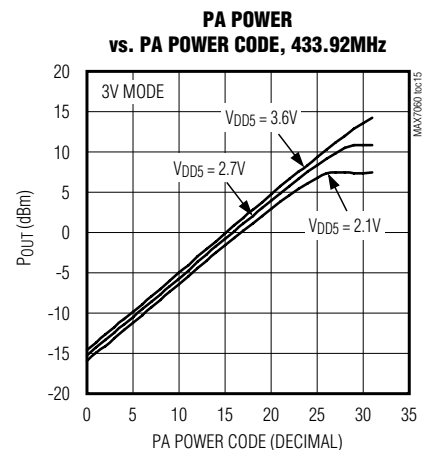
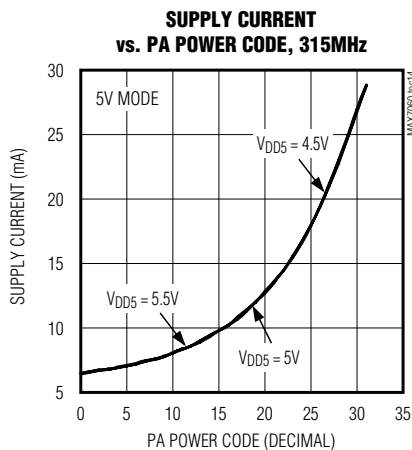
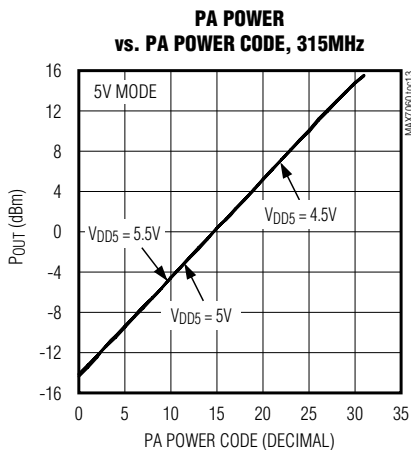
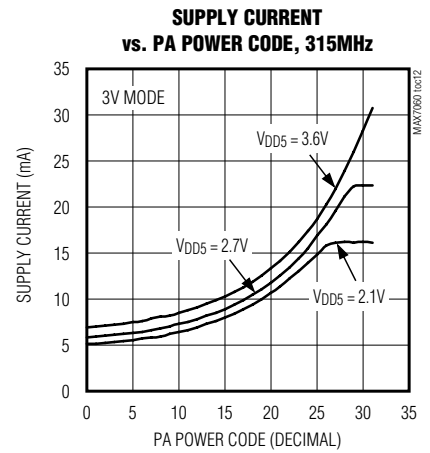
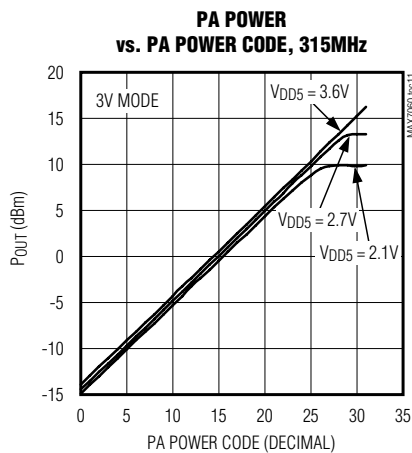
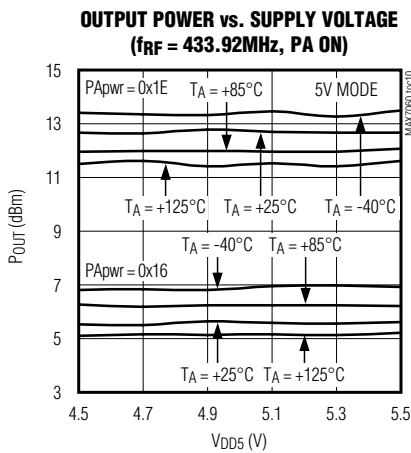
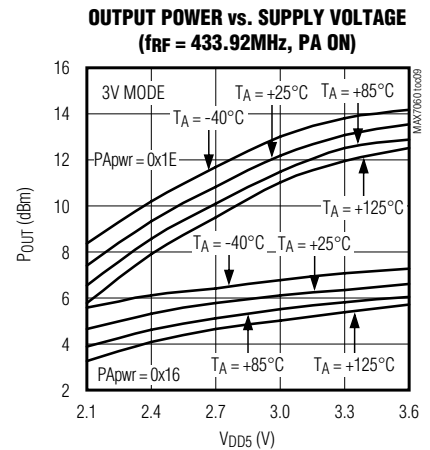
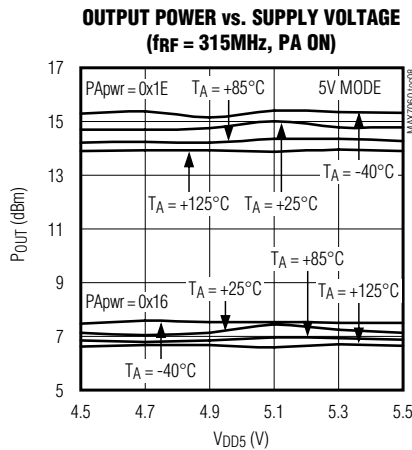
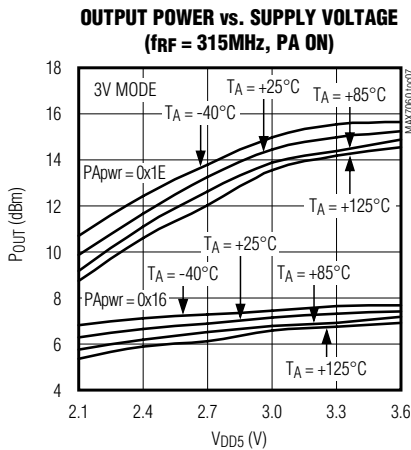


MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

Typical Operating Characteristics (continued)

(Typical Application Circuit, 50Ω system impedance, VDD5 = VGPOVDD = VAVDD = VD5VDD = VPAVDD = 2.1V to 3.6V, fRF = 280MHz to 450MHz, fXTAL = 16MHz, TA = -40°C to +125°C, unless otherwise noted. Typical values are at VDD5 = VGPOVDD = VAVDD = VD5VDD = VPAVDD = 2.7V, TA = +25°C, PA matched for optimum output power, unless otherwise noted. Supply current and output power are greatly dependent on board layout and PAOUT match.)

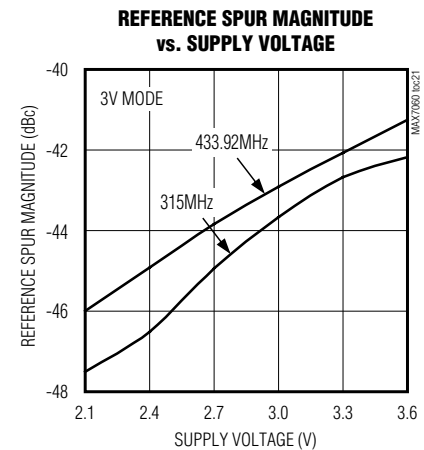
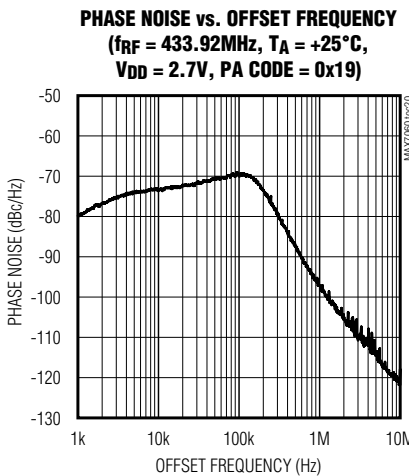
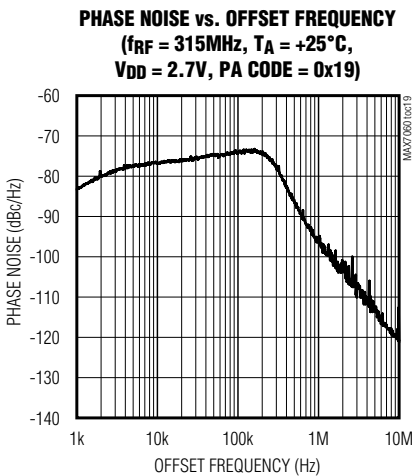
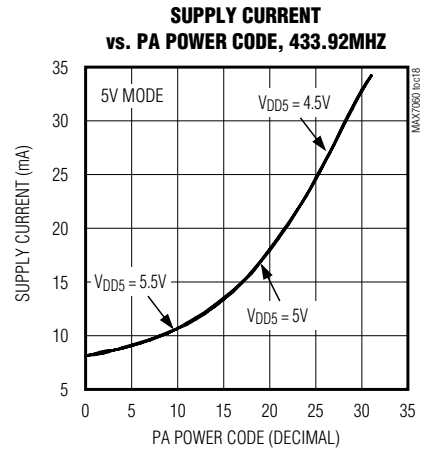
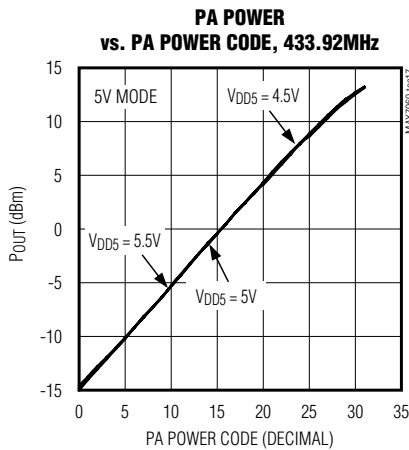
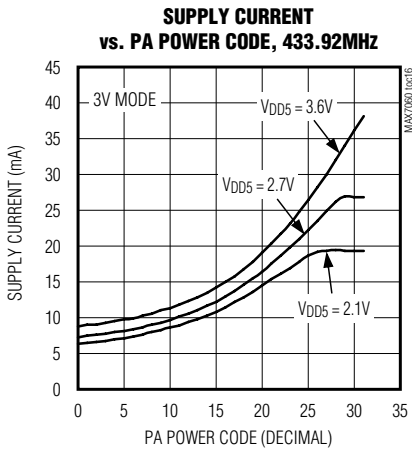


MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

Typical Operating Characteristics (continued)

(Typical Application Circuit, 50Ω system impedance, $V_{DD5} = V_{GPOVDD} = V_{AVDD} = V_{DVDD} = V_{PAVDD} = 2.1V$ to $3.6V$, $f_{RF} = 280MHz$ to $450MHz$, $f_{XTAL} = 16MHz$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. Typical values are at $V_{DD5} = V_{GPOVDD} = V_{AVDD} = V_{DVDD} = V_{PAVDD} = 2.7V$, $T_A = +25^{\circ}C$, PA matched for optimum output power, unless otherwise noted. Supply current and output power are greatly dependent on board layout and PAOUT match.)

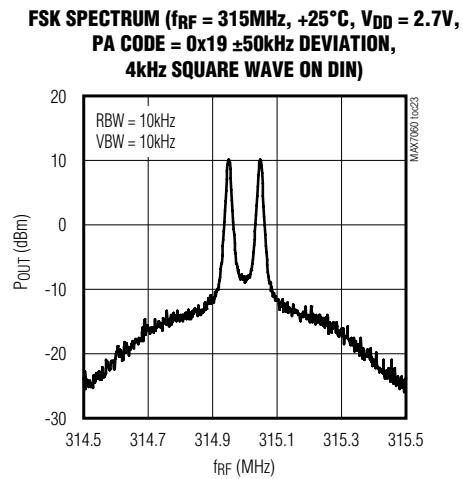
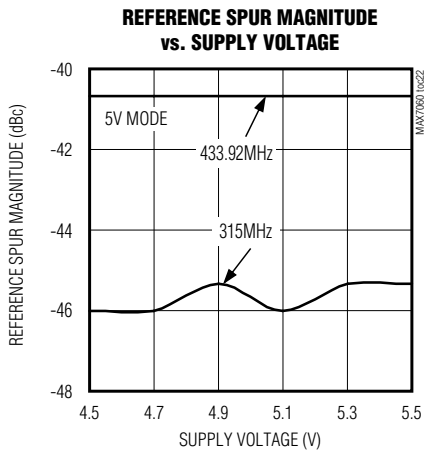


MAX7060

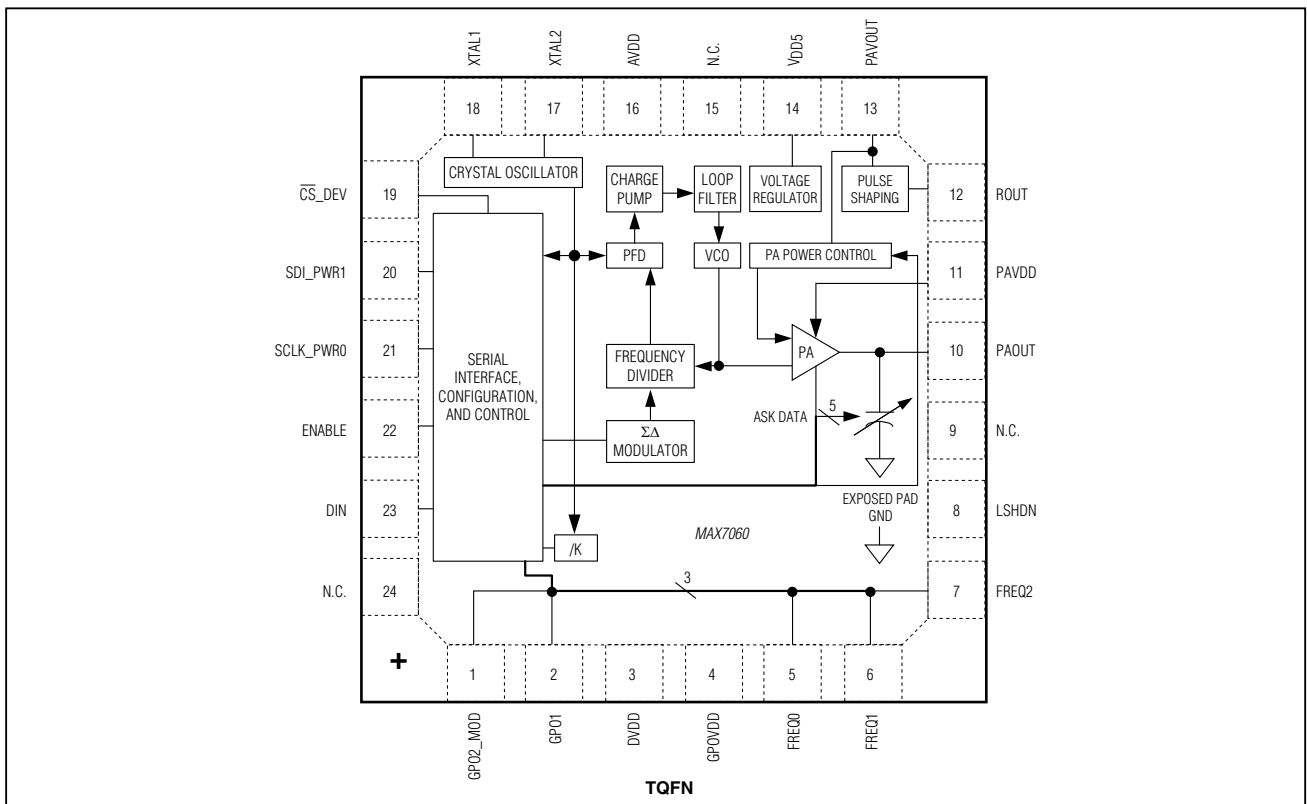
280MHz to 450MHz Programmable ASK/FSK Transmitter

Typical Operating Characteristics (continued)

(Typical Application Circuit, 50Ω system impedance, VDD5 = VGPOVDD = VAVDD = VD VDD = VPAVDD = 2.1V to 3.6V, f_{RF} = 280MHz to 450MHz, f_{XTAL} = 16MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at VDD5 = VGPOVDD = VAVDD = VD VDD = VPAVDD = 2.7V, T_A = +25°C, PA matched for optimum output power, unless otherwise noted. Supply current and output power are greatly dependent on board layout and PAOUT match.)



Pin Configuration/Functional Diagram



MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

Pin Description

| PIN | NAME | FUNCTION |
|-----------|-----------|---|
| 1 | GPO2_MOD | (SPI Mode/Manual Mode) Digital Input/Output. GPO2 output in SPI mode. Acts as an SPI data output when CS_DEV is low. ASK (0)/FSK (1) modulation select input in manual mode. This pin is internally pulled down in manual mode. |
| 2 | GPO1 | General-Purpose Output 1. In SPI mode, this pin can output many internal status signals. In manual mode, this pin outputs the synthesizer lock-detect (lockdet) signal. |
| 3 | DVDD | Digital-Supply Voltage Input. Bypass to GND with a 0.01μF capacitor as close as possible to the pin. |
| 4 | GPOVDD | Power-Supply Voltage Input for GPOs and ESD-Protection Devices. Bypass to GND with a 0.01μF capacitor as close as possible to the pin. |
| 5 | FREQ0 | Frequency-Select Pin 0 in Manual Mode. Internally pulled down. FREQ0 = FREQ1 = FREQ2 = 0 for SPI mode. |
| 6 | FREQ1 | Frequency-Select Pin 1 in Manual Mode. Internally pulled down. FREQ0 = FREQ1 = FREQ2 = 0 for SPI mode. |
| 7 | FREQ2 | Frequency-Select Pin 2 in Manual Mode. Internally pulled down. FREQ0 = FREQ1 = FREQ2 = 0 for SPI mode. |
| 8 | LSHDN | Low-Power Shutdown Current-Select Digital Input. Turns off internal POR circuit and disables pullup/pulldown currents. Must be driven low for normal operation in 3V mode. Functional only in 3V mode. Connect to GND in 5V mode. |
| 9, 15, 24 | N.C. | No Connection. Internally not connected. Leave unconnected. |
| 10 | PAOUT | Power Amplifier Output. Requires a pullup inductor to PAVOUT, which can be part of the output-matching network to an antenna. |
| 11 | PAVDD | Power Amplifier Predriver Power-Supply Input. Bypass to GND with a 680pF capacitor and a 0.01μF as close as possible to the pin. |
| 12 | ROUT | Envelope-Shaping Resistor Connection. See the <i>Typical Application Circuits</i> and the <i>ASK Envelope Shaping</i> sections for details. |
| 13 | PAVOUT | Power Amplifier Power-Control Output. Controls the transmitted power. Connect to PA pullup inductor. Bypass to ground with 680pF capacitor. |
| 14 | VDD5 | Supply Voltage Input. Bypass to ground with 0.01μF and 0.1μF capacitors. |
| 16 | AVDD | Analog Supply Voltage and Regulator Output. Bypass to GND with 0.1μF and 0.01μF capacitors as close as possible to the pin. |
| 17 | XTAL2 | Crystal Input 2. XTAL2 can be driven from an AC-coupled external reference. |
| 18 | XTAL1 | Crystal Input 1. AC-couple to GND if XTAL2 is driven from an AC-coupled external reference. |
| 19 | CS_DEV | (SPI Mode/Manual Mode) Serial Peripheral Interface (SPI) Active-Low Chip-Select Input. FSK frequency-deviation input (0 = low deviation, 1 = high deviation) in manual mode. Internally pulled up. |
| 20 | SDI_PWR1 | (SPI Mode/Manual Mode) SPI Data Input in SPI Mode. Power-control MSB input in manual mode. Internally pulled down. |
| 21 | SCLK_PWR0 | (SPI Mode/Manual Mode) SPI Clock Input in SPI Mode. Power-control LSB input in manual mode. Internally pulled down. |
| 22 | ENABLE | Enable Digital Input. All internal circuits (except the PA in ASK mode) are enabled on the rising edge of ENABLE. Internally pulled down. |
| 23 | DIN | Transmit Data Digital Input. Internally pulled down. |
| — | EP | Exposed Pad. Solder evenly to the board's ground plane for proper operation. |

MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

Detailed Description

The MAX7060 is power and frequency programmable from 280MHz to 450MHz. The MAX7060 has an internal transmit power control that can be programmed over a 28dB power range. The MAX7060 has tuning capacitors at the output of the power amplifier (PA) to ensure high-power efficiency at various programmable frequencies with a single matching network.

The crystal-based architecture of the MAX7060 eliminates many of the common problems with SAW transmitters by providing greater modulation depth, faster frequency settling, tighter tolerance of the transmit frequency, and reduced temperature dependence. In particular, the tighter transmit frequency tolerance means that a superheterodyne receiver with a narrower IF bandwidth (therefore lower noise bandwidth) can be used. The payoff is better overall receiver performance when using a superheterodyne receiver such as the MAX1473, MAX1471, MAX7033, MAX7034, MAX7036, and MAX7042.

The MAX7060 can be configured in either SPI or manual mode, where the transmitter can easily be configured without the need of an SPI interface.

In the 3V operation, the MAX7060 can be put in a low-power shutdown mode by pulling ENABLE low and LSHDN high. In this mode, all the blocks are shut down including power-on reset (POR). All the MAX7060 registers must be reprogrammed after LSHDN is asserted high. In the 5V operation, the low-power shutdown mode is not available, and LSHDN should be connected to GND.

Frequency Programming

The MAX7060 is a crystal-referenced phased-locked-loop (PLL) VHF/UHF transmitter that transmits data over a wide frequency range. The internal VCO can be tuned from 280MHz to 450MHz and controlled by a single crystal to cover up to a 1.47:1 carrier-frequency range. The transmit frequency is set by the crystal frequency and the programmable divider in the PLL; the programmable PLL divide ratios can be set anywhere from 19 to 28, which means that with a crystal frequency of 15MHz, the output is 285MHz to 420MHz. With a crystal frequency of 16MHz, the output is 304MHz to 448MHz.

The MAX7060 has an internal variable capacitor connected across the PA output. This capacitor can be programmed to maintain high-efficiency transmission at any frequency within a 1.47 to 1 (28/19) tuning range. This

means that it is possible to change the frequency and retune the antenna to the new frequency in a very short time. The combination of rapid antenna-tuning ability with rapid synthesizer tuning makes the MAX7060 a true frequency-agile transmitter. The tuning capacitor has a nominal resolution of 0.25pF, from 0 to 7.75pF.

The MAX7060 supports data rates up to 100kbps NRZ in ASK mode and 140kbps NRZ in FSK mode. In FSK mode, the frequency deviation corresponding to bit 1 and bit 0 can be set as low as ± 2 kHz, and as high as ± 100 kHz. The frequency deviation is fully programmable in SPI mode, and can be selected either as ± 16 kHz or ± 50 kHz in manual mode.

Power Amplifier (PA)

The PA of the MAX7060 is a high-efficiency, open-drain switching-mode amplifier. In a switching-mode amplifier, the gate of the final-stage FET is driven with a very sharp 25% duty-cycle square wave at the transmit frequency. This square wave is derived from the synthesizer circuit. When the matching network is tuned correctly, the output FET resonates the attached tank circuit with a minimum amount of power dissipated in the FET. With a proper output-matching network, the PA can drive a wide range of antenna impedances, which include a small-loop PCB trace and a 50 Ω antenna. The output-matching network suppresses the carrier harmonics and transforms the antenna impedance to an optimal impedance at PAOUT, which is from 60 Ω to 125 Ω . When the output-matching network is properly tuned, the MAX7060 transmits power with a high overall efficiency. The efficiency of the PA itself is approximately 50%.

Transmitter Power Control

The transmitter power of the MAX7060 can be set in approximately 1dB steps (SPI mode) to produce a maximum output power level of +14dBm with a 5V supply. If a battery is used as the supply, the maximum output power level varies from +15dBm at 3.6V to +10dBm at 2.1V. The minimum power level is -14dBm for both 5V and battery supplies. The maximum transmitter power (and the transmitter current) can be lowered by increasing the load impedance on the PA. Four fixed power levels are available in manual mode.

When a 5V supply is used, the VDD5 and GPOVDD pins are connected to the 5V supply. AVDD is the output of an internal voltage regulator and must be connected externally to DVDD and PAVDD. The PAVOUT pin is connected to the PAOUT pin through a biasing inductor. PAVOUT is not connected to any of the power-supply

MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

pins. Connecting PAVOUT to PAOUT enables Tx power control. In SPI mode, there are 31 power-control settings in approximately 1dB monotonic steps. In manual mode, four power-control settings are available.

ASK Envelope Shaping

The MAX7060 has two types of ASK envelope shaping: digital shaping (SPI mode only) and analog shaping through an internal resistor. Envelope shaping results in a smaller spectral width of the modulated PA output signal.

In digital shaping, the user can choose the final Tx power setting, the power step size in units as small as 1dB, and the step-time interval in units as small as 0.25 μ s, when a 16MHz crystal is used. This shaping method causes the PA to transmit an envelope that rises linearly in decibels (exponentially in power) with time. Digital shaping is programmed through the SPI.

The analog shaping mode uses an internal envelope-shaping resistor for ASK modulation, which connects between PAVOUT and ROUT. When the ROUT pin (rather than the PAVOUT pin) is connected to the PA pullup inductor, the envelope-shaping resistor slows the turn-on/turn-off time of the PA. The user can choose two turn-on/turn-off times through the SPI. A single turn-on/turn-off time is set internally in manual mode.

It should be noted that, by default, data pulses applied to the DIN pin are internally lengthened by 64 crystal clock cycles (4 μ s for a 16MHz crystal) to allow time for the analog shaping to occur. For cases in which no analog shaping is desired, the PA pullup inductor must be connected to PAVOUT and the analog shaping bits in the Conf0 register set to either anshp[1:0] = 00, which leaves the extra 4 μ s pulse extension in place, or to anshp[1:0] = 11, which removes the extra 4 μ s and allows transmitted pulses to track the data present at the DIN pin. If digital shaping is used, the PA pullup inductor must be connected to PAVOUT and there is no 4 μ s pulse extension, regardless of the status of the anshp[1:0] bits.

At low data rates, where shaping is not necessary and the 4 μ s pulse lengthening has minimal impact on duty cycle symmetry, it may be acceptable to use the default configuration of anshp[1:0] = 00. For higher data rates, it may be necessary to use anshp[1:0] = 11, to avoid duty cycle skew. Another method to remove the pulse lengthening is to apply a minimal amount of digital shaping, by setting tstep[3:0] = 0001 and selecting pastep[4:0] = papwr[4:0].

Variable Capacitor

The MAX7060 has an internal set of capacitors that can be switched in and out to present different capacitor values at the PA output. The capacitors are connected from the PA output to ground. This allows changing the tuning network along with the synthesizer divide ratio each time the transmitted frequency changes, making it possible to maintain maximum transmitter power while moving rapidly from one frequency to another.

In SPI mode, the variable capacitor is programmed through a register setting. In manual mode, the capacitor setting is programmed through the DIN pin.

The tuning capacitor has a nominal resolution of 0.25pF, from 0 to 7.75pF.

Phase-Locked Loop (PLL)

The MAX7060 utilizes a fully integrated fractional-N PLL for its frequency synthesizer. All PLL components, including the loop filter, are included on-chip. Two loop bandwidths can be selected in SPI mode. The synthesizer has 16-bit fractional-N topology (4 bits integer, 12 bits fractional) with a divide ratio that can be set from 19 to 28, allowing the transmit frequency to be adjusted in increments of $f_{XTAL}/4096$.

The fractional-N architecture also allows exact FSK frequency deviations to be programmed, completely eliminating the problems associated with generating frequency deviations by crystal oscillator pulling.

FSK deviations as low as ± 2 kHz and as high as ± 100 kHz can be set in SPI mode. In manual mode, the user can select between ± 16 kHz and ± 50 kHz.

The integer and fractional portions of the PLL divider ratio set the transmit frequency. This is done by loading the divide-ratio registers in SPI mode, or selecting the states of the three frequency-control pins (FREQ2, FREQ1, FREQ0) in manual mode. For ASK modulation, the two 8-bit center-frequency registers (fce[15:0]) are loaded with the divide ratio determined by the center frequency and the crystal. For FSK modulation, the two 8-bit high (mark) frequency registers (fhi[15:0]) and the two 8-bit low (space) frequency registers (flo[15:0]) are loaded. The divide ratios for the fhi and flo are determined by the center frequency, the frequency deviation, and the crystal frequency. Examples of typical settings for ASK and FSK modulation are given in the *SPI Mode Settings* section.

MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

Crystal (XTAL) Oscillator

The XTAL oscillator in the MAX7060 is designed to present a capacitance of approximately 6pF between the XTAL1 and XTAL2 pins. In most cases, this corresponds to a 8pF load capacitance applied to the external crystal when typical PCB parasitics are added. It is very important to use a crystal with a load capacitance equal to the capacitance of the MAX7060 crystal oscillator plus PCB parasitics. If a crystal designed to oscillate with a different load capacitance is used, the crystal is pulled away from its stated operating frequency, introducing an error in the reference frequency. A crystal designed to operate at a higher load capacitance than the value specified for the oscillator is always pulled higher in frequency. Adding capacitance to increase the load capacitance on the crystal increases the startup time and can prevent oscillation altogether.

In actuality, the oscillator pulls every crystal. The crystal's natural frequency is really below its specified frequency, but when loaded with the specified load capacitance, the crystal is pulled and oscillates at its specified frequency. This pulling is already accounted for in the specification of the load capacitance.

Additional pulling can be calculated if the electrical parameters of the crystal are known. The frequency pulling is given by:

$$f_P = \frac{C_M}{2} \left(\frac{1}{C_{CASE} + C_{LOAD}} - \frac{1}{C_{CASE} + C_{SPEC}} \right) \times 10^6$$

where:

f_P is the amount the crystal frequency pulled in ppm

C_M is the motional capacitance of the crystal

C_{CASE} is the case capacitance

C_{SPEC} is the specified load capacitance

C_{LOAD} is the actual load capacitance

When the crystal is loaded as specified (i.e., $C_{LOAD} = C_{SPEC}$), the frequency pulling equals zero.

General-Purpose Output (GPO)/Clock Outputs

The MAX7060 has two GPO pins in SPI mode (GPO2_MOD and GPO1) and one GPO in manual mode (GPO1).

The GPO1 pin can serve as a clock for a microprocessor or any other GPO function in SPI mode. In manual mode, this pin outputs the synthesizer lock-detect (lockdet) status, after which the user can send data through the DIN pin.

The GPO2_MOD pin acts as the SPI data output when the $\overline{CS_DEV}$ pin is low, in SPI mode. When $\overline{CS_DEV}$ is high, it acts as a GPO that can output various internal signals, such as the synthesizer lock detect (lockdet).

In SPI mode, the output clock that can be routed through GPO1 is a divided version of the crystal frequency. The divide ratio is set through the MAX7060 registers, and the divide settings are 1 (no division), 2, 4, 8, or 16. When driving an output clock through GPO1, the gp1bst bit (register Conf0, address 0x01, bit 6) can be set to 1 to increase GPO1 drive strength. If even more drive capability is required, the user should provide an external buffer.

Serial Peripheral Interface (SPI)

The MAX7060 utilizes a 4-wire SPI protocol for programming its registers, configuring and controlling the operation of the whole transmitter. For SPI operation, the FREQ2, FREQ1, and FREQ0 pins must be reset to 0.

The following digital I/Os control the operation of the SPI:

| | |
|----------------------|----------------------------|
| $\overline{CS_DEV}$ | Active-low SPI chip select |
| SDI_PWR1 | SPI data Input |
| SCLK_PWR0 | SPI clock |
| GPO2_MOD | SPI data output |

Figure 2 shows the general timing diagram of the SPI protocol.

Any number of 8-bit data bursts (Data 1, Data 2 ... Data n) can be sent within one cycle of the $\overline{CS_DEV}$ pin, to allow for burst-write or burst-read operations. The SPI data output signal is routed through the GPO2_MOD pin when $\overline{CS_DEV}$ is low.

MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

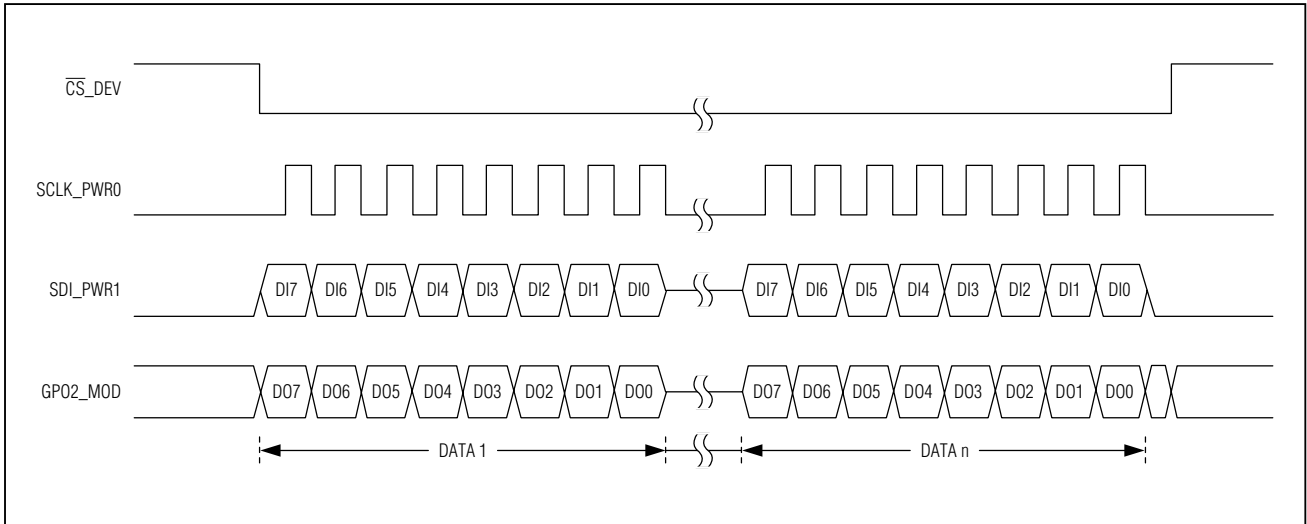


Figure 2. SPI Format

SPI Commands

The following commands are implemented in the MAX7060:

Write: Within the same $\overline{CS_DEV}$ cycle, a write command is implemented as follows:

SDI_PWR1: <0x01> <Initial Address> <Data 1> <Data 2> ... <Data N>

With this command, Data 1 is written to the address given by <Initial Address>, Data 2 is written to <Initial Address + 1>, and so on.

Read: Within the same $\overline{CS_DEV}$ cycle, a read command is implemented as follows:

SDI_PWR1: <0x02> <Address 1> <Address 2> <Address 3> ... <Address N> <0x00>

GPO2_MOD: <0xXX> <0xXX> <Data 1> <Data 2> ... <Data N - 1> <Data N>

With this command, all the registers can be read within the same cycle of $\overline{CS_DEV}$. The addresses can be given in any order.

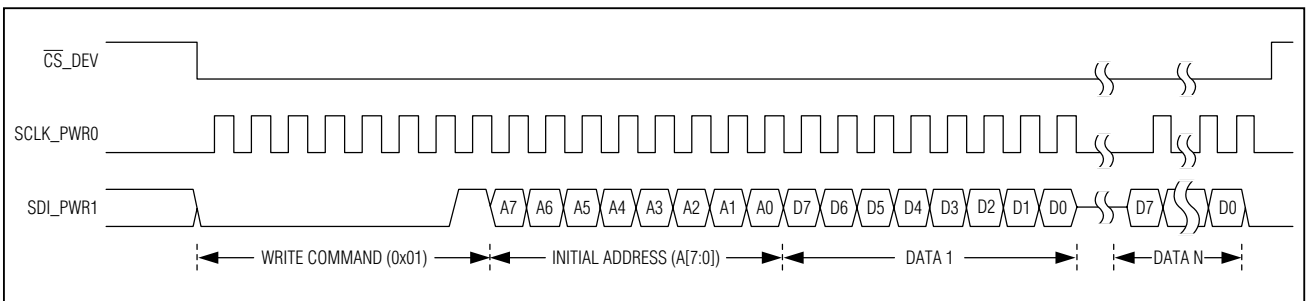


Figure 3. SPI Write Command Format

MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

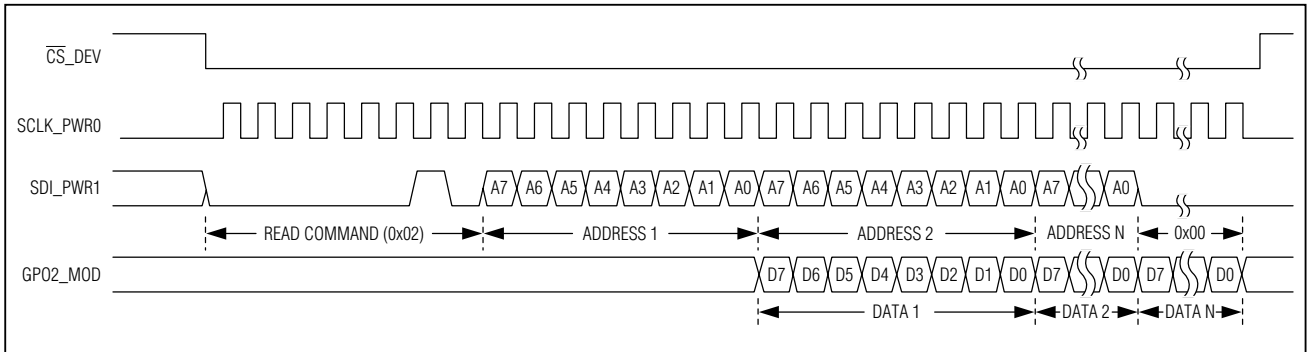
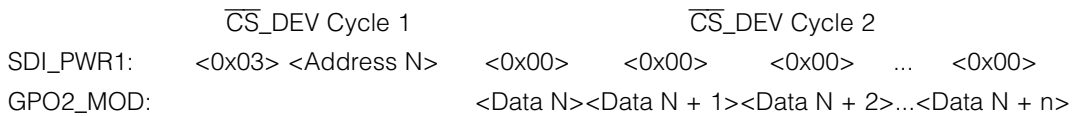


Figure 4. SPI Read Command Format

Read All: Within two $\overline{CS_DEV}$ cycles, the read-all command is implemented as follows:



Reset: An SPI reset command is implemented as follows:

SDI_PWR1: <0x04>

An internal active-low master reset pulse is generated, from the falling edge of the last SCLK_PWR0 signal to the falling edge of the following $\overline{CS_DEV}$ signal ($t_{HCS} + t_{CSH}$).

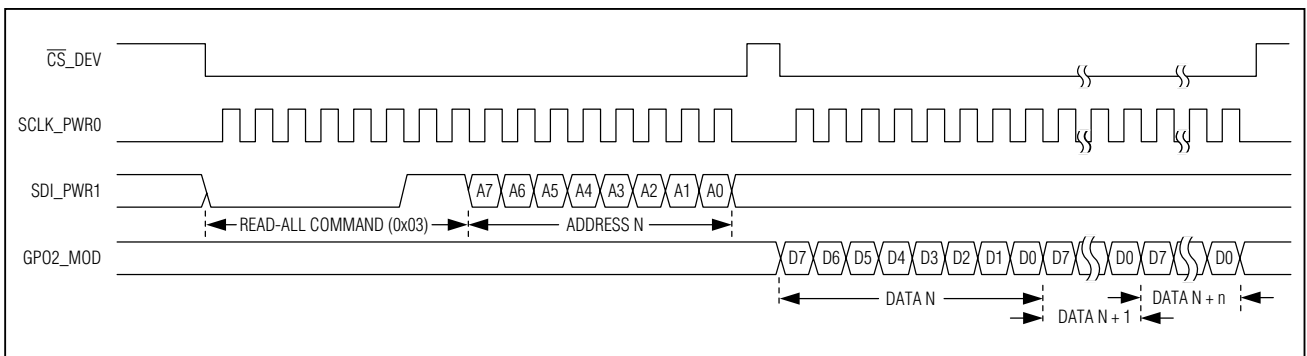


Figure 5. SPI Read-All Command Format

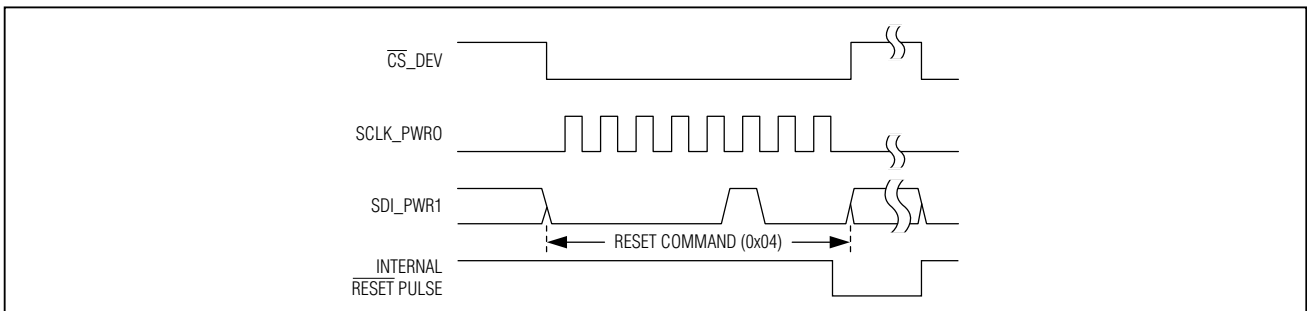


Figure 6. SPI Reset Command Format

MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

Applications Information

SPI Mode Settings

ASK Carrier Frequency

When the MAX7060 is in ASK mode, only the carrier frequency needs to be set. To do this, the user calculates the divide ratio based on the carrier frequency and crystal frequency. The example below shows how to determine the correct value to be loaded into the carrier-frequency registers (fce[15:0]).

Due to the nature of the transmit PLL frequency divider, a fixed offset of 16 must be subtracted from the transmit PLL divider ratio for programming the MAX7060's transmit-frequency registers. To determine the value to program the MAX7060's transmit-frequency registers, convert the decimal value of the following equation to the nearest hexadecimal value:

$$\left(\frac{f_{RF}}{f_{XTAL}} - 16 \right) \times 4096 = \text{decimal value to program the transmit-frequency registers}$$

Assume the ASK transmit frequency = 315MHz and fXTAL = 16MHz. In this example, the rounded decimal value is 15,104 or 0x3B00. The upper byte (0x3B) is loaded into the FCenter0 register (fce[15:8]) and the lower byte (0x00) is loaded into the FCenter1 register (fce[7:0]).

FSK Mark and Space Frequencies

When the MAX7060 is in FSK mode, two frequencies need to be set: the mark (logical 1) frequency and the space (logical 0) frequency. In most cases, the two frequencies are above and below the carrier frequency by the deviation frequency. Therefore, the user needs to calculate the divide ratio for both frequencies and load them into four registers. The procedure for calculating the register settings is the same as it is for calculating the carrier frequency. The example below shows how to determine the register settings for the mark and space frequencies when the frequency deviation is ±50kHz (100kHz between mark and space).

Assume that, for an FSK transmitter centered at 433.92MHz, the mark frequency is 433.97MHz, the space frequency is 433.87MHz, and the crystal frequency is 16MHz. In this example, the rounded decimal value for the mark frequency is 45,560 or 0xB1F8. For the space frequency, the rounded decimal value is 45,535 or 0xB1DE. The mark setting is loaded into the FHigh0 and FHigh1 registers (fhi[15:0]), and the space setting is loaded into the FLow0 and FLow1 registers (flo[15:0]).

Transmit Power Settings (5V Supply)

The output power level is set by entering a 5-bit value into the PApwr register (papwr[4:0]). The highest setting (30dec or 0x1E) corresponds to the highest transmitted power level. Each step is slightly less than 1dB (approximately 0.95dB), with the lowest setting producing a transmitted power 28dB lower than the highest. The highest transmitted power depends on the load presented to the PA output. A 50Ω or 60Ω load produces an output power level of +14dBm to +15dBm when the highest papwr[4:0] setting (0x1E) is applied. Increasing the load resistance reduces the output power level. Reducing the setting by one step reduces the power by approximately 1dB, and the minimum transmitted power is still about 28dB below the maximum. For example, if the load resistance is increased to the point where the output power for the maximum setting (0x1E) is +10dBm, then the minimum setting (0x00) produces an output power of about -18dBm.

Transmit Power Settings (3V Supply)

The output power level in 3V operation is set the same way as in 5V operation, but the variation in the 3V supply (the specified range is 2.1V to 3.6V) affects the maximum power that can be transmitted. If the supply is 3.6V, then the maximum papwr[4:0] setting (0x1E) still produces a +14dBm to +15dBm transmitted power level. As the supply voltage decreases, the transmitted power at the highest settings is compressed, so that the top setting and an increasing number of the lower settings produce the same transmitted power, which is lower than the +14dBm to +15dBm achieved with a 3.6V supply. For example, a 2.7V supply produces a maximum transmitter power of +12dBm to +13dBm, and the PApwr register settings from 0x1B to 0x1E (27dec to 30dec) produce the same transmitter power. Below this compressed range, the power settings give the same power levels that they would give with a 5V supply. At the lowest supply level of 2.1V, the maximum setting produces a maximum transmitter power of +10dBm, and the PApwr register settings from 0x19 to 0x1E (25dec to 30dec) produce the same transmitter power. The effect of a lower supply voltage reduces the maximum power and the adjustment range. The power at the lowest setting remains unchanged.

The transmitted power using a 3V supply can be set higher than the levels described in the paragraph above by connecting PAOUT directly to PAVDD and disconnecting (leave open) the PAVOUT pin. The tradeoff of this connection is that there is no transmit power adjustment.

MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

ASK Amplitude Shaping

At data rates higher than 30kbps Manchester (60kbps NRZ), it may be necessary to shape the ASK transmitter pulses to reduce the occupied bandwidth of the transmitted signal to comply with government regulations (FCC in the U.S., ETSI in Europe). There is no shaping of the FSK modulation. The MAX7060 has two forms of amplitude shaping: digital and analog.

Digital Amplitude Shaping

The digital shaping feature allows the user to choose a linear stairstep function to increase and decrease the power when the PA is turned on and off for an ASK bit interval. There are three registers that control the digital amplitude shaping settings. The first setting is the final power of the PA when the pulse reaches its maximum (PApwr register). The second setting is the amplitude change, in decibels, for each step, which is the vertical axis of the stairstep (PAstep register). The third setting is the time interval of each step, which is the horizontal axis of the stairstep (Tstep register). The final power setting (decimal 0 to 30 in increments of 1dB) is entered in the PApwr register. The amplitude step (decimal 0 to 30 in increments of 1dB) is entered in the PAstep register. The time interval (decimal 0 to 60/fXTAL in increments of 4/fXTAL) is entered in the Tstep register. For example, to shape an 80kbps NRZ data stream (12.5µs bit interval), the user might choose a maximum power level of 0x1E (30dec), an amplitude step of 5dB, and a time interval of 0.5µs assuming a crystal frequency of 16MHz. This would produce an ASK pulse that ramps up in 3µs, levels off for 9.5µs, and ramps down in 3µs. Because the amplitude steps are in decibels, the shape of the pulse rise and fall is exponential on a linear display (an oscilloscope, for instance). Because most ASK receivers use a logarithmic amplitude detector, the demodulated pulse

has a linear ramp shape. The digital shaping is disabled when the Tstep register is 0x00.

If no shaping of any kind is used (digital or analog), the PA pullup inductor must be connected to PAVOUT and the analog shaping bits in the Conf0 register must also be set to either anshp[1:0] = 00 or to anshp[1:0] = 11, as described in the *ASK Envelope Shaping* section.

Analog Amplitude Shaping

To use the analog shaping feature, the user must connect the bias inductor to the ROUT pin instead of directly to the PAVOUT pin. This places a MOS resistor between PAVOUT and ROUT, which slows down the application of the PAVOUT voltage to the drain of the PA FET when the PA is turned on. There are two settings in the anshp[1:0] bits in the Conf0 register for the rate at which the pulse ramps up: anshp[1:0] = 10 is approximately 1.5µs and anshp[1:0] = 01 is approximately 3µs. The anshp[1:0] = 11 setting turns analog shaping off and removes the 4µs pulse extension, while the anshp[1:0] = 00 setting opens the connection between PAVOUT and ROUT.

Tuning Capacitor Settings

The internal variable shunt capacitor, which can be used to match the PA to the antenna with changing transmitter frequency, is controlled by setting the 5-bit cap variable in the registers. This allows for 32 levels of shunt capacitance control. Since the control of these 5 bits is independent of the other settings, any capacitance value can be chosen at any frequency, making it possible to maintain maximum transmitter efficiency while moving rapidly from one frequency to another. The internal tuning capacitor adds 0 to 7.75pF to the PA output in 0.25pF steps. The PA output capacitance at the minimum cap setting is approximately 4.5pF.

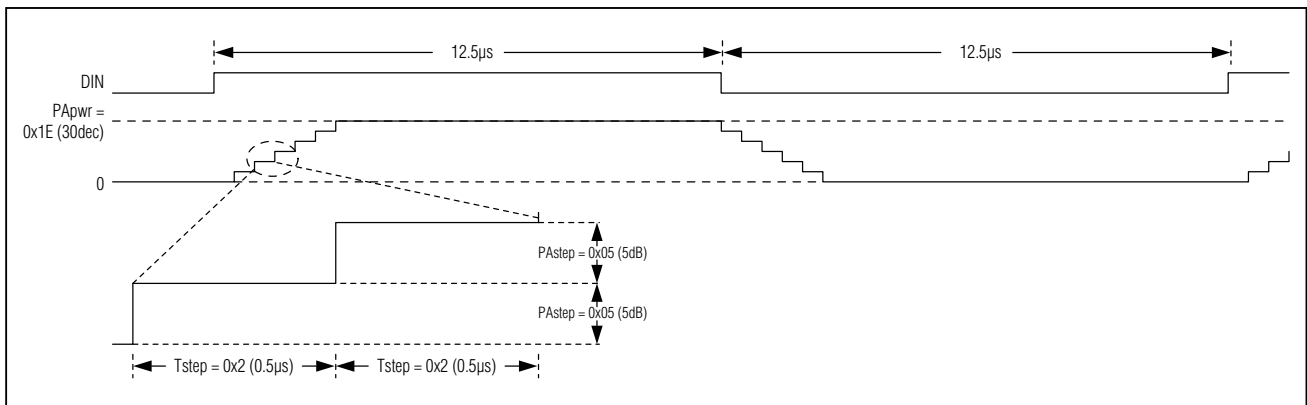


Figure 7. Digital Amplitude Shaping Timing Diagram

MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

Register Details

The following tables provide information on the MAX7060 registers.

Table 1. Register Summary

| REGISTER | ADDRESS | DESCRIPTION |
|-----------|---------|---|
| Ident | 0x00 | Read-only register used for identification purpose. The content of this register is always 0xA6. |
| Conf0 | 0x01 | Configuration 0 register. Controls the GPO1 boost mode, PLL bandwidth, analog shaping, crystal clock output, and the modulation mode (ASK/FSK). |
| Conf1 | 0x02 | Configuration 1 register. Controls the clock output frequency divider and the capacitance at the PA output. |
| Conf2 | 0x03 | Configuration 2 register. Controls the emulation mode. |
| IOConf0 | 0x04 | IO configuration 0 register. Selects the status register bus for SPI operation. |
| IOConf1 | 0x05 | IO configuration 1 register. Selects the outputs of GPO1 and GPO2_MOD pins. |
| Tstep | 0x06 | Digital shaping time step register. Controls the time step in the digital shaping. |
| PAstep | 0x07 | Digital shaping power step register. Controls the power step in the digital shaping. |
| PAPwr | 0x08 | Final power register. Controls the final output power. |
| FHigh0 | 0x09 | High-frequency 0 register (upper byte). Sets the high frequency in FSK transmission. |
| FHigh1 | 0x0A | High-frequency 1 register (lower byte). Sets the high frequency in FSK transmission. |
| FCenter0 | 0x0B | Center-frequency 0 register (upper byte). Sets the carrier frequency in ASK transmission. |
| FCenter1 | 0x0C | Center-frequency 1 register (lower byte). Sets the carrier frequency in ASK transmission. |
| FLow0 | 0x0D | Low-frequency 0 register (upper byte). Sets the low frequency in FSK transmission. |
| FLow1 | 0x0E | Low-frequency 1 register (lower byte). Sets the low frequency in FSK transmission. |
| FLoad | 0x0F | Frequency-load register. Performs the frequency-load function. |
| EnableReg | 0x10 | Enable register. Register equivalent of ENABLE pin. |
| DataReg | 0x11 | Data register. Register equivalent of DIN pin. |
| Status | 0x12 | Status register |

Table 2. Configuration Registers

| REGISTER | ADDRESS | DATA | | | | | | | | MODE |
|----------|---------|---------|---------|---------|---------|---------|---------|---------|---------|------|
| | | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| Ident | 0x00 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | R |
| Conf0 | 0x01 | — | gp1bst | pllbw | anshp_1 | anshp_0 | clksby | clkout | mode | R/W |
| Conf1 | 0x02 | ckdiv_2 | ckdiv_1 | ckdiv_0 | cap_4 | cap_3 | cap_2 | cap_1 | cap_0 | R/W |
| Conf2 | 0x03 | fixed | fxmode | fxpwr_1 | fxpwr_0 | fxhdev | fxfrq_2 | fxfrq_1 | fxfrq_0 | R/W |
| IOConf0 | 0x04 | — | — | — | — | — | tmux_2 | tmux_1 | tmux_0 | R/W |
| IOConf1 | 0x05 | — | gp2s_2 | gp2s_1 | gp2s_0 | — | gp1s_2 | gp1s_1 | gp1s_0 | R/W |
| Tstep | 0x06 | — | — | — | — | tstep_3 | tstep_2 | tstep_1 | tstep_0 | R/W |
| PAstep | 0x07 | — | — | — | pastp_4 | pastp_3 | pastp_2 | pastp_1 | pastp_0 | R/W |
| PAPwr | 0x08 | — | — | — | papwr_4 | papwr_3 | papwr_2 | papwr_1 | papwr_0 | R/W |
| FHigh0 | 0x09 | fhi_15 | fhi_14 | fhi_13 | fhi_12 | fhi_11 | fhi_10 | fhi_9 | fhi_8 | R/W |
| FHigh1 | 0x0A | fhi_7 | fhi_6 | fhi_5 | fhi_4 | fhi_3 | fhi_2 | fhi_1 | fhi_0 | R/W |
| FCenter0 | 0x0B | fce_15 | fce_14 | fce_13 | fce_12 | fce_11 | fce_10 | fce_9 | fce_8 | R/W |
| FCenter1 | 0x0C | fce_7 | fce_6 | fce_5 | fce_4 | fce_3 | fce_2 | fce_1 | fce_0 | R/W |

MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

Table 2. Configuration Registers (continued)

| REGISTER | ADDRESS | DATA | | | | | | | | |
|-----------|---------|----------|----------|----------|----------|----------|----------|----------|----------|------|
| | | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | MODE |
| FLow0 | 0x0D | flo_15 | flo_14 | flo_13 | flo_12 | flo_11 | flo_10 | flo_9 | flo_8 | R/W |
| FLow1 | 0x0E | flo_7 | flo_6 | flo_5 | flo_4 | flo_3 | flo_2 | flo_1 | flo_0 | R/W |
| FLoad | 0x0F | — | — | — | — | — | — | — | hop | R/W |
| EnableReg | 0x10 | — | — | — | — | — | — | — | enable | R/W |
| DataReg | 0x11 | — | — | — | — | — | — | — | datain | R/W |
| Status | 0x12 | status_7 | status_6 | status_5 | status_4 | status_3 | status_2 | status_1 | status_0 | R |

Table 3. Identification (Ident) Register (Address: 0x00)

| BIT | NAME | FUNCTION |
|-----|-------|--|
| 7:0 | ident | Read-only register used for identification purpose. The content of this register is always 0xA6. |

Table 4. Configuration 0 (Conf0) Register (Address: 0x01)

| BIT | NAME | FUNCTION |
|-----|------------|--|
| 6 | gp1bst | 0 = Normal GPO1 output driver 1 = Extended driving capability on GPO1 |
| 5 | pllbw | PLL bandwidth setting, low (0) = 300kHz or high (1) = 600kHz; 300kHz is recommended for fractional-N and 600kHz for fixed-N (ASK mode only) |
| 4:3 | anshp[1:0] | Control time constants of the analog shaping (bias inductor connected to the ROUT pin) anshp[1:0] Rise/fall time 00 ROU _T open-circuited, 4μs pulse extension present 01 nominal 3.0μs rise/fall time 10 nominal 1.5μs rise/fall time 11 no analog shaping, no 4μs pulse extension |
| 2 | clksby | Crystal clock output enable (1) while part is in standby mode |
| 1 | clkout | Crystal clock output enable (1) on GPO1 output, gp1s[2:0] = 0x2 |
| 0 | mode | ASK (0) or FSK (1) |

Table 5. Configuration 1 (Conf1) Register (Address: 0x02)

| BIT | NAME | FUNCTION |
|-----|------------|--------------------------------------|
| 7:5 | ckdiv[2:0] | 3-bit clock output frequency divider |
| 4:0 | cap[4:0] | 5-bit capacitor setting |

Table 6. Crystal Divide Settings for Clock Output

| ckdiv[2:0] | CRYSTAL FREQUENCY DIVIDED BY |
|------------|------------------------------|
| 000 | 1 |
| 001 | 2 |
| 010 | 4 |
| 011 | 8 |
| 1XX | 16 |

MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

Table 7. Configuration 2 (Conf2) Register (Address: 0x03)

| BIT | NAME | FUNCTION | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|---------------------------|---|------------|---------------------------|--------------|-----|-----|-----|-----|--------|----------|-----|--------|----------|-----|--------|----------|-----|--------|----------|-----|--------|----------|-----|--------|----------|-----|--------|----------|
| 7 | fixed | Enable (1) or disable (0) emulation mode | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | fxmode | FSK (1) or ASK (0) | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5:4 | fxpwr[1:0] | Output power setting <table border="1"> <thead> <tr> <th>fxpwr[1:0]</th> <th>dB below P_{MAX}</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>0</td> </tr> <tr> <td>01</td> <td>3</td> </tr> <tr> <td>10</td> <td>6</td> </tr> <tr> <td>11</td> <td>10</td> </tr> </tbody> </table> | fxpwr[1:0] | dB below P _{MAX} | 00 | 0 | 01 | 3 | 10 | 6 | 11 | 10 | | | | | | | | | | | | | | | | | |
| fxpwr[1:0] | dB below P _{MAX} | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 11 | 10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | fxhdev | 100kHz (1) or 32kHz (0) frequency deviation in FSK | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2:0 | fxfrq[2:0] | Frequency selection The combinations are same as those in manual mode. When a 16MHz crystal is used, the following frequency values are selected by fxfrq[2:0]. <table border="1"> <thead> <tr> <th>fxfrq[2:0]</th> <th>Freq (MHz)</th> <th>Divide Ratio</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>N/A</td> <td>N/A</td> </tr> <tr> <td>001</td> <td>315.00</td> <td>19.68750</td> </tr> <tr> <td>010</td> <td>433.62</td> <td>27.10125</td> </tr> <tr> <td>011</td> <td>390.00</td> <td>24.37500</td> </tr> <tr> <td>100</td> <td>418.00</td> <td>26.12500</td> </tr> <tr> <td>101</td> <td>372.00</td> <td>23.25000</td> </tr> <tr> <td>110</td> <td>345.00</td> <td>21.56250</td> </tr> <tr> <td>111</td> <td>433.92</td> <td>27.12000</td> </tr> </tbody> </table> | fxfrq[2:0] | Freq (MHz) | Divide Ratio | 000 | N/A | N/A | 001 | 315.00 | 19.68750 | 010 | 433.62 | 27.10125 | 011 | 390.00 | 24.37500 | 100 | 418.00 | 26.12500 | 101 | 372.00 | 23.25000 | 110 | 345.00 | 21.56250 | 111 | 433.92 | 27.12000 |
| fxfrq[2:0] | Freq (MHz) | Divide Ratio | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 000 | N/A | N/A | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 001 | 315.00 | 19.68750 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010 | 433.62 | 27.10125 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 011 | 390.00 | 24.37500 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 100 | 418.00 | 26.12500 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 101 | 372.00 | 23.25000 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 110 | 345.00 | 21.56250 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 111 | 433.92 | 27.12000 | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Table 8. IO Configuration 0 (IOConf0) Register (Address: 0x04)

| BIT | NAME | FUNCTION |
|-----|-----------|---------------------------------------|
| 2:0 | tmux[2:0] | Status register output selection bits |

MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

Table 9. IO Configuration 1 (IOConf1) Register (Address: 0x05)

| BIT | NAME | FUNCTION |
|--|-----------|---|
| 6:4 | gp2s[2:0] | GPO2 output selection |
| | | CS_DEV Bit 2 Bit 1 Bit 0 GPO2_MOD |
| | | 0 X X X SPI Data Output |
| | | 1 0 0 0 lockdet |
| | | 1 0 0 1 — |
| | | 1 0 1 0 ckout |
| | | 1 0 1 1 — |
| | | 1 1 0 0 — |
| 2:0 | gp1s[2:0] | GPO1 output selection |
| | | Bit 2 Bit 1 Bit 0 GPO1 |
| | | 0 0 0 lockdet |
| | | 0 0 1 — |
| | | 0 1 0 ckout |
| | | 0 1 1 — |
| | | 1 0 0 — |
| | | 1 0 1 nock |
| 1 1 0 — | | |
| 1 1 1 — | | |

where:

- Reserved signals
- nock No-clock flag (1) if crystal oscillator is disabled, and (0) if clock activity is observed
- ckout Clock output signal, according to programmed dividers (ckdiv[2:0])
- lockdet PLL lock-detect flag

Table 10. ASK Digital Shaping Time Step (Tstep) Register (Address: 0x06)

| BIT | NAME | FUNCTION |
|-----|------------|---|
| 3:0 | tstep[3:0] | Time interval value used in digital shaping, in increments of 4/fXTAL |

Table 11. PA Digital Shaping Amplitude Step (PAstep) Register (Address: 0x07)

| BIT | NAME | FUNCTION |
|-----|------------|---|
| 4:0 | pastp[4:0] | Power step in digital shaping, in increments of 1dB |

Table 12. PA Power (PAPwr) Register (Address: 0x08)

| BIT | NAME | FUNCTION |
|-----|------------|-------------------------------|
| 4:0 | papwr[4:0] | Final PA output power setting |

Table 13. FSK High-Frequency 0 (FHigh0) Register (Address: 0x09)

| BIT | NAME | FUNCTION |
|-----|-----------|--|
| 7:0 | fhi[15:8] | 8-bit upper byte of high-frequency divider for FSK |

MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

Table 14. FSK High-Frequency 1 (FHigh1) Register (Address: 0x0A)

| BIT | NAME | FUNCTION |
|-----|----------|--|
| 7:0 | fhi[7:0] | 8-bit lower byte of high-frequency divider for FSK |

The 4 MSBs of FHigh0, fhi[15:12], are the integer portion of the divider, excluding offset of 16. The 12 LSBs (fhi[11:0]) are the fractional part of the divider.

Table 15. ASK Center-Frequency 0 (FCenter0) Register (Address: 0x0B)

| BIT | NAME | FUNCTION |
|-----|-----------|---|
| 7:0 | fce[15:8] | 8-bit upper byte of frequency divider for ASK |

Table 16. ASK Center-Frequency 1 (FCenter1) Register (Address: 0x0C)

| BIT | NAME | FUNCTION |
|-----|----------|---|
| 7:0 | fce[7:0] | 8-bit lower byte of frequency divider for ASK |

The 4 MSBs of FCenter0, fce[15:12], are the integer portion of the divider, excluding offset of 16. The 12 LSBs (fce[11:0]) are the fractional part of the divider.

When fce[11:0] are all zeros and ASK mode is selected (mode bit = 0), the PLL works in the fixed-N mode, which reduces current consumption and reference spurs. Set pllhw bit high (Conf0 register, bit 5). For all other combinations, the PLL works in fractional-N mode.

Table 17. FSK Low-Frequency 0 (FLo0) Register (Address: 0x0D)

| BIT | NAME | FUNCTION |
|-----|-----------|---|
| 7:0 | flo[15:8] | 8-bit upper byte of low-frequency divider for FSK |

Table 18. FSK Low-Frequency 1 (FLo1) Register (Address: 0x0E)

| BIT | NAME | FUNCTION |
|-----|----------|---|
| 7:0 | flo[7:0] | 8-bit lower byte of low-frequency divider for FSK |

The 4 MSBs of FLo0, flo[15:12], are the integer portion of the divider, excluding offset of 16. The 12 LSBs (flo[11:0]) are the fractional part of the divider.

Table 19. Maximum and Minimum Values for Frequency Divider

| DECIMAL VALUE | fhi[15:0], fce[15:0], flo[15:0] |
|---------------|---------------------------------|
| 12.0220 | 0xC05A |
| 2.9536 | 0x2F42 |

Table 20. Frequency-Load (FLoad) Register (Address: 0x0F)

| BIT | NAME | FUNCTION |
|-----|------|--|
| 0 | hop | Effectively changes the PLL frequency to the ones written in registers 0x09 to 0x0E. This is a self-reset bit and is reset to zero after the operation is completed. |

MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

Table 21. Enable (EnableReg) Register (Address: 0x10)

| BIT | NAME | FUNCTION |
|-----|--------|---|
| 0 | enable | SPI equivalent of the ENABLE pin, which should be kept low (0) if the external ENABLE pin is used. The external ENABLE pin should also be kept low (0) if the enable bit is used. |

Table 22. Data Input (DataReg) Register (Address: 0x11)

| BIT | NAME | FUNCTION |
|-----|--------|--|
| 0 | datain | SPI equivalent of DIN, where the transmitted data can be controlled through the SPI interface. It should be kept low (0) if only the external DIN pin is used. The external DIN pin should also be kept low (0) if the datain bit is used. |

Table 23. Status (Status) Register (Address: 0x12)

| BIT | NAME | FUNCTION |
|-----|-------------|---|
| 7:0 | status[7:0] | Read-only status register, selected through tmux[2:0] (register 0x04 IOConf0) |

Table 24. Status Bus Signals

| tmux[2:0] | status[7] | status[6] | status[5] | status[4] | status[3] | status[2] | status[1] | status[0] |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 0 | — | — | — | — | ckout | ckd16 | ckd4 | nock |
| 1 | — | — | — | — | — | — | — | — |
| 2 | — | — | — | — | enable | — | — | — |
| 3 | — | frac_fxdb | — | cap[4] | cap[3] | cap[2] | cap[1] | cap[0] |
| 4 | — | — | notover | capfxd[4] | capfxd[3] | capfxd[2] | capfxd[1] | capfxd[0] |
| 5 | integ[3] | integ[2] | integ[1] | integ[0] | frac[11] | frac[10] | frac[9] | frac[8] |
| 6 | frac[7] | frac[6] | frac[5] | frac[4] | frac[3] | frac[2] | frac[1] | frac[0] |
| 7 | — | — | — | — | — | — | lockdet | xmit_en |

| | | | |
|----------|--|-------------|--|
| — | Reserved signals | frac_fxdb | Fractional-N mode (1) or ASK fixed-N mode (0) |
| nock | No-clock flag (1) if crystal oscillator is disabled, and (0) if clock activity is observed | capfxd[4:0] | Emulation mode variable capacitor setting |
| ckd4 | Crystal clock signal divided by 4 | notover | ASK digital shaping flag (1) when PA power value is different than 0 |
| ckd16 | Crystal clock signal divided by 16 | integ[3:0] | Fractional-N 4-bit integer value |
| ckout | Clock output signal, according to programmed dividers (ckdiv[2:0]) | frac[11:0] | Fractional-N 12-bit fractional value |
| enable | Internal enable signal (OR function of the ENABLE pin and enable bit) | xmit_en | Transmitter PA enable flag |
| cap[4:0] | SPI mode capacitor setting | lockdet | PLL lock-detect flag |

MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

Manual Mode Settings

The MAX7060 can be operated by controlling certain pins directly, thereby eliminating the need for an SPI controller. There is a restricted selection of frequency and power settings, but operation is simpler. The pins that are used in manual mode are as follows:

Pin 1: GPO2_MOD (modulation mode, 0 = ASK, 1 = FSK)

Pins 5, 6, 7: FREQ0, FREQ1, FREQ2

Pin 19: $\overline{CS_DEV}$ (FSK deviation selection, 0 = ± 16 kHz, 1 = ± 50 kHz)

Pins 20, 21: SDI_PWR1 and SCLK_PWR0 (2-pin power selection)

Pins 22, 23: ENABLE and DIN (PA variable capacitor setting, data input, enable)

To put the MAX7060 in manual mode, set any of the FREQ0, FREQ1, FREQ2 pins (5, 6, and 7) to logic-high. These pins are normally pulled down, so the default state of the MAX7060 is for SPI operation. The settings in Table 25 can be made in manual mode.

Frequency Selection

There are seven internally set fractional-N divide ratios that correspond to commonly used frequencies when a 16MHz crystal is used.

Notice that the MAX7060 can be operated manually at any single frequency over its 280MHz to 450MHz operating range by choosing a crystal frequency and one of the divide ratios from Table 25. For example, a transmitting frequency of 308MHz can be achieved by selecting the 19.68750 divide ratio and a 15.6444MHz crystal.

The frequency settings in the manual mode of operation were designed in a way that allows the customer to toggle only one control line between low and high states to switch between seven commonly used frequency pairs (see Table 26).

ASK or FSK Modulation

Reset pin 1 (GPO2_MOD) to 0 for ASK modulation and 1 for FSK modulation. Analog shaping in ASK mode is enabled by using the ROUT pin. The turn-on and turn-off time is fixed at approximately 1 μ s.

Table 25. Manual Mode Frequency Selection

| FREQ2 | FREQ1 | FREQ0 | FREQUENCY (MHz) | DIVIDE RATIO |
|-------|-------|-------|-----------------|--------------|
| 0 | 0 | 0 | SPI | N/A |
| 0 | 0 | 1 | 315.00 | 19.68750 |
| 0 | 1 | 0 | 433.62 | 27.10125 |
| 0 | 1 | 1 | 390.00 | 24.37500 |
| 1 | 0 | 0 | 418.00 | 26.12500 |
| 1 | 0 | 1 | 372.00 | 23.25000 |
| 1 | 1 | 0 | 345.00 | 21.56250 |
| 1 | 1 | 1 | 433.92 | 27.12000 |

Table 26. Manual Mode Frequency Pair Switching

| LOW FREQUENCY (MHz) | HIGH FREQUENCY (MHz) | FREQ2, FREQ1, FREQ0 |
|---------------------|----------------------|--|
| 315.00 | 433.92 | 001 to 111. Set FREQ0 high, shorting FREQ1 and FREQ2, toggling 1 line. |
| 418.00 | 433.92 | 100 to 111. Set FREQ2 high, shorting FREQ1 and FREQ0, toggling 1 line. |
| 433.62 | 433.92 | 010 to 111. Set FREQ1 high, shorting FREQ2 and FREQ0, toggling 1 line. |
| 315.00 | 390.00 | 001 to 011. Set FREQ0 high and FREQ2 low, toggling FREQ1. |
| 315.00 | 372.00 | 001 to 101. Set FREQ1 low and FREQ0 high, toggling pin FREQ2. |
| 345.00 | 433.92 | 110 to 111. Set FREQ2 and FREQ1 high, toggling FREQ0. |
| 390.00 | 433.92 | 011 to 111. Set FREQ1 and FREQ0 high, toggling FREQ2. |

MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

Table 27. Output Power Settings

| SDI_PWR1 | SCLK_PWR0 | dB BELOW P _{MAX} |
|----------|-----------|---------------------------|
| 0 | 0 | 0 |
| 0 | 1 | 3 |
| 1 | 0 | 6 |
| 1 | 1 | 10 |

Frequency Deviation

Reset pin 19 ($\overline{CS_DEV}$) to 0 for 32kHz (± 16 kHz) FSK deviation and 1 for 100kHz (± 50 kHz) FSK deviation.

Transmitter Power

Set SDI_PWR1 (pin 20) and SCLK_PWR0 (pin 21) to four power settings (relative to the maximum power setting).

Note that at battery voltages below 3V, the top two power settings are compressed and the power difference is less than 3dB.

PA Variable Capacitor Setting

In manual mode, capacitance can be added to the PA output for one selected frequency. This allows the user to adjust the matching network when switching between two frequencies in the manual selection table, or for switching to one frequency that is significantly different from the others in the table. The user can set the capacitance by resetting the ENABLE pin to a logic-low, then selecting the frequency for which the variable capacitor is to be added from the seven possible settings, and then sending a stream of 1 to 32 pulses through the DIN pin. The first pulse is used to reset the internal capacitor counter and to latch the selected frequency. After the first pulse, the remaining number of pulses sent equals the variable capacitor setting. When the ENABLE pin goes high, the capacitor setting for the specified frequency is set, so that it adds the programmed capacitance to the PA when the chosen frequency is selected. This scheme must be executed only once to set the value of the variable capacitor.

For example, a user can operate the MAX7060 at 315MHz and 433.92MHz into a narrowband antenna by resetting the ENABLE pin low, setting the FREQ0, FREQ1, FREQ2 pins to 001 (315MHz), and sending the appropriate number of pulses into the DIN pin, and then setting the ENABLE pin high. When the frequency is set to 433.92MHz (or any other frequency in the table except 315MHz), no capacitance is added to the PA output.

When the frequency is set to 315MHz, the PA capacitance increases by the programmed value.

Figure 8 illustrates how to set the capacitance. It begins with the ENABLE pin pulled low. The frequency is sampled at the rising edge of the first pulse. Pulses 2–11 set the capacitance code to 0x0A (10dec), which is approximately 2.5pF. The ENABLE pin is then pulled high to finish the setting.

Emulation Mode Settings

All the settings available through the manual mode of operation are also easily accessible in the SPI mode. This mode is called emulation mode, whereby only writing one or two registers, the whole transmitter can be configured. The Conf2 register controls this mode.

The emulation mode is a subset of SPI mode. It gives SPI users the capability to operate the part by programming just one or two registers instead of all registers.

Since it is still SPI mode, pins 5, 6, and 7 (FREQ0, FREQ1, and FREQ2) must be pulled low. The Conf2 register is the only register that needs to be programmed. Setting bit 7 (fixed) to 1 enables this mode. Bit 6 (fxmode) is equivalent to pin 1 (GPO2_MOD) in manual mode. Bits 5 and 4 (fxpwr[1:0]) are equivalent to pin 20 and 21 (SDI_PWR1 and SCLK_PWR0) in manual mode. Bit 3 (fxhdev) is equivalent to pin 19 ($\overline{CS_DEV}$) in manual mode. Bits 2, 1, and 0 (fxfrq[2:0]) are equivalent to pins 5, 6, and 7 (FREQ0, FREQ1, and FREQ2) in manual mode.

Similar to manual mode, the PA capacitor setting in the emulation mode can be done by toggling the DIN pin with the ENABLE pin low. In addition, the capacitor setting can also be done by directly writing to the capacitor register (bits 4:0 of the Conf1 register, cap[4:0]). As long as the capacitor register value is not zero, the capacitor value sent in by toggling the DIN pin is ignored.

Control Interface Considerations

When operating the MAX7060 with a +4.5V to +5.5V supply voltage, the $\overline{CS_DEV}$, SCLK_PWR0, SDI_PWR1, FREQ0, FREQ1, FREQ2, ENABLE, DIN, and LSHDN pins can be driven by a microcontroller with either 3V or 5V interface logic levels. When operating the MAX7060 with a +2.1V to +3.6V supply, the microcontroller must produce logic levels that conform to the V_{IH} and V_{IL} specifications in the *DC Electrical Characteristics* for the MAX7060.

MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

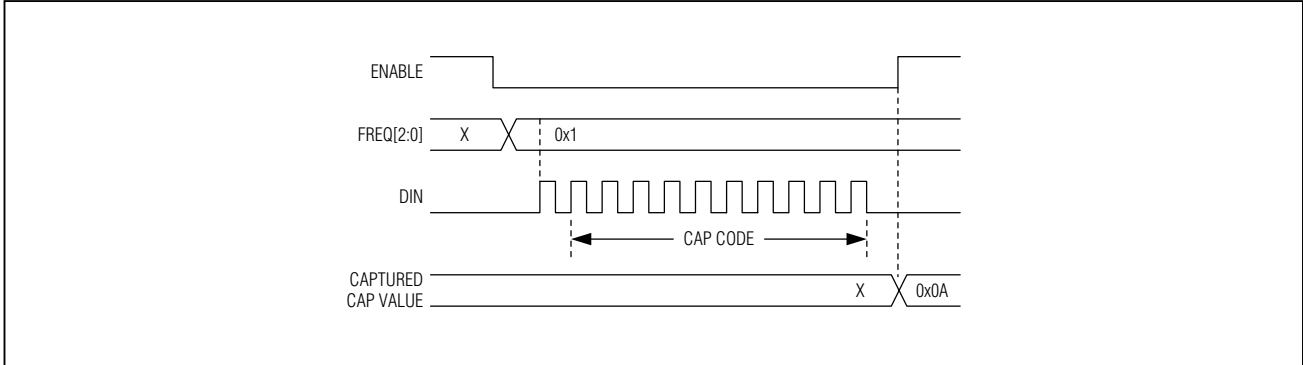
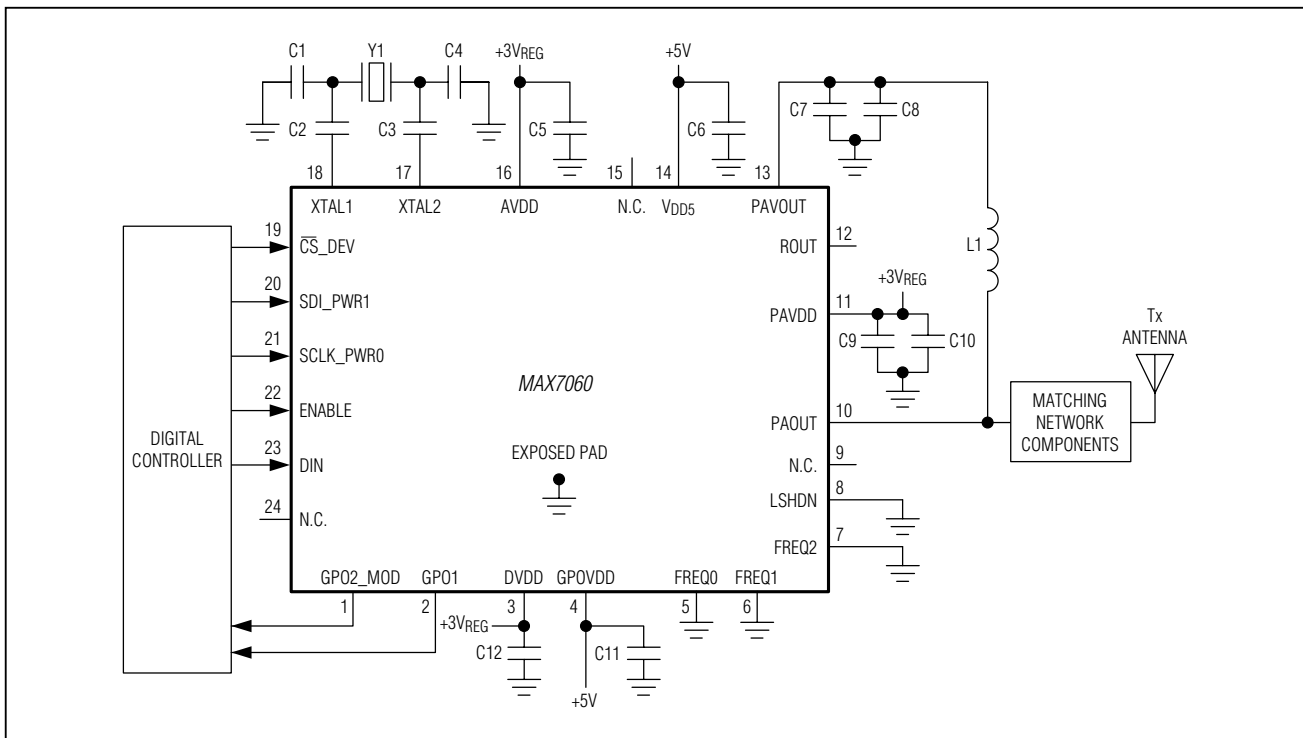


Figure 8. Variable Capacitor Setting Timing Diagram

Typical Application Circuits

SPI Mode (5V Supply)

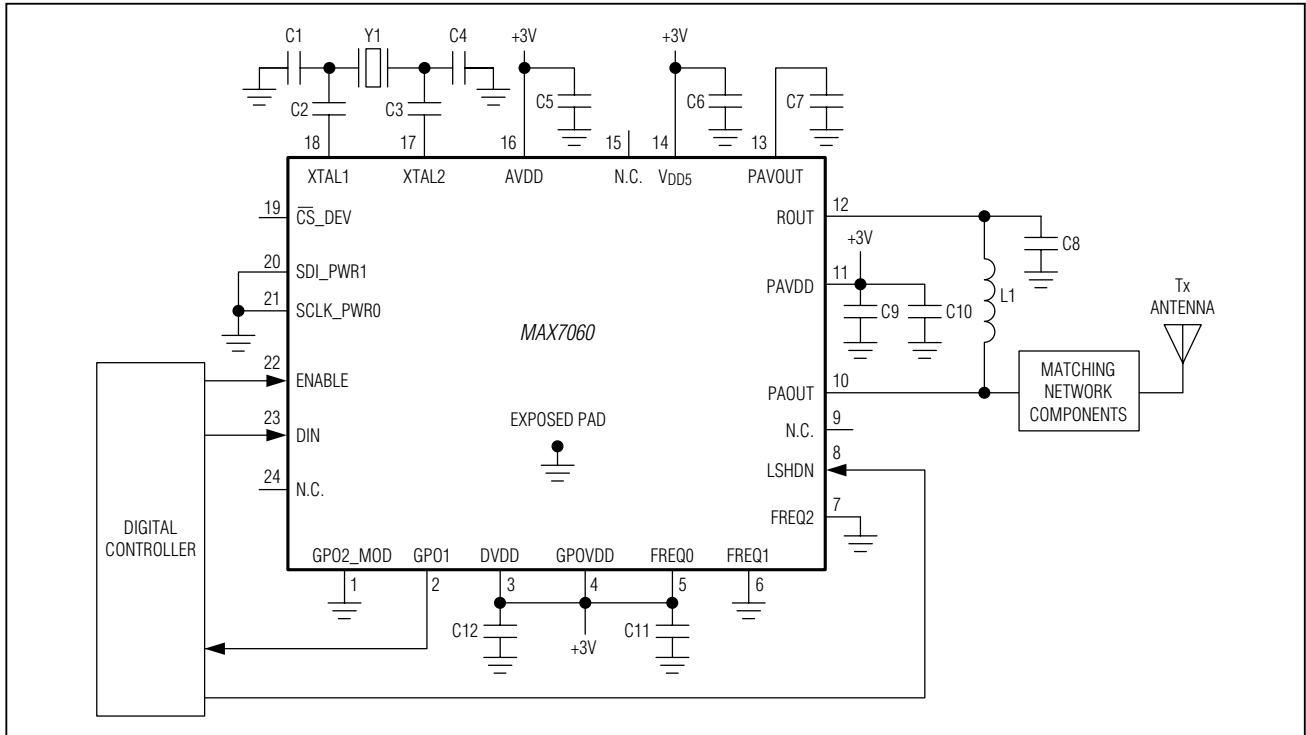


MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

Typical Application Circuits (continued)

Manual Mode (3V Supply, Shaped ASK Modulation, 315MHz)



Component List

| DESIGNATION | QTY | DESCRIPTION |
|-----------------------------|-----|---|
| C1, C4 | 2 | May not be needed for low C _{LOAD} crystals, depending on PCB layout parasitics |
| C2, C3 | 2 | 1.5nF ±10%, 50V X7R ceramic capacitors (0603) Murata GRM188R71H152K |
| C5, C6 | 2 | 100nF ±10%, 50V X7R ceramic capacitors (0603) Murata GRM188R71H104K |
| C7, C8, C9 | 3 | 220pF ±5% ceramic capacitors (0603) Murata GRM1885C1H220JA01D |
| C10, C11, C12 | 3 | 10nF ±10%, 50V X7R ceramic capacitors (0603) Murata GRM188R71H103K |
| L1 | 1 | ±5% wire-wound inductor (0603) Murata LQW18 series (value depends on matching network) |
| Matching Network Components | 4 | 3 capacitors and 1 inductor (values depend on frequency range and antenna impedance) |
| U1 | 1 | Maxim MAX7060ATG+ |
| Y1 | 1 | 16MHz crystal, 10pF C _{LOAD} Crystek 17466 Suntsu SCX284 |

MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|--------------|--------------|-------------------------|-------------------------|
| 24 TQFN-EP | T2444+3 | 21-0139 | 90-0021 |

MAX7060

280MHz to 450MHz Programmable ASK/FSK Transmitter

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|--|-------------------------------|
| 0 | 2/10 | Initial release | — |
| 1 | 2/12 | Power dissipation and derating factor shown for wrong package type; clarified GPO1 boost mode and nature of analog and digital ASK envelope shaping. Added paragraph on control interface considerations; updated <i>Typical Application Circuits</i> to add exposed pad (grounded); and specified typical load C on crystal in component list | 2, 14, 15, 19, 21, 27, 28, 29 |



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31