

4V Drive Nch + Pch MOSFET

SP8M51

● Structure

Silicon N-channel MOSFET/
Silicon P-channel MOSFET

● Features

- 1) Low on-resistance.
- 2) Built-in G-S Protection Diode.
- 3) Small Surface Mount Package (SOP8).

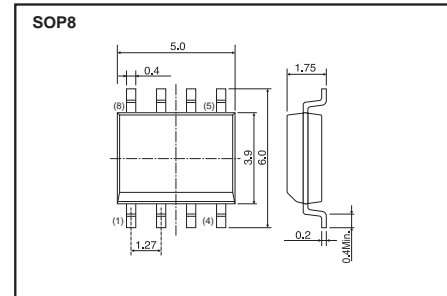
● Application

Switching

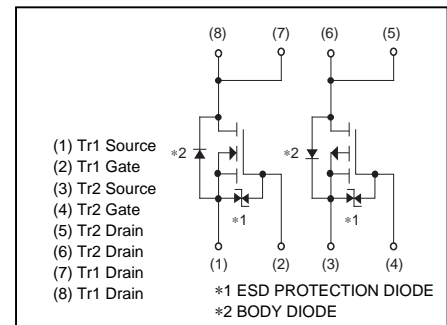
● Packaging specifications

Type	Package	Taping
	Code	TB
	Basic ordering unit (pieces)	2500
SP8M51		○

● Dimensions (Unit : mm)



● Inner circuit



● Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits		Unit
		Tr1 : N-ch	Tr2 : P-ch	
Drain-source voltage	V_{DSS}	100	-100	V
Gate-source voltage	V_{GSS}	±20	±20	V
Drain current	Continuous	I_D	±3.0	A
	Pulsed	I_{DP} *1	±12	A
Source current (Body Diode)	Continuous	I_s	1.0	A
	Pulsed	I_{sp} *1	12	A
Total power dissipation	P_D *2	2.0		W / TOTAL
		1.4		W / ELEMENT
Channel temperature	T_{ch}	150		°C
Range of storage temperature	T_{stg}	-55 to +150		°C

*1 $P_w \leq 10 \mu s$, Duty cycle $\leq 1\%$

*2 Mounted on a ceramic board.

● **Electrical characteristics** (Ta = 25°C)

<Tr1(Nch)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	±10	μA	$V_{GS}=\pm 20V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$I_D=1mA, V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=100V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	1.0	-	2.5	V	$V_{DS}=10V, I_D=1mA$
Static drain-source on-state resistance	$R_{DS(on)}^*$	-	120	170	mΩ	$I_D=3.0A, V_{GS}=10V$
		-	130	180		$I_D=3.0A, V_{GS}=4.5V$
		-	135	190		$I_D=3.0A, V_{GS}=4.0V$
Forward transfer admittance	$ Y_{fs} ^*$	3.5	-	-	S	$V_{DS}=10V, I_D=3.0A$
Input capacitance	C_{iss}	-	610	-	pF	$V_{DS}=25V$
Output capacitance	C_{oss}	-	55	-	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	-	35	-	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}^*$	-	13	-	ns	$I_D=1.5A, V_{DD}=50V$
Rise time	t_r^*	-	13	-	ns	$V_{GS}=10V$
Turn-off delay time	$t_{d(off)}^*$	-	50	-	ns	$R_L=33\Omega$
Fall time	t_f^*	-	14	-	ns	$R_G=10\Omega$
Total gate charge	Q_g^*	-	8.5	-	nC	$I_D=3.0A$
Gate-source charge	Q_{gs}^*	-	1.8	-	nC	$V_{DD}=50V$
Gate-drain charge	Q_{gd}^*	-	3.5	-	nC	$V_{GS}=5V$

*Pulsed

● **Body diode characteristics** (Source-Drain) (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD}^*	-	-	1.2	V	$I_s=3.0A, V_{GS}=0V$

*Pulsed

● **Electrical characteristics** (Ta = 25°C)

<Tr2(Pch)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	±10	μA	$V_{GS}=\pm 20V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	-100	-	-	V	$I_D=-1mA, V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}		-	-1	μA	$V_{DS}=-100V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	-1.0	-	-2.5	V	$V_{DS}=-10V, I_D=-1mA$
Static drain-source on-state resistance	$R_{DS(on)}^*$	-	210	290	mΩ	$I_D=-2.5A, V_{GS}=-10V$
		-	230	320		$I_D=-1.25A, V_{GS}=-4.5V$
		-	240	340		$I_D=-1.25A, V_{GS}=-4.0V$
Forward transfer admittance	$ Y_{fs} ^*$	3.5	-	-	S	$I_D=-2.5A, V_{DS}=-10V$
Input capacitance	C_{iss}	-	1550	-	pF	$V_{DS}=-25V$
Output capacitance	C_{oss}	-	65	-	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	-	40	-	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}^*$	-	15	-	ns	$I_D=-1.25A, V_{DD}=-50V$
Rise time	t_r^*	-	13	-	ns	$V_{GS}=-10V$
Turn-off delay time	$t_{d(off)}^*$	-	75	-	ns	$R_L=50\Omega$
Fall time	t_f^*	-	19	-	ns	$R_G=10\Omega$
Total gate charge	Q_g^*	-	12.5		nC	$I_D=-2.5A$
Gate-source charge	Q_{gs}^*	-	3.8	-	nC	$V_{DD}=-50V$
Gate-drain charge	Q_{gd}^*	-	3.2	-	nC	$V_{GS}=-5V$

*Pulsed

● **Body diode characteristics** (Source-Drain) (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD}^*	-	-	-1.2	V	$I_s=-2.5A, V_{GS}=0V$

*Pulsed

●Electrical characteristic curves (Ta=25°C)

<TR1(Nch)>

Fig.1 Typical Output Characteristics(I)

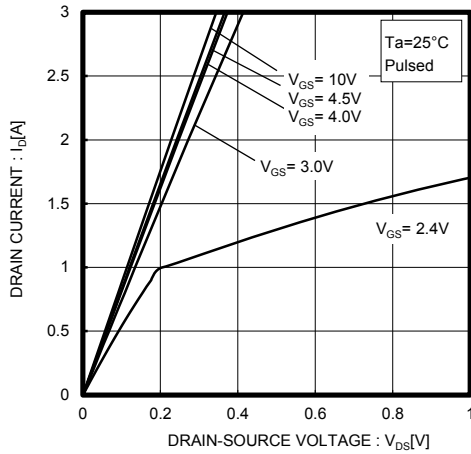


Fig.2 Typical Output Characteristics(II)

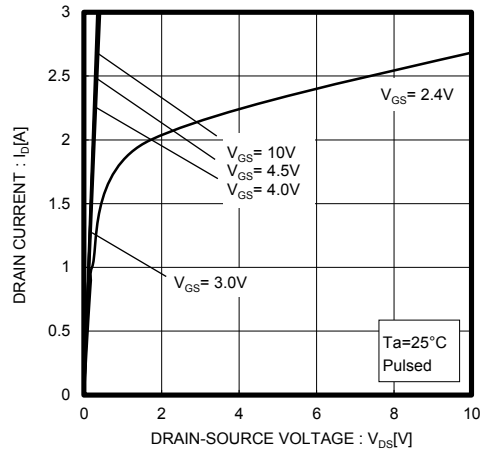


Fig.3 Typical Transfer Characteristics

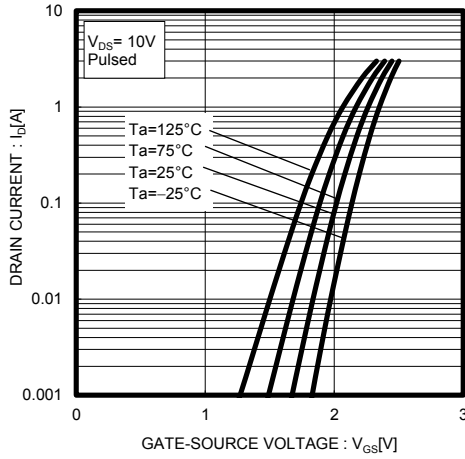


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)

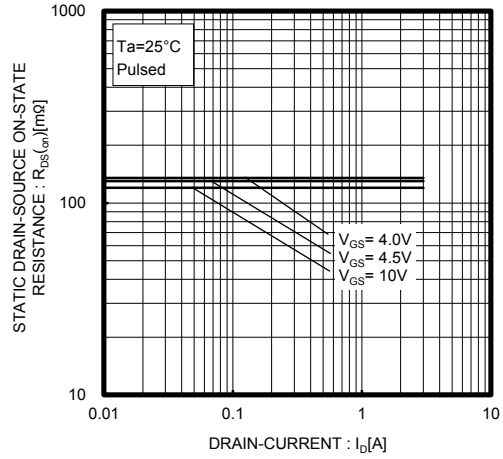


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)

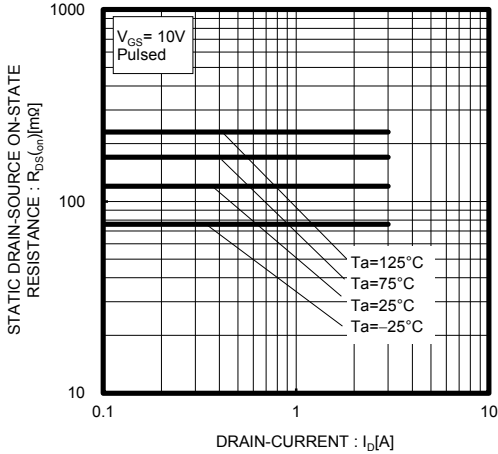


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(III)

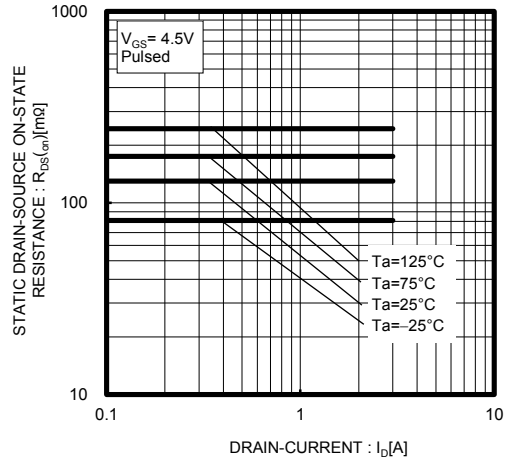


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)

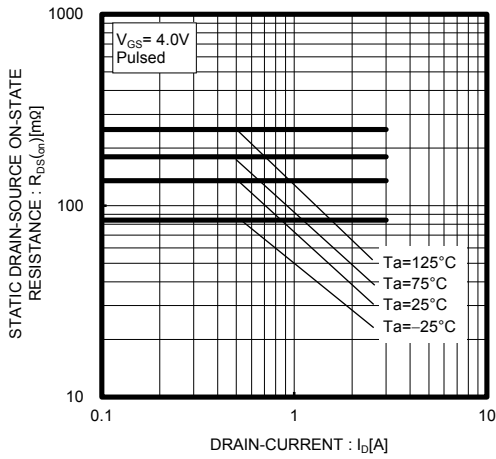


Fig.8 Forward Transfer Admittance vs. Drain Current

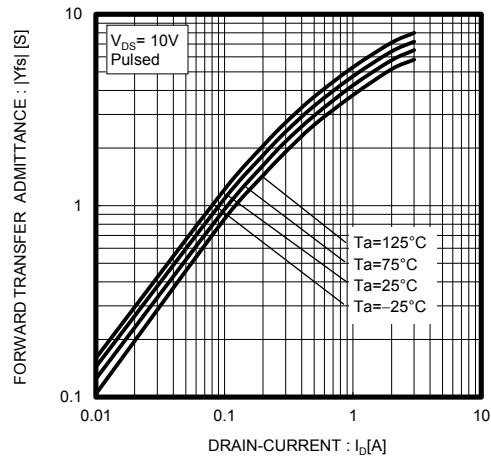


Fig.9 Reverse Drain Current vs. Source-Drain Voltage

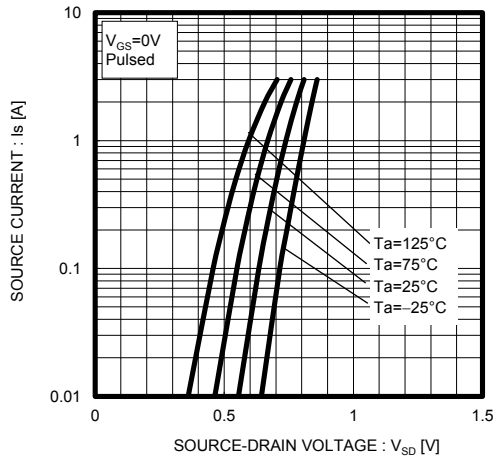


Fig.10 Static Drain-Source On-State Resistance vs. Gate Source Voltage

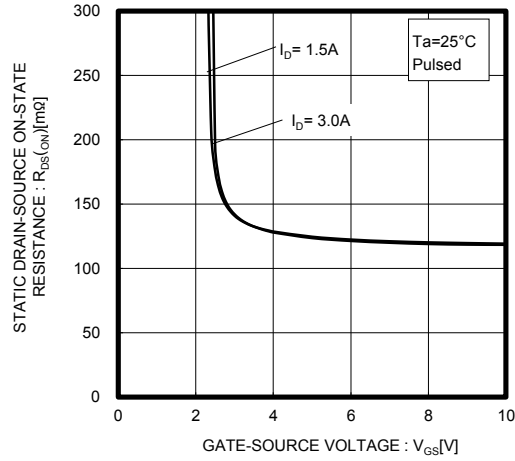


Fig.11 Switching Characteristics

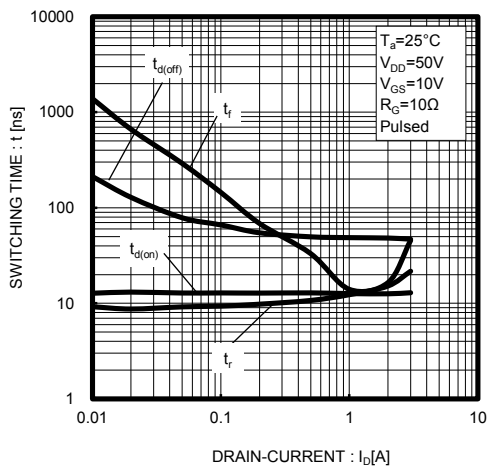


Fig.12 Dynamic Input Characteristics

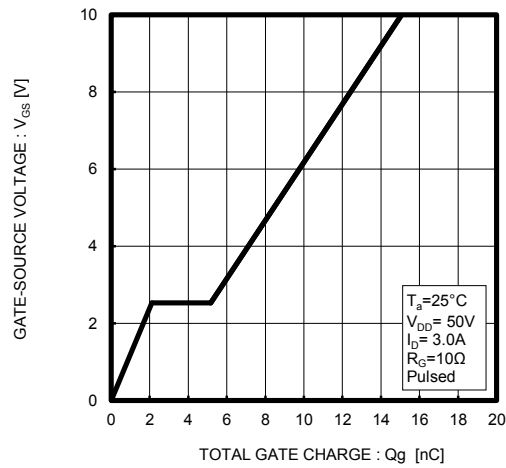


Fig.13 Typical Capacitance vs. Drain-Source Voltage

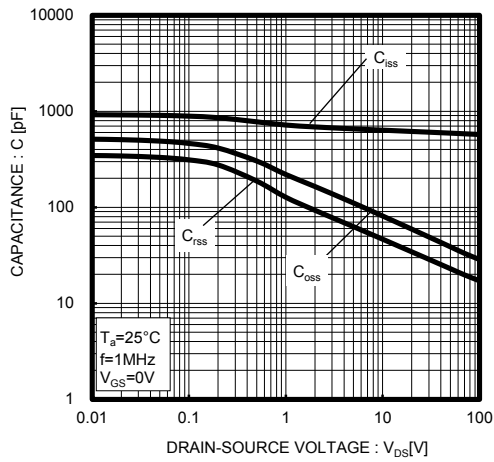


Fig.14 Maximum Safe Operating Area

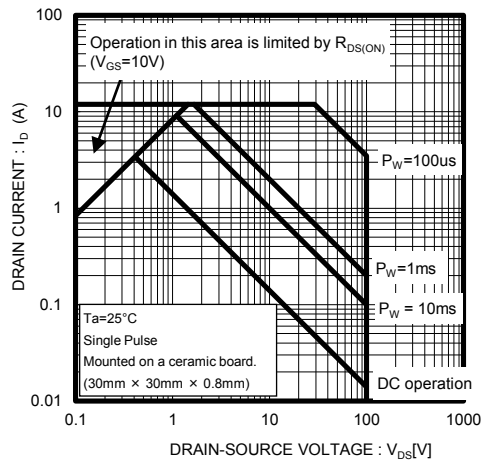
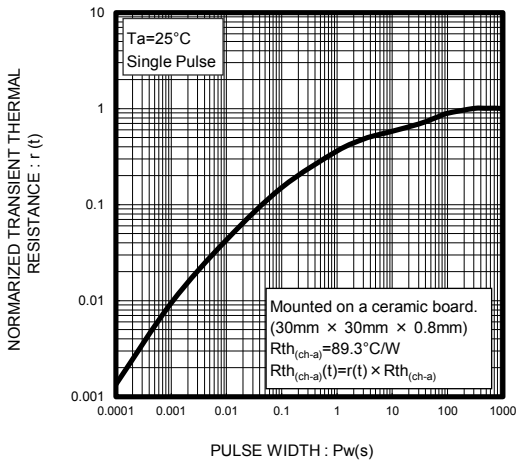


Fig.15 Normalized Transient Thermal Resistance vs. Pulse Width



<TR2(Pch)>

Fig.1 Typical Output Characteristics(I)

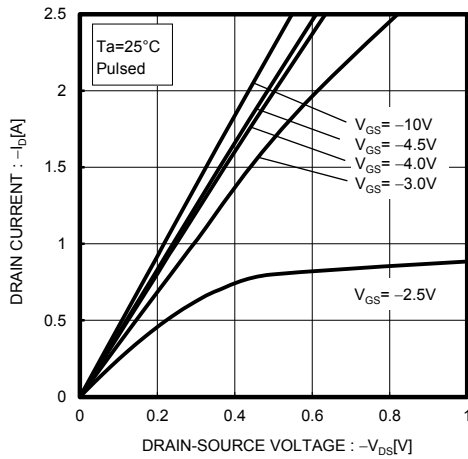


Fig.2 Typical Output Characteristics(II)

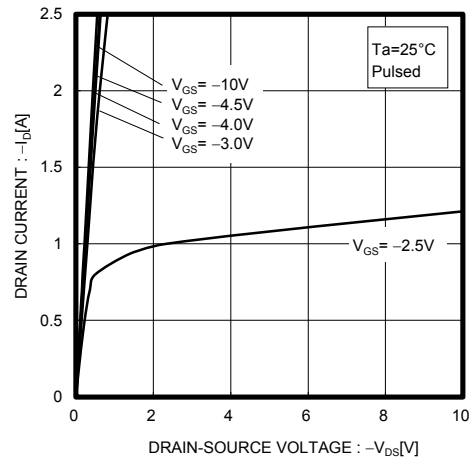


Fig.3 Typical Transfer Characteristics

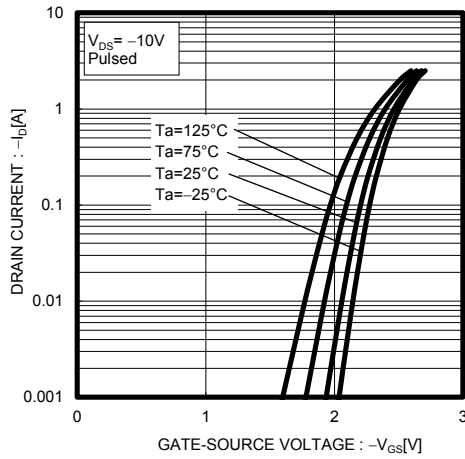


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)

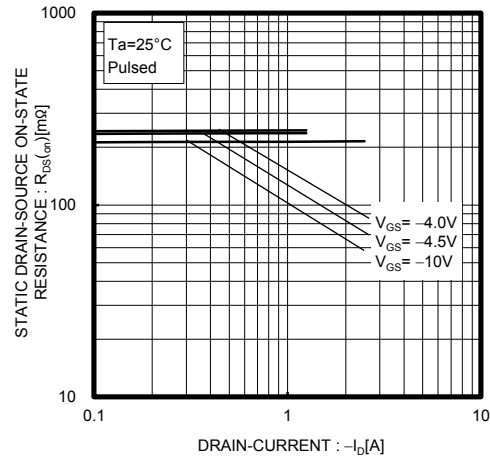


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)

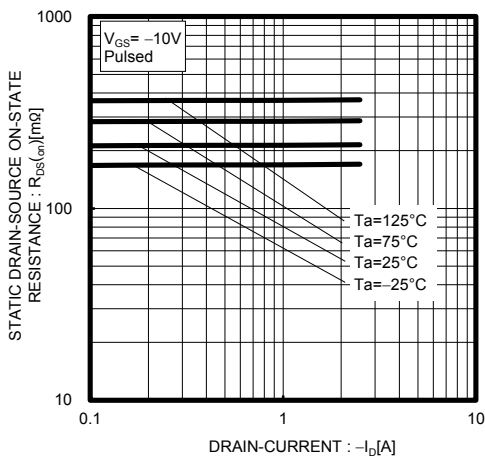


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(III)

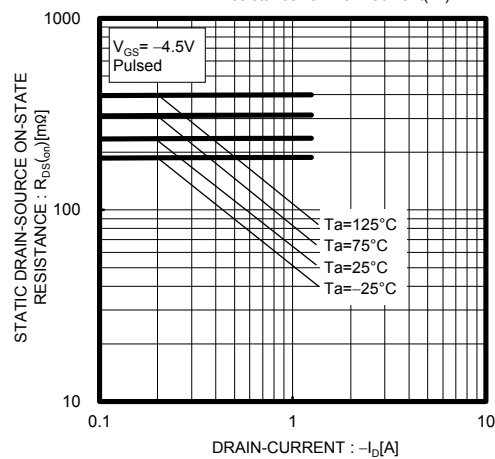


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (IV)

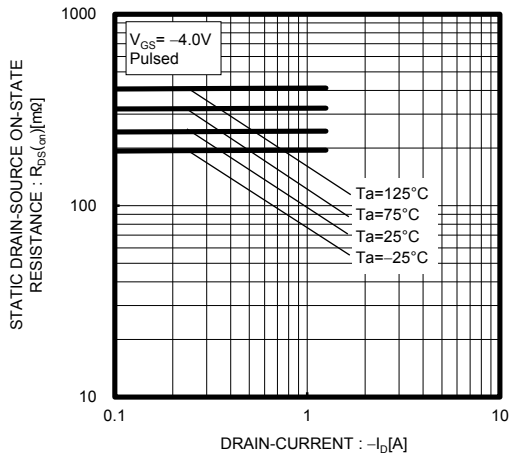


Fig.8 Forward Transfer Admittance vs. Drain Current

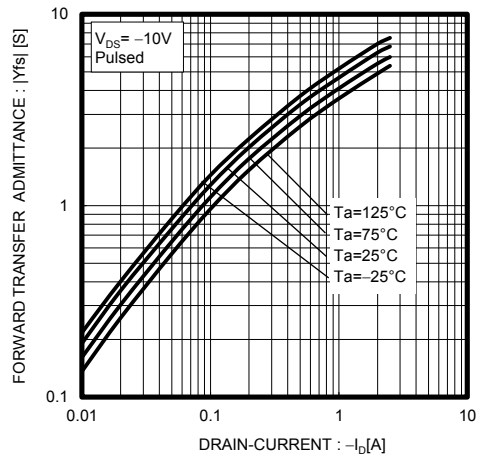


Fig.9 Reverse Drain Current vs. Source-Drain Voltage

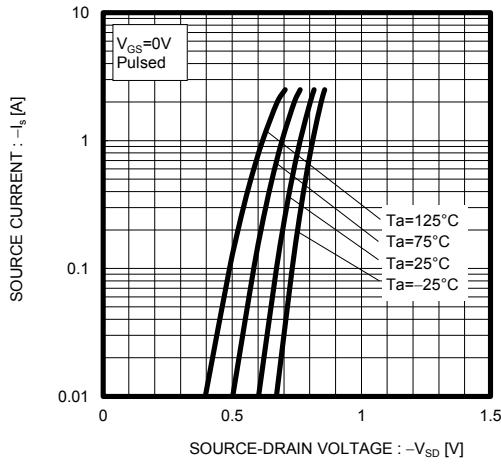


Fig.10 Static Drain-Source On-State Resistance vs. Gate Source Voltage

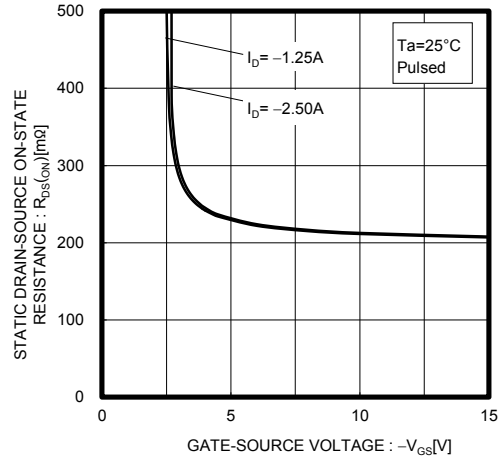


Fig.11 Switching Characteristics

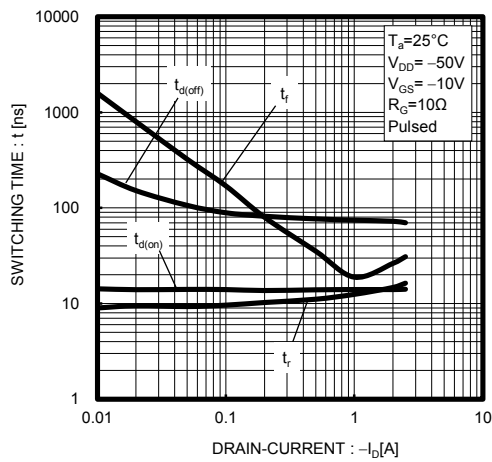


Fig.12 Dynamic Input Characteristics

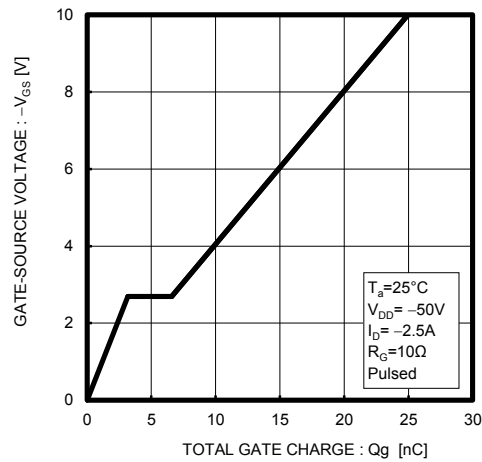


Fig.13 Typical Capacitance vs. Drain-Source Voltage

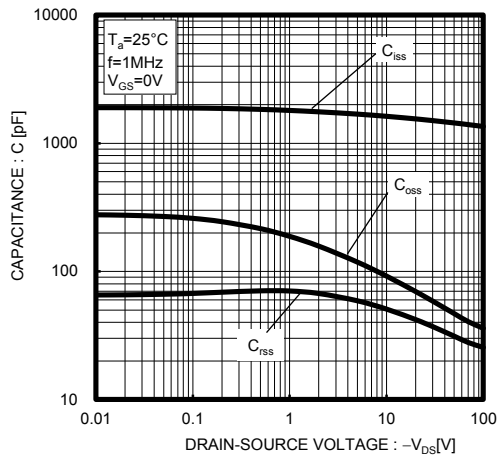


Fig.14 Maximum Safe Operating Area

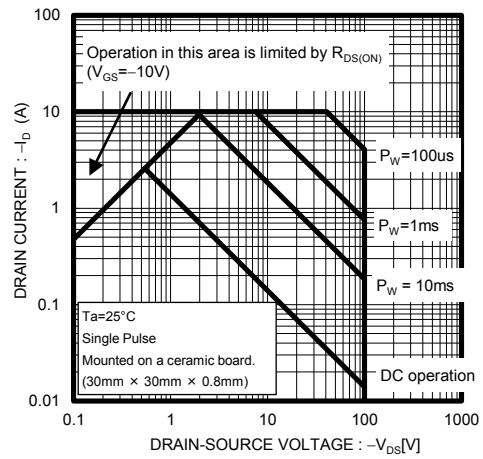
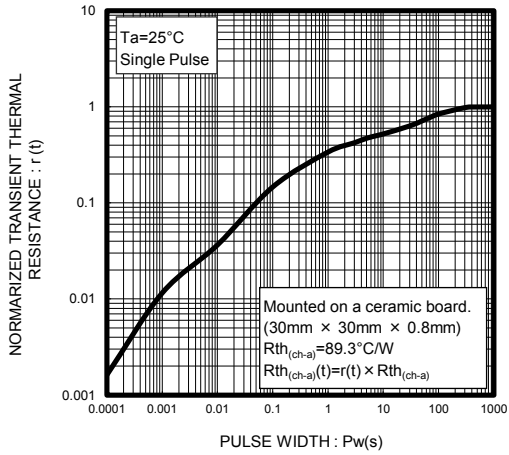


Fig.15 Normalized Transient Thermal Resistance vs. Pulse Width



● Measurement circuits

<Tr1(Nch)>

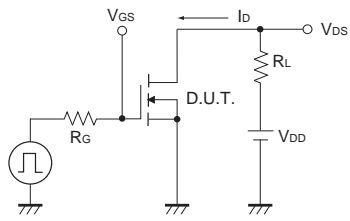


Fig.1-1 Switching Time Measurement Circuit

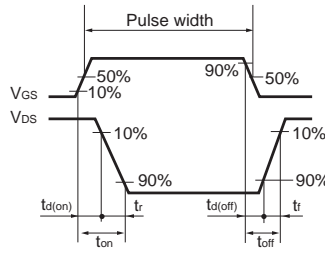


Fig.1-2 Switching Waveforms

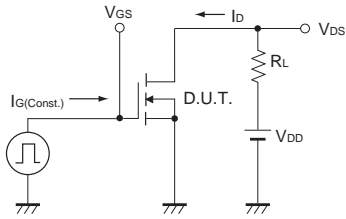


Fig.2-1 Gate Charge Measurement Circuit

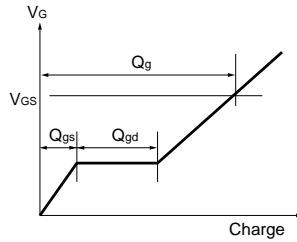


Fig.2-2 Gate Charge Waveform

<Tr2(Pch)>

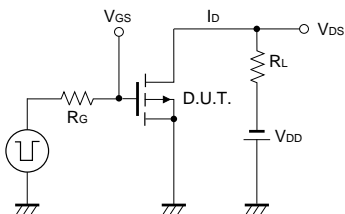


Fig.3-1 Switching Time Measurement Circuit

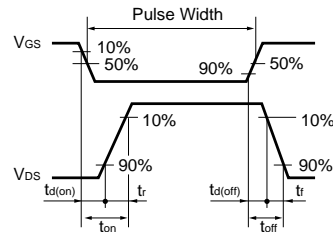


Fig.3-2 Switching Waveforms

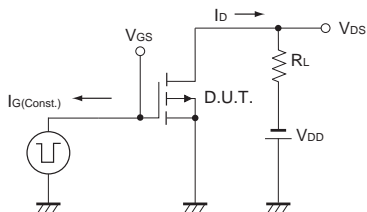


Fig.4-1 Gate Charge Measurement Circuit

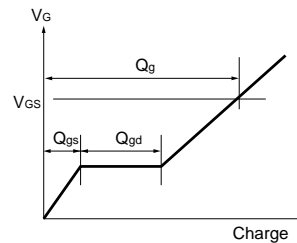


Fig.4-2 Gate Charge Waveform

Notes

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