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[ALD1726GPAL](#)

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**PRECISION ULTRA MICROPOWER CMOS OPERATIONAL AMPLIFIER**

**GENERAL DESCRIPTION**

The ALD1726/ALD1726G is a monolithic precision CMOS ultra micropower high slew-rate, high performance operational amplifier intended for a broad range of analog applications using  $\pm 1V$  to  $\pm 5V$  dual power supply systems, as well as  $+2V$  to  $+10V$  battery operated systems. All device characteristics are specified for  $+5V$  single supply or  $\pm 2.5V$  dual supply systems. Supply current is  $40\mu A$  maximum at  $5V$  supply voltage.

The ALD1726/ALD1726G is designed to offer high performance for a wide range of applications requiring very low power dissipation. It has been developed specifically for the  $+5V$  single battery or  $\pm 1V$  to  $\pm 5V$  dual battery user and offers the popular industry standard single operational amplifier pin configuration.

Several important characteristics of the device make application easier to implement at those voltages. First, the operational amplifier can operate with rail to rail input and output voltages. This means the signal input voltage and output voltage can be close to or equal to the positive and negative supply voltages. This feature allows numerous analog serial stages and flexibility in input signal bias levels. Second, the device was designed to accommodate mixed applications where digital and analog circuits may operate off the same power supply or battery. Third, the output stage can typically drive up to  $25pF$  capacitive and  $20K\Omega$  resistive loads. These features, combined with extremely low input currents, high open loop voltage gain of  $100V/mV$ , useful bandwidth of  $400KHz$ , a slew rate of  $0.17V/\mu s$ , low offset voltage and temperature drift, make the ALD1726/ALD1726G a versatile, micropower operational amplifier.

The ALD1726/ALD1726G, designed and fabricated with silicon gate CMOS technology, offers  $0.01 pA$  typical input bias current. On chip offset voltage trimming allows the device to be used without nulling in most applications.

The ALD1726/ALD1726G is also designed to offer tolerance to over-voltage input spikes of  $300mV$  beyond supply rails, high open loop voltage gain, and robust operation at temperature extremes. Additionally, robust design and rigorous screening make this device especially suitable for operation in temperature-extreme environments and rugged conditions.

**FEATURES & BENEFITS**

- Lead Free - RoHS compatible
- Robust high-temperature operation
- $20\mu A$  supply current
- All parameters specified for  $+5V$  single supply or  $\pm 2.5V$  dual supply systems
- Rail to rail input and output voltage ranges
- No frequency compensation required -- unity gain stable
- Extremely low input bias currents --  $0.1pA$  typical ( $30pA$  max.)
- Ideal for high source impedance applications
- Dual power supply  $\pm 1.0V$  to  $\pm 5.0V$  operation
- Single power supply  $+2V$  to  $+10V$  operation
- High voltage gain -- typically  $100V/mV @ \pm 2.5V$  ( $100dB$ )
- Drive as low as a  $20K\Omega$  load
- Output short circuit protected
- Unity gain bandwidth of  $0.4MHz$
- Slew rate of  $0.17V/\mu s$
- Suitable for rugged, temperature-extreme environments

**APPLICATIONS**

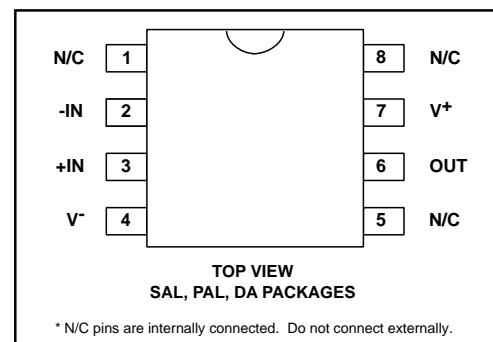
- Voltage amplifier
- Voltage follower/buffer
- Charge integrator
- Photodiode amplifier
- Data acquisition systems
- High performance portable instruments
- Biochemical probe interface
- Signal conditioning circuits
- Sensor and transducer amplifiers
- Low leakage amplifiers
- Precision Sample and Hold amplifiers
- Active filters
- Picoammeter
- Current to voltage converter

**ORDERING INFORMATION ("L" suffix denotes lead-free (RoHS))**

Operating Temperature Range		
$0^{\circ}C$ to $+70^{\circ}C$	$0^{\circ}C$ to $+70^{\circ}C$	$-55^{\circ}C$ to $+125^{\circ}C$
8-Pin Small Outline Package (SOIC)	8-Pin Plastic Dip Package	8-Pin CERDIP Package
ALD1726SAL	ALD1726PAL	ALD1726DA
ALD1726GSAL	ALD1726GPAL	ALD1726GDA

\* Contact factory for leaded (non-RoHS) or high temperature versions.

**PIN CONFIGURATION**



**ABSOLUTE MAXIMUM RATINGS**

Supply voltage, V+	_____	10.6V
Differential input voltage range	_____	-0.3V to V+ +0.3V
Power dissipation	_____	600 mW
Operating temperature range	SAL, PAL packages	0°C to +70°C
	DA package	-55°C to +125°C
Storage temperature range	_____	-65°C to +150°C
Lead temperature, 10 seconds	_____	+260°C

**CAUTION:** ESD Sensitive Device. Use static control procedures in ESD controlled environment.

**OPERATING ELECTRICAL CHARACTERISTICS**

**T<sub>A</sub> = 25°C V<sub>S</sub> = ±2.5V unless otherwise specified**

Parameter	Symbol	1726			1726G			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Supply Voltage	V <sub>S</sub>	±1.0		±5.0	±1.0		±5.0	V	Dual Supply Single Supply
	V+	2.0		10.0	2.0		10.0	V	
Input Offset Voltage	V <sub>OS</sub>		.07	.15 0.6		.15	.35 1.0	mV mV	R <sub>S</sub> ≤ 100KΩ 0°C ≤ T <sub>A</sub> ≤ +70°C
Input Offset Current	I <sub>OS</sub>		.01	10 240		.01	10 240	pA pA	T <sub>A</sub> = 25°C 0°C ≤ T <sub>A</sub> ≤ +70°C
Input Bias Current	I <sub>B</sub>		.01	10 300		.01	10 600	pA pA	T <sub>A</sub> = 25°C 0°C ≤ T <sub>A</sub> ≤ +70°C
Input Voltage Range	V <sub>IR</sub>	-0.3		5.3	-0.3		5.3	V	V+ = +5V V <sub>S</sub> = ±2.5V
		-2.8		2.8	-2.8		2.8	V	
Input Resistance	R <sub>IN</sub>		10 <sup>14</sup>			10 <sup>14</sup>		Ω	
Input Offset Voltage Drift	TCV <sub>OS</sub>		7			7		μV/°C	R <sub>S</sub> ≤ 100KΩ
Power Supply Rejection Ratio	PSRR	65	80		60	80		dB	R <sub>S</sub> ≤ 100KΩ 0°C ≤ T <sub>A</sub> ≤ +70°C
		65	80		60	80		dB	
Common Mode Rejection Ratio	CMRR	65	83		60	83		dB	R <sub>S</sub> ≤ 100KΩ 0°C ≤ T <sub>A</sub> ≤ +70°C
		65	83		60	83		dB	
Large Signal Voltage Gain	A <sub>v</sub>	32	100		32	100		V/ mV	R <sub>L</sub> = 1MΩ R <sub>L</sub> = 1MΩ 0°C ≤ T <sub>A</sub> ≤ +70°C
		20			20			V/ mV	
Output Voltage Range	V <sub>O</sub> low	4.99	0.001	0.01	4.99	0.001	0.01	V	R <sub>L</sub> = 1MΩ 0°C ≤ T <sub>A</sub> ≤ +70°C
			4.999			4.999		V	
	V <sub>O</sub> high	-2.48	-2.40	2.40	-2.48	-2.40	V		
		2.48			2.40		V		
Output Short Circuit Current	I <sub>SC</sub>		200			200		μA	
Supply Current	I <sub>S</sub>		25	40		25	50	μA	V <sub>IN</sub> = 0V No Load
Power Dissipation	P <sub>D</sub>			200			250	μW	V <sub>S</sub> = ±2.5V
Input Capacitance	C <sub>IN</sub>		1			1		pF	
Bandwidth	BW		400			400		KHz	
Slew Rate	SR		.17			.17		V/μs	A <sub>v</sub> = +1 R <sub>L</sub> = 1MΩ

**OPERATING ELECTRICAL CHARACTERISTICS (cont'd)**

**T<sub>A</sub> = 25°C V<sub>S</sub> = ±2.5V unless otherwise specified (cont'd)**

Parameter	Symbol	1726			1726G			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Rise time	t <sub>r</sub>		1.0			1.0		μs	R <sub>L</sub> = 1MΩ
Overshoot Factor			20			20		%	R <sub>L</sub> = 1MΩ, C <sub>L</sub> = 25pF
Settling Time	t <sub>s</sub>		10.0			10.0		μs	0.1% A <sub>V</sub> = 1, R <sub>L</sub> = 1MΩ C <sub>L</sub> = 25pF

**T<sub>A</sub> = 25°C V<sub>S</sub> = ±1.0V unless otherwise specified**

Parameter	Symbol	1726			1726G			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Power Supply Rejection Ratio	PSRR		70			70		dB	R <sub>S</sub> ≤ 1MΩ
Common Mode Rejection Ratio	CMRR		70			70		dB	R <sub>S</sub> ≤ 1MΩ
Large Signal Voltage Gain	A <sub>V</sub>		50			50		V/mV	R <sub>L</sub> = 1MΩ
Output Voltage Range	V <sub>O</sub> low V <sub>O</sub> high	0.9	-0.95 0.95	-0.9	0.9	-0.95 0.95	-0.9	V	R <sub>L</sub> = 1MΩ
Bandwidth	B <sub>W</sub>		0.3			0.3		MHz	
Slew Rate	S <sub>R</sub>		0.17			0.17		V/μs	A <sub>V</sub> = +1, C <sub>L</sub> = 50pF

**V<sub>S</sub> = ±2.5V -55°C ≤ T<sub>A</sub> ≤ +125°C unless otherwise specified**

Parameter	Symbol	1726			1726G			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Input Offset Voltage	V <sub>OS</sub>			1.0			2.0	mV	R <sub>S</sub> ≤ 100KΩ
Input Offset Current	I <sub>OS</sub>			2.0			2.0	nA	
Input Bias Current	I <sub>B</sub>			2.0			2.0	nA	
Power Supply Rejection Ratio	PSRR	60	75		60	75		dB	R <sub>S</sub> ≤ 1MΩ
Common Mode Rejection Ratio	CMRR	60	83		60	83		dB	R <sub>S</sub> ≤ 1MΩ
Large Signal Voltage Gain	A <sub>V</sub>	15	50		15	50		V/mV	R <sub>L</sub> = 1MΩ
Output Voltage Range	V <sub>O</sub> low V <sub>O</sub> high	2.30	-2.40 2.40	-2.30	2.30	-2.40 2.40	-2.30	V V	R <sub>L</sub> = 1MΩ

**Design & Operating Notes:**

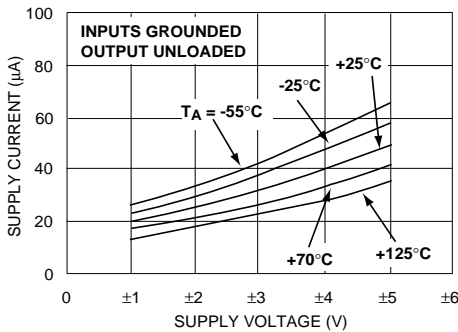
1. The ALD1726/ALD1726G CMOS operational amplifier uses a 3 gain stage architecture and an improved frequency compensation scheme to achieve large voltage gain, high output driving capability, and better frequency stability. In a conventional CMOS operational amplifier design, compensation is achieved with a pole splitting capacitor together with a nulling resistor. This method is, however, very bias dependent and thus cannot accommodate the large range of supply voltage operation as is required from a stand alone CMOS operational amplifier. The ALD1726/ALD1726G is internally compensated for unity gain stability using a novel scheme that does not use a nulling resistor. This scheme produces a clean single pole roll off in the gain characteristics while providing for more than 70 degrees of phase margin at the unity gain frequency.
2. The ALD1726/ALD1726G has complementary p-channel and n-channel input differential stages connected in parallel to accomplish rail to rail input common mode voltage range. This means that with the ranges of common mode input voltage close to the power supplies, one of the two differential stages is switched off internally. To maintain compatibility with other operational amplifiers, this switching point has been selected to be about 1.5V below the positive supply voltage. Since offset voltage trimming on the ALD1726/ALD1726G is made when the input voltage is symmetrical to the supply voltages, this internal switching does not affect a large variety of applications such as an inverting amplifier or non-inverting amplifier with a gain larger than 2.5 (5V operation), where the common mode voltage does not make excursions below this switching point. The user should, however, be aware that this switching does take place if the operational amplifier is connected as a unity gain buffer and should make provision in his design to allow for input offset voltage variations.
3. The input bias and offset currents are essentially input protection diode reverse bias leakage currents, and are typically less than 1pA at room temperature. This low input bias current assures that the analog signal from the source will not be distorted by input bias currents. Normally, this extremely high input impedance of greater

than  $10^{12}\Omega$  would not be a problem as the source impedance would limit the node impedance. However, for applications where source impedance is very high, it may be necessary to limit noise and hum pickup through proper shielding.

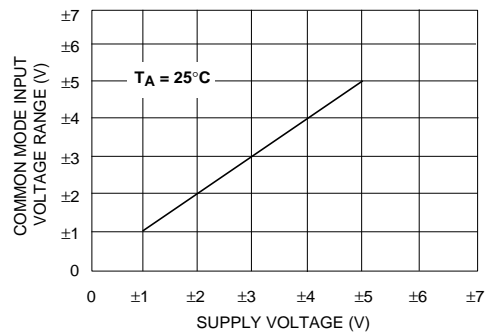
4. The output stage consists of class AB complementary output drivers, capable of driving a low resistance load. The output voltage swing is limited by the drain to source on-resistance of the output transistors as determined by the bias circuitry, and the value of the load resistor. When connected in the voltage follower configuration, the oscillation resistant feature, combined with the rail to rail input and output feature, makes an effective analog signal buffer for medium to high source impedance sensors, transducers, and other circuit networks.
5. ALD1726/ALD1726G operational amplifier has been designed to provide full static discharge protection. Internally, the design has been carefully implemented to minimize latch up. However, care must be exercised when handling the device to avoid strong static fields that may degrade a diode junction, causing increased input leakage currents. In using the operational amplifier, the user is advised to power up the circuit before, or simultaneously with, any input voltages applied and to limit input voltages to not exceed 0.3V of the power supply voltage levels.
6. The ALD1726/ALD1726G, with its micropower operation, offers numerous benefits in reduced power supply requirements, less noise coupling and current spikes, less thermally induced drift, better overall reliability due to lower self heating, and lower input bias current. It requires practically no warm up time as the chip junction heats up to  $0.1^\circ\text{C}$  or less above ambient temperature under most operating conditions.
7. The ALD1726/ALD1726G has an internal design architecture that provides robust high temperature operation. Contact factory for custom screening versions.

**TYPICAL PERFORMANCE CHARACTERISTICS**

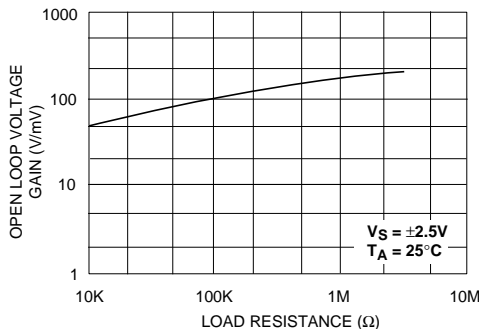
**SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE**



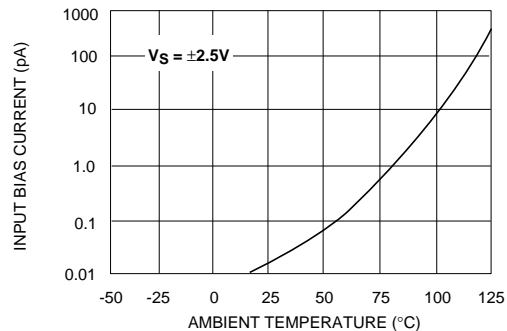
**COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE**



**OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE**

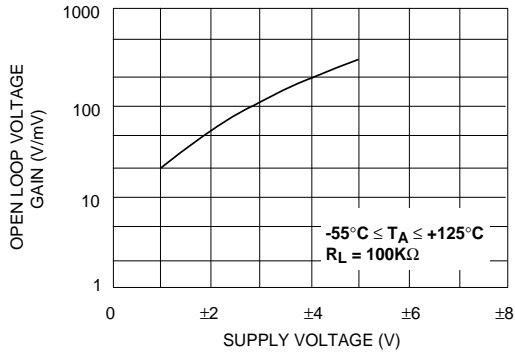


**INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE**

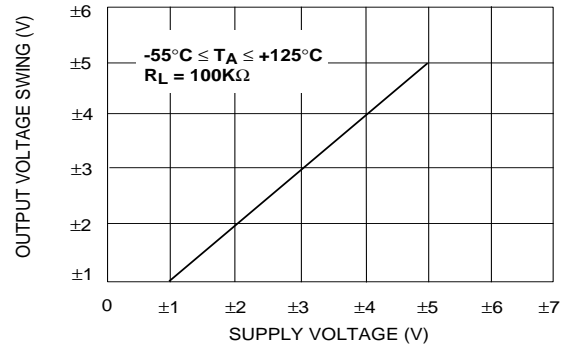


**TYPICAL PERFORMANCE CHARACTERISTICS (cont'd)**

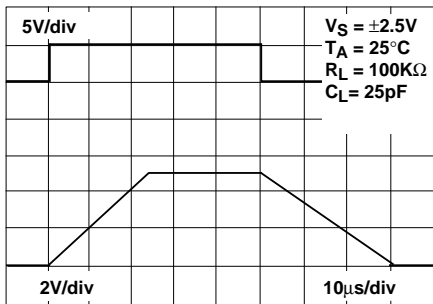
**OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE AND TEMPERATURE**



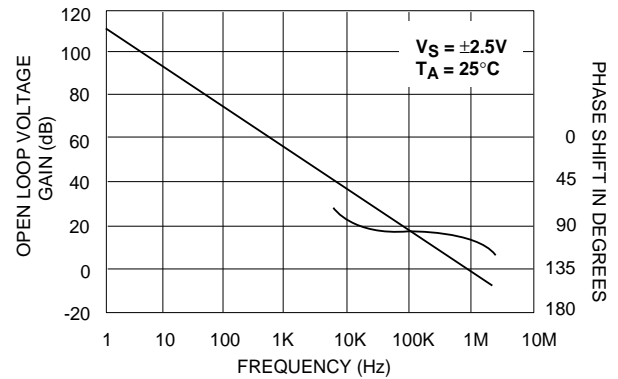
**OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE**



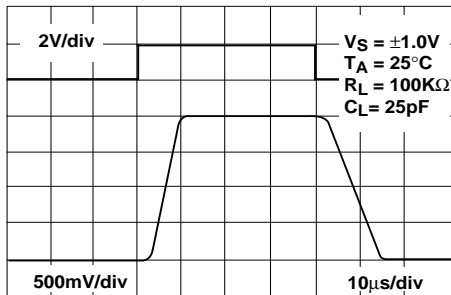
**LARGE - SIGNAL TRANSIENT RESPONSE**



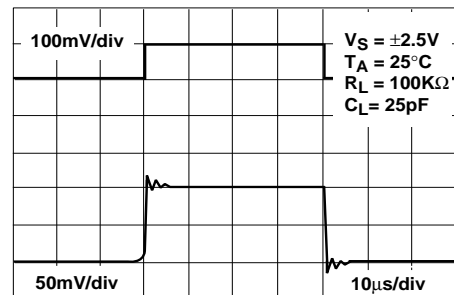
**OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY**



**LARGE - SIGNAL TRANSIENT RESPONSE**

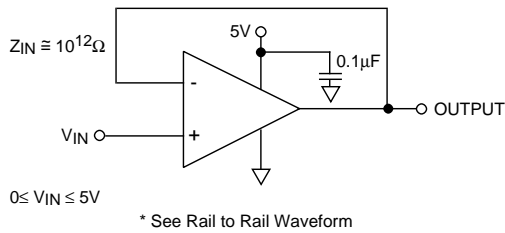


**SMALL - SIGNAL TRANSIENT RESPONSE**

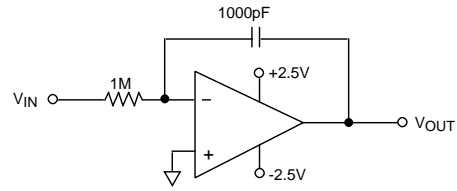


**TYPICAL APPLICATIONS**

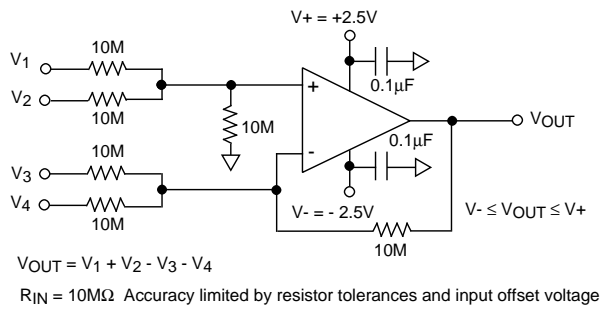
**RAIL-TO-RAIL VOLTAGE FOLLOWER/BUFFER**



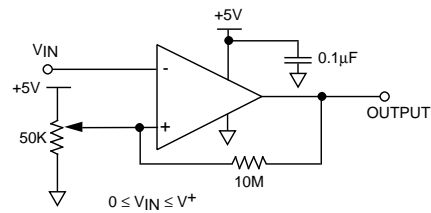
**CHARGE INTEGRATOR**



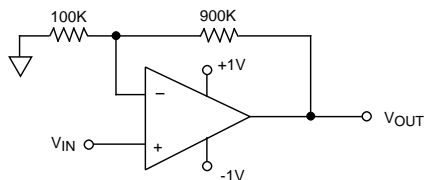
**HIGH INPUT IMPEDANCE RAIL-TO-RAIL PRECISION DC SUMMING AMPLIFIER**



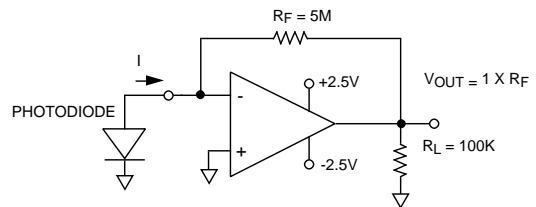
**RAIL-TO-RAIL VOLTAGE COMPARATOR**



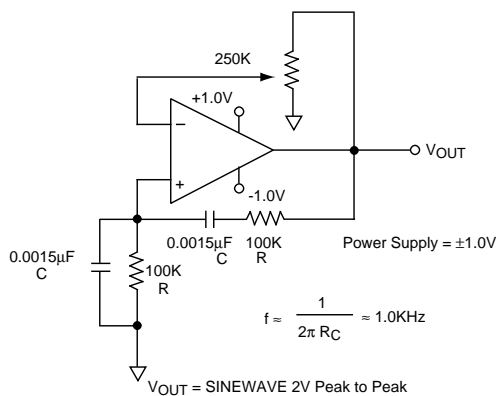
**HIGH IMPEDANCE NON-INVERTING AMPLIFIER**



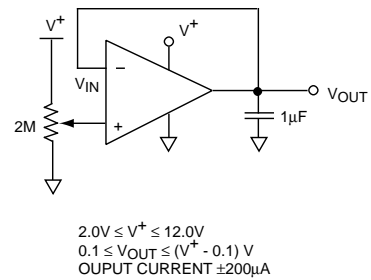
**PHOTO DETECTOR CURRENT TO VOLTAGE CONVERTER**



**WIEN BRIDGE OSCILLATOR**

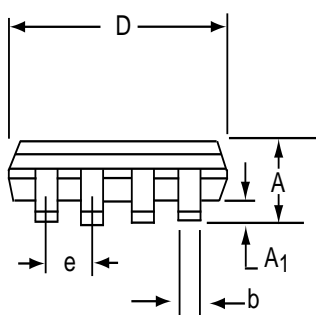
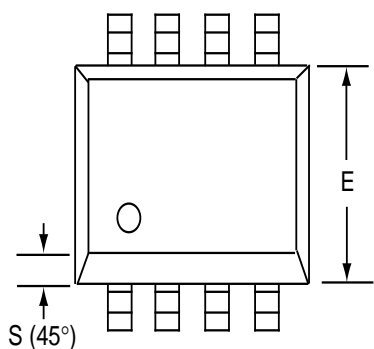


**MICROPOWER BUFFERED VARIABLE VOLTAGE SOURCE**

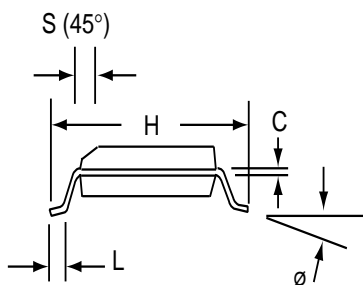


### SOIC-8 PACKAGE DRAWING

#### 8 Pin Plastic SOIC Package



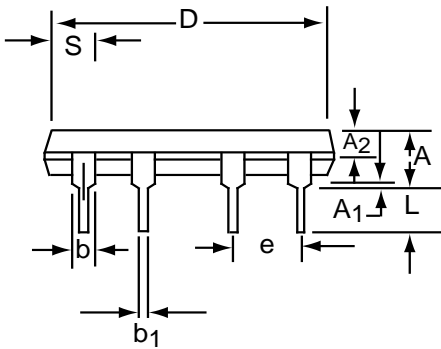
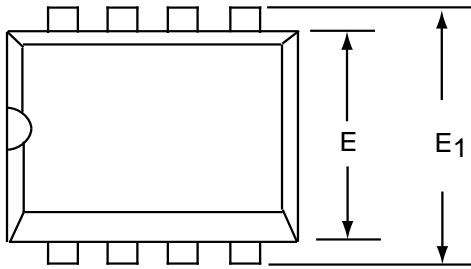
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.25	0.004	0.010
b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-8	4.69	5.00	0.185	0.196
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
∅	0°	8°	0°	8°
S	0.25	0.50	0.010	0.020



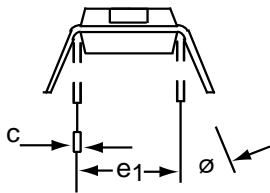


**PDIP-8 PACKAGE DRAWING**

**8 Pin Plastic DIP Package**

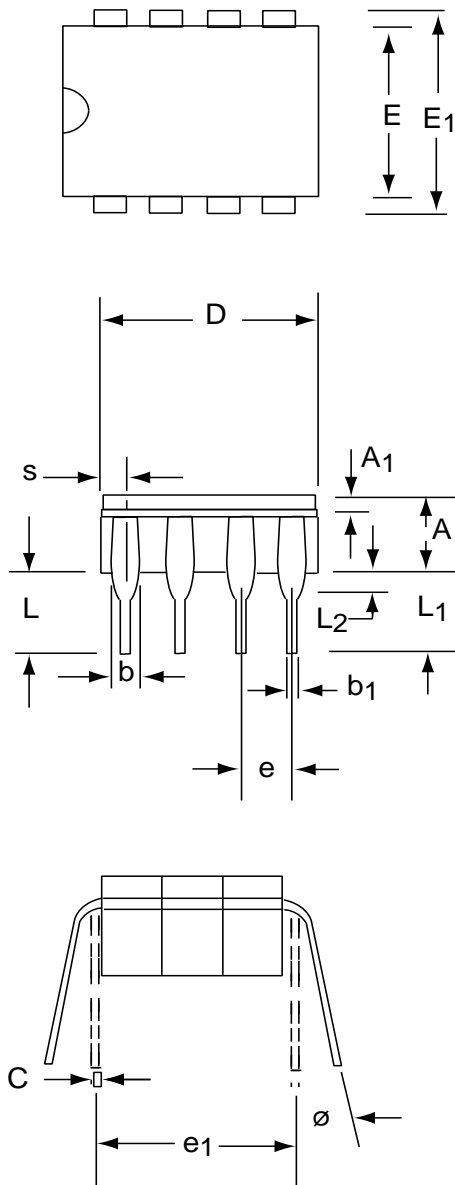


Dim	Millimeters		Inches	
	Min	Max	Min	Max
<b>A</b>	3.81	5.08	0.105	0.200
<b>A<sub>1</sub></b>	0.38	1.27	0.015	0.050
<b>A<sub>2</sub></b>	1.27	2.03	0.050	0.080
<b>b</b>	0.89	1.65	0.035	0.065
<b>b<sub>1</sub></b>	0.38	0.51	0.015	0.020
<b>c</b>	0.20	0.30	0.008	0.012
<b>D-8</b>	9.40	11.68	0.370	0.460
<b>E</b>	5.59	7.11	0.220	0.280
<b>E<sub>1</sub></b>	7.62	8.26	0.300	0.325
<b>e</b>	2.29	2.79	0.090	0.110
<b>e<sub>1</sub></b>	7.37	7.87	0.290	0.310
<b>L</b>	2.79	3.81	0.110	0.150
<b>S-8</b>	1.02	2.03	0.040	0.080
<b>∅</b>	0°	15°	0°	15°



### CERDIP-8 PACKAGE DRAWING

#### 8 Pin CERDIP Package



Dim	Millimeters		Inches	
	Min	Max	Min	Max
<b>A</b>	3.55	5.08	0.140	0.200
<b>A<sub>1</sub></b>	1.27	2.16	0.050	0.085
<b>b</b>	0.97	1.65	0.038	0.065
<b>b<sub>1</sub></b>	0.36	0.58	0.014	0.023
<b>C</b>	0.20	0.38	0.008	0.015
<b>D-8</b>	--	10.29	--	0.405
<b>E</b>	5.59	7.87	0.220	0.310
<b>E<sub>1</sub></b>	7.73	8.26	0.290	0.325
<b>e</b>	2.54 BSC		0.100 BSC	
<b>e<sub>1</sub></b>	7.62 BSC		0.300 BSC	
<b>L</b>	3.81	5.08	0.150	0.200
<b>L<sub>1</sub></b>	3.18	--	0.125	--
<b>L<sub>2</sub></b>	0.38	1.78	0.015	0.070
<b>S</b>	--	2.49	--	0.098
<b>∅</b>	0°	15°	0°	15°