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[Vishay/Siliconix](#)
[SI4340CDY-T1-E3](#)

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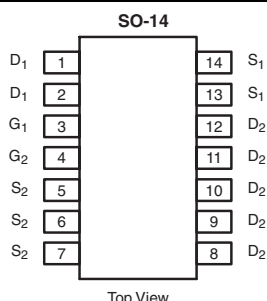


Si4340CDY
 Vishay Siliconix

Dual N-Channel 20-V (D-S) MOSFET with Schottky Diode

PRODUCT SUMMARY				
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
Channel-1	20	0.0094 at V _{GS} = 10 V	14.1	9.6
		0.0125 at V _{GS} = 4.5 V	12.2	
Channel-2	20	0.008 at V _{GS} = 10 V	20	14.1
		0.0095 at V _{GS} = 4.5 V	18.9	

SCHOTTKY PRODUCT SUMMARY		
V _{DS} (V)	V _{SD} (V) Diode Forward Voltage	I _F (A)
20	0.55 V at 2.5 A	2



Top View

Ordering Information: Si4340CDY-T1-E3 (Lead (Pb)-free)
 Si4340CDY-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

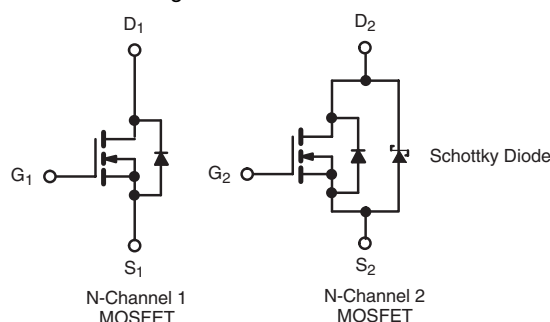
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
 COMPLIANT
 HALOGEN
FREE
 Available

APPLICATIONS

- DC/DC Converters
 - Game Stations
 - Notebook PC Logic



ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted					
Parameter	Symbol	Channel-1	Channel-2	Unit	
Drain-Source Voltage	V _{DS}	20	20	V	
Gate-Source Voltage	V _{GS}	± 20	± 16		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	14.1	A	
		T _C = 70 °C	11.2		
		T _A = 25 °C	11.5 ^{b, c}		
		T _A = 70 °C	9.2 ^{b, c}		
Pulsed Drain Current	I _{DM}	40	50	A	
Source-Drain Current Diode Current	I _S	T _C = 25 °C	2.5		4.5
		T _A = 25 °C	1.7 ^{b, c}	2.5 ^{b, c}	
Single Pulse Avalanche Current	I _{AS}	5		mJ	
Single Pulse Avalanche Energy	E _{AS}	1.25			
Maximum Power Dissipation	P _D	T _C = 25 °C	3	5.4	W
		T _C = 70 °C	1.9	3.5	
		T _A = 25 °C	2 ^{b, c}	3 ^{b, c}	
		T _A = 70 °C	1.3 ^{b, c}	1.9 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C	

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	Channel-1		Channel-2		Unit	
		Typ.	Max.	Typ.	Max.		
Maximum Junction-to-Ambient ^{b, d}	R _{thJA}	53	62.5	35	42	°C/W	
Maximum Junction-to-Foot (Drain)	R _{thJF}	35	42	18	23		

Notes:

- Based on T_C = 25 °C.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under Steady State conditions for channel 1 is 110 °C/W and channel 2 is 87 °C/W.

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SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch-1	20			V
		$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch-2	20			
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	Ch-1		20		mV/°C
		$I_D = 25\text{ mA}$	Ch-2		22		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	Ch-1		- 5.5		
		$I_D = 25\text{ mA}$	Ch-2		- 2.5		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-1	1		3	V
		$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-2	0.8		2.2	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	Ch-1			100	nA
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 16\text{ V}$	Ch-2			100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	Ch-1			1	μA
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	Ch-2			100	
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 85\text{ }^\circ\text{C}$	Ch-1			15	
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 85\text{ }^\circ\text{C}$	Ch-2			10 000	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-1	20			A
		$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-2	30			
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 11.5\text{ A}$	Ch-1		0.0077	0.0094	Ω
		$V_{GS} = 10\text{ V}, I_D = 15.2\text{ A}$	Ch-2		0.0065	0.008	
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	Ch-1		0.010	0.0125	
		$V_{GS} = 4.5\text{ V}, I_D = 14\text{ A}$	Ch-2		0.0075	0.0095	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 11.5\text{ A}$	Ch-1		45		S
		$V_{DS} = 10\text{ V}, I_D = 15.2\text{ A}$	Ch-2		73		
Dynamic^a							
Input Capacitance	C_{iss}	Channel-1 $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ Channel-2 $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1		1300		pF
			Ch-2		1900		
Output Capacitance	C_{oss}		Ch-1		330		
			Ch-2		500		
Reverse Transfer Capacitance	C_{rss}		Ch-1		150		
			Ch-2		160		
Total Gate Charge	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}, I_D = 11.5\text{ A}$	Ch-1		21	32	nC
		$V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}, I_D = 15.2\text{ A}$	Ch-2		31	47	
		Channel-1 $V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 11.5\text{ A}$	Ch-1		9.6	15	
			Ch-2		14.1	22	
Gate-Source Charge	Q_{gs}	Channel-2 $V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 15.2\text{ A}$	Ch-1		4		
			Ch-2		5		
Gate-Drain Charge	Q_{gd}	Ch-1		3			
		Ch-2		3.5			
Gate Resistance	R_g	$f = 1\text{ MHz}$	Ch-1		0.65	1.2	Ω
			Ch-2		1.4	2.8	

Notes:

- a. Guaranteed by design, not subject to production testing.
 b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.



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SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Dynamic^a							
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = 10\text{ V}, R_L = 1.1\text{ }\Omega$ $I_D \cong 9.2\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$	Ch-1		20	30	ns
			Ch-2		22	35	
Rise Time	t_r		Ch-1		10	15	
			Ch-2		10	15	
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 $V_{DD} = 10\text{ V}, R_L = 1\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$	Ch-1		20	30	
			Ch-2		32	50	
Fall Time	t_f		Ch-1		10	15	
			Ch-2		10	15	
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = 10\text{ V}, R_L = 1.1\text{ }\Omega$ $I_D \cong 9.2\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$	Ch-1		10	15	
			Ch-2		10	15	
Rise Time	t_r		Ch-1		10	15	
			Ch-2		10	15	
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 $V_{DD} = 10\text{ V}, R_L = 1\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$	Ch-1		20	30	
			Ch-2		25	40	
Fall Time	t_f		Ch-1		10	15	
			Ch-2		10	15	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$	Ch-1			2.5	A
			Ch-2			4.5	
Pulse Diode Forward Current ^a	I_{SM}		Ch-1			40	
			Ch-2			50	
Body Diode Voltage	V_{SD}	$I_S = 9.2\text{ A}$	Ch-1		0.8	1.2	V
		$I_S = 2.5\text{ A}$	Ch-2		0.45	0.55	
Body Diode Reverse Recovery Time	t_{rr}	Channel-1 $I_F = 9.2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	Ch-1		30	60	ns
			Ch-2		30	60	
Body Diode Reverse Recovery Charge	Q_{rr}	Channel-2 $I_F = 2.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	Ch-1		15	25	nC
			Ch-2		20	30	
Reverse Recovery Fall Time	t_a		Ch-1		12		ns
			Ch-2		14		
Reverse Recovery Rise Time	t_b		Ch-1		18		
			Ch-2		16		

Notes:

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

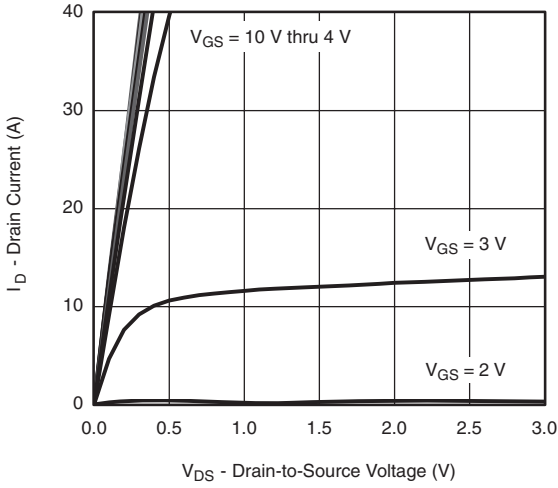
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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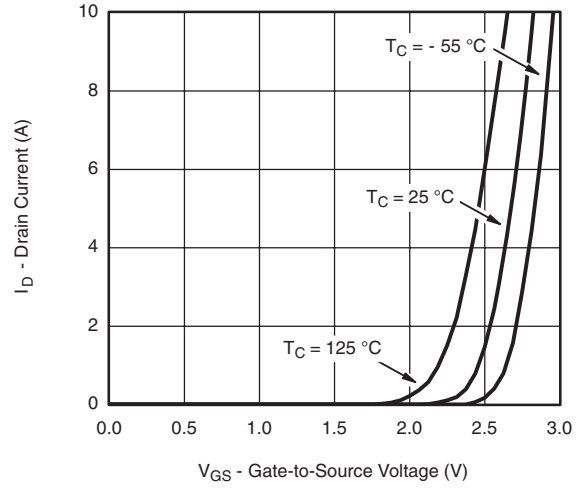
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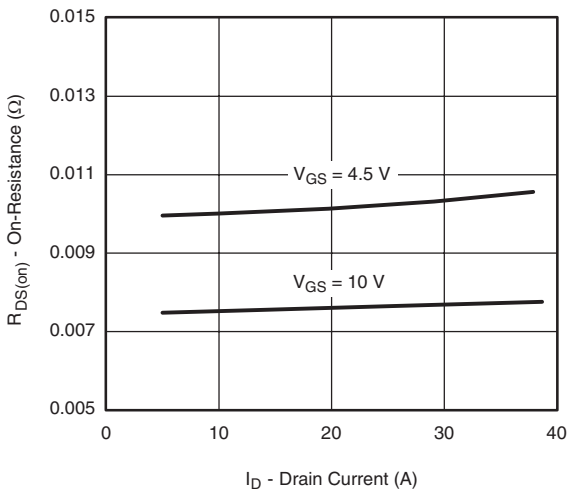
CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



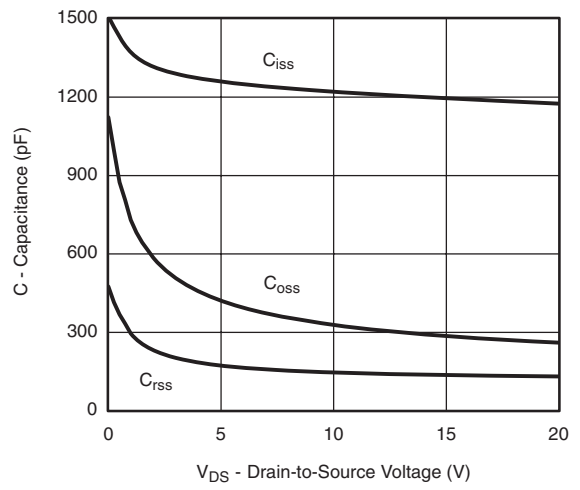
Output Characteristics



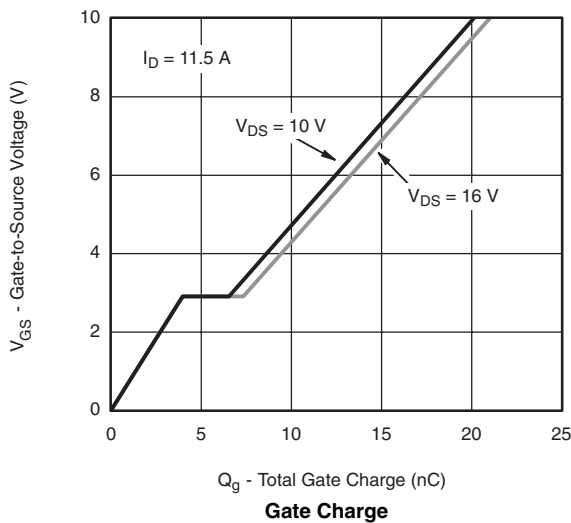
Transfer Characteristics



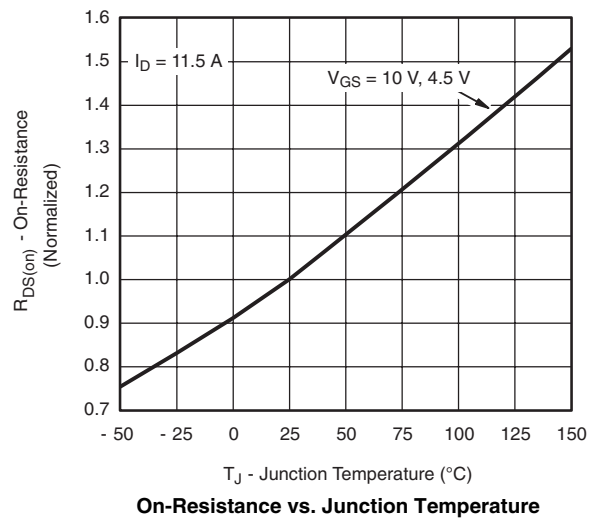
On-Resistance vs. Drain Current



Capacitance



Gate Charge

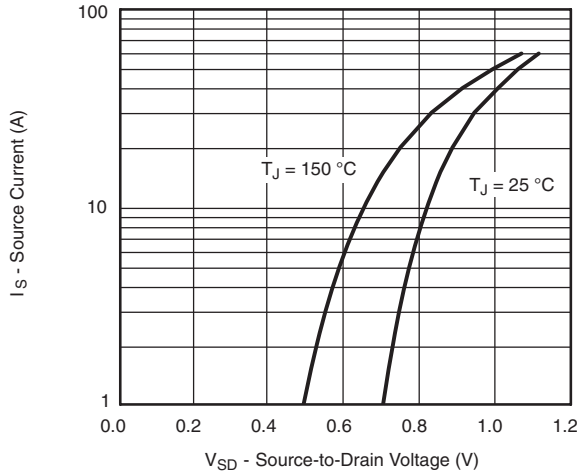


On-Resistance vs. Junction Temperature

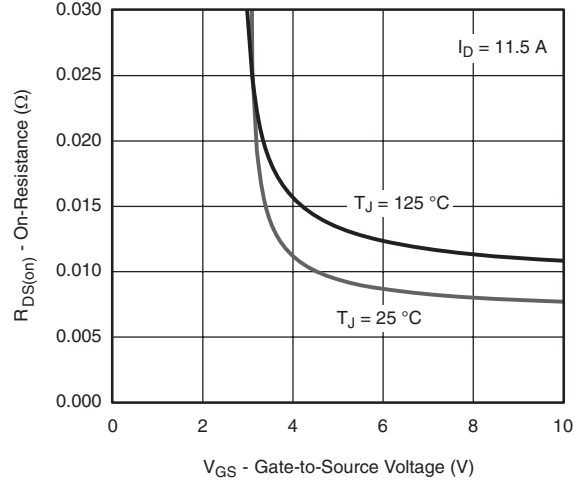


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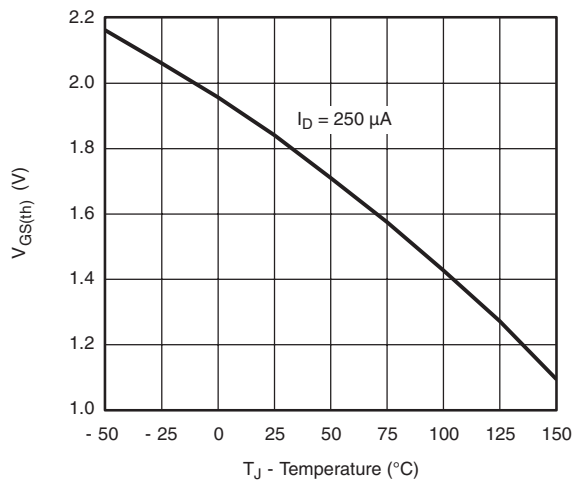
CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



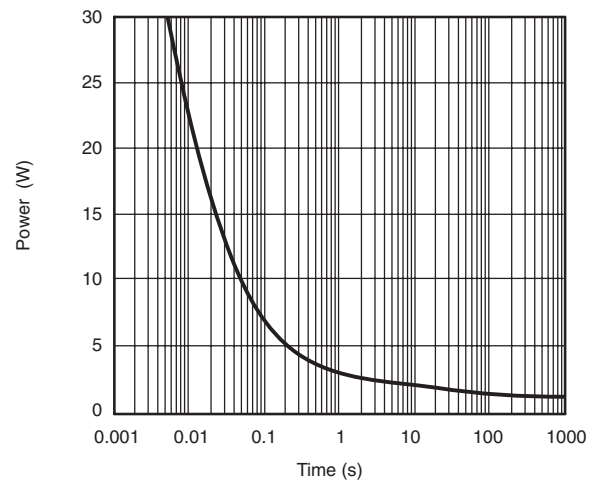
Source-Drain Diode Forward Voltage



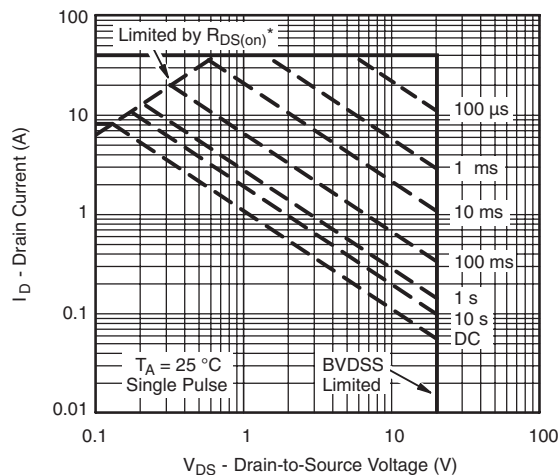
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



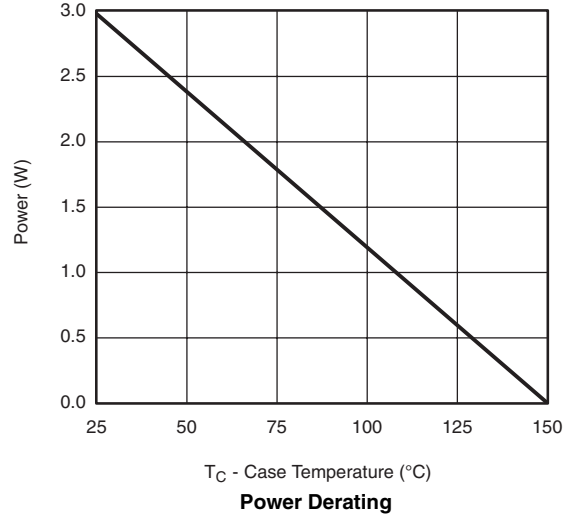
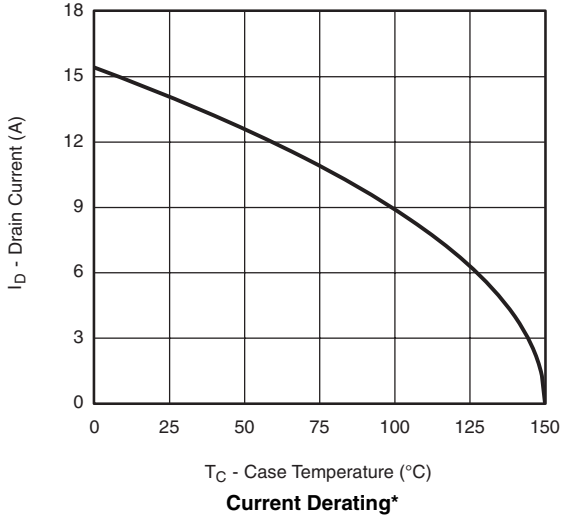
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

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CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

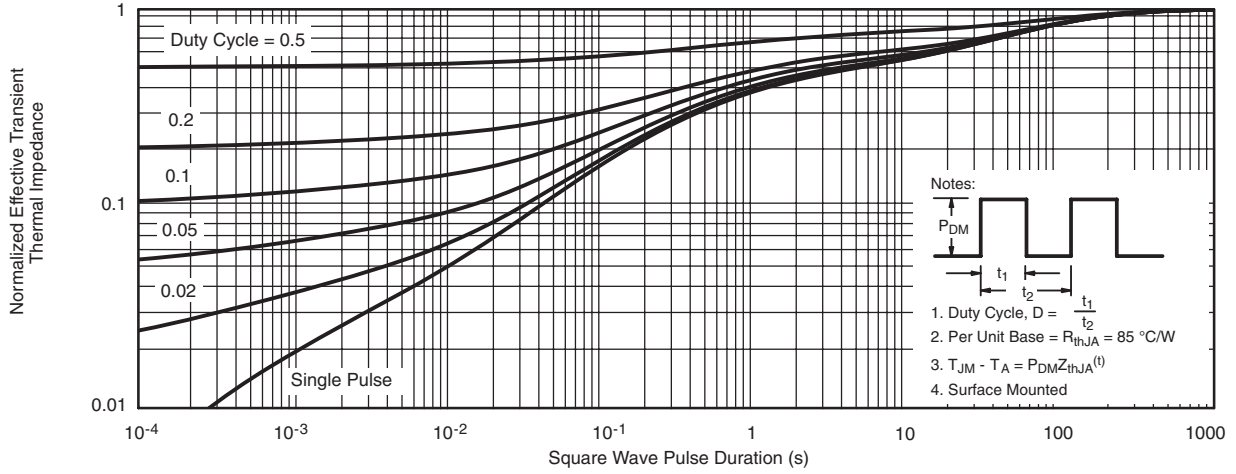


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

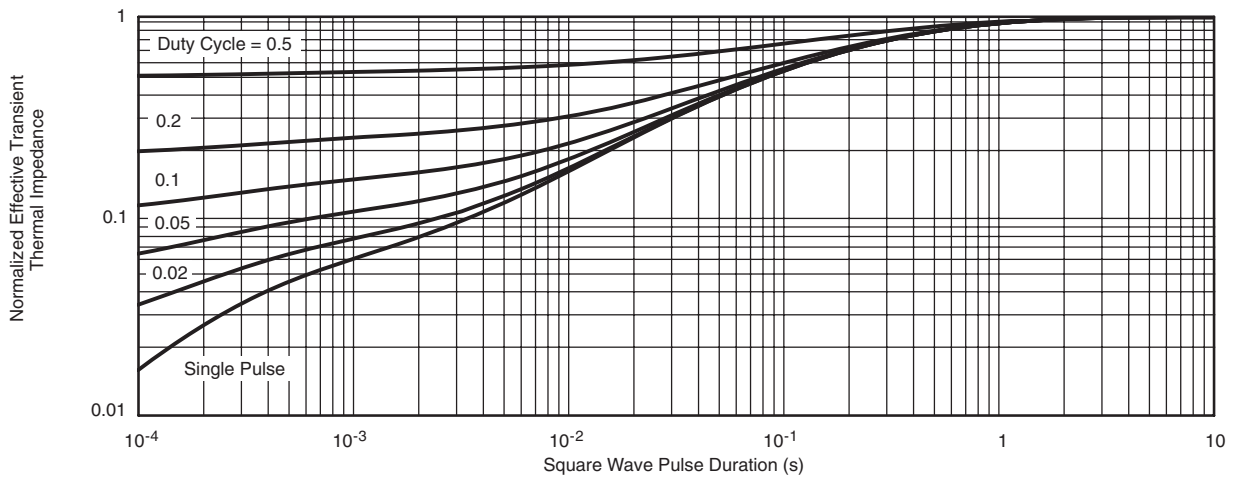


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CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient

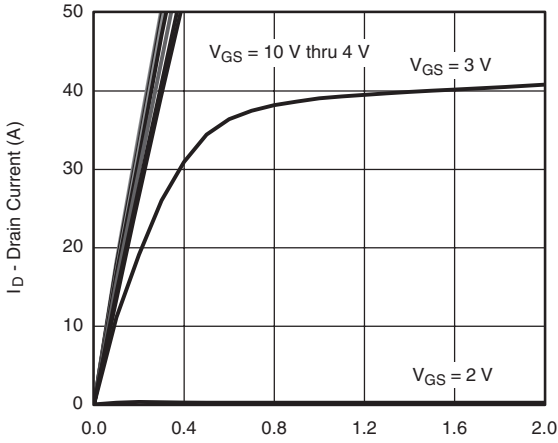


Normalized Thermal Transient Impedance, Junction-to-Foot

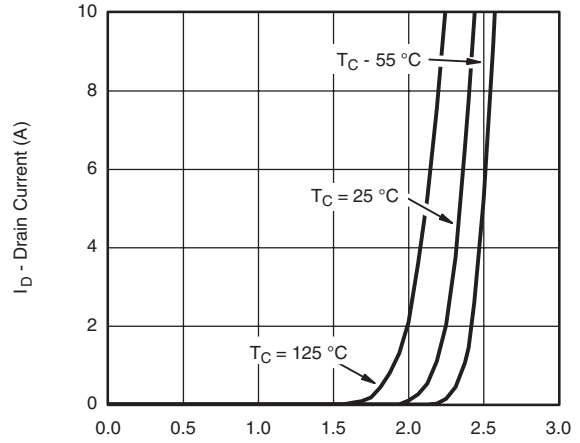
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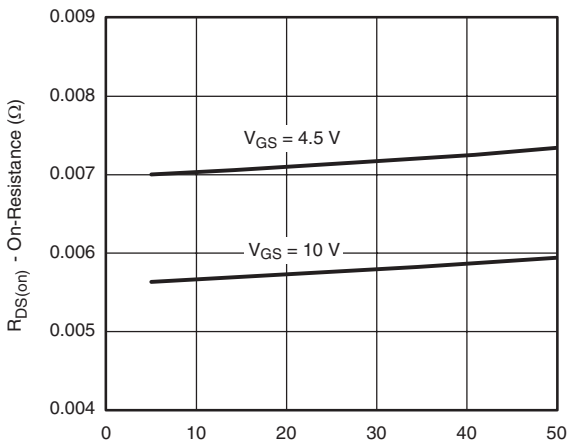
CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



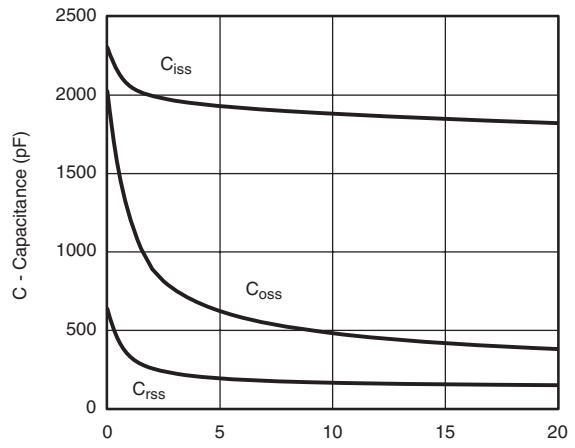
Output Characteristics



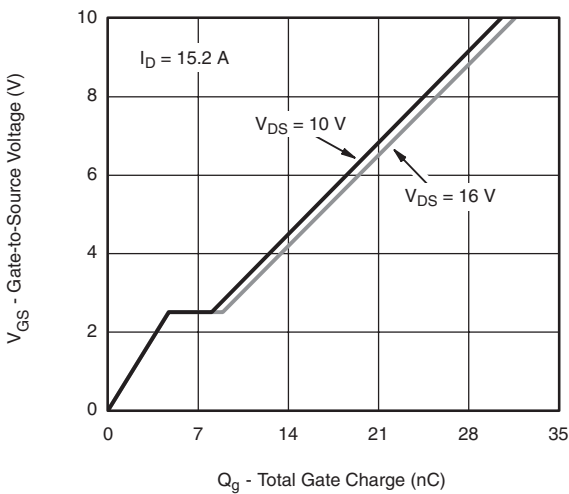
Transfer Characteristics



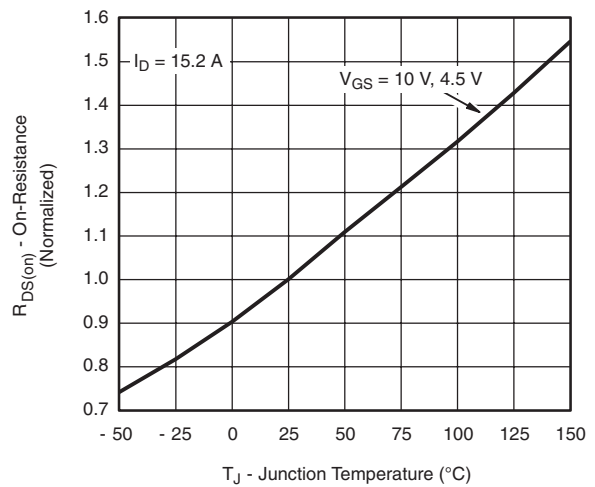
On-Resistance vs. Drain Current



Capacitance



Gate Charge

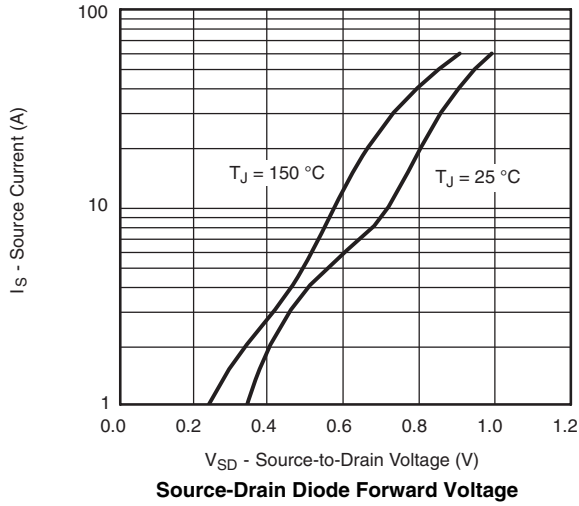


On-Resistance vs. Junction Temperature

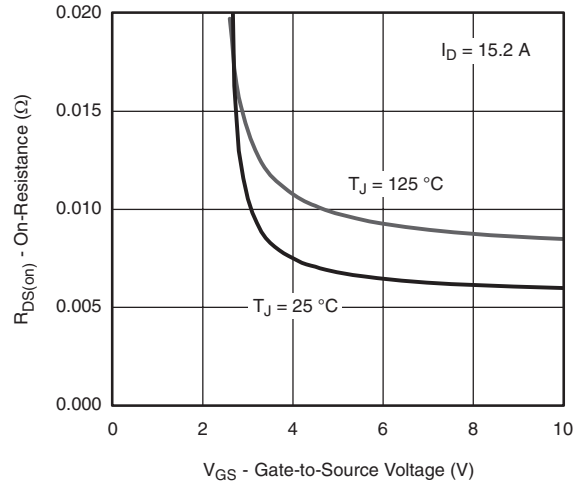


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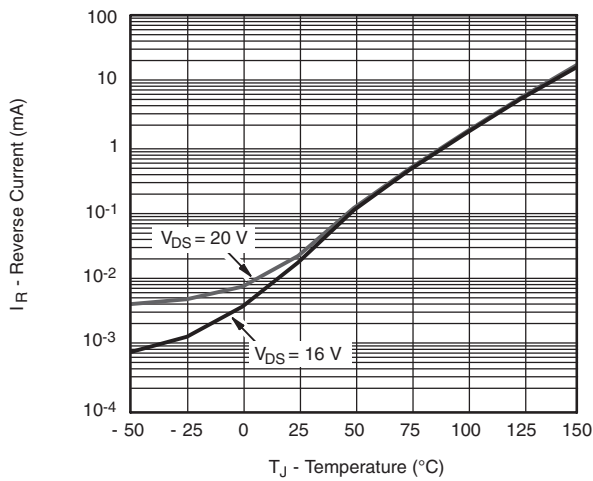
CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



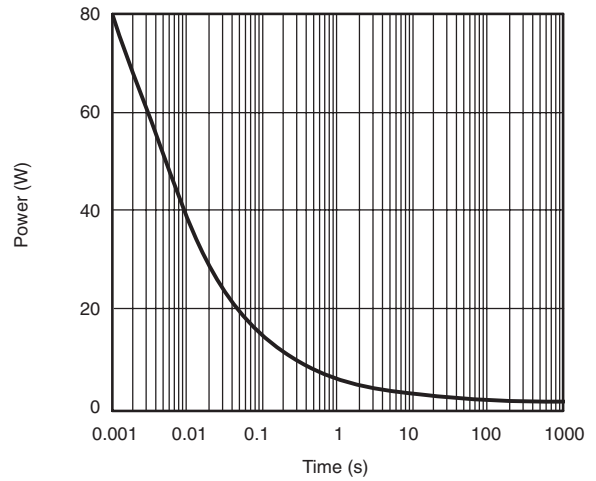
Source-Drain Diode Forward Voltage



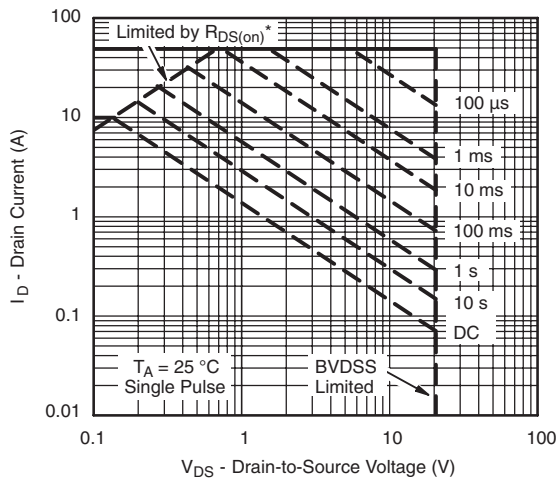
On-Resistance vs. Gate-to-Source Voltage



Reverse Current vs. Junction Temperature



Single Pulse Power



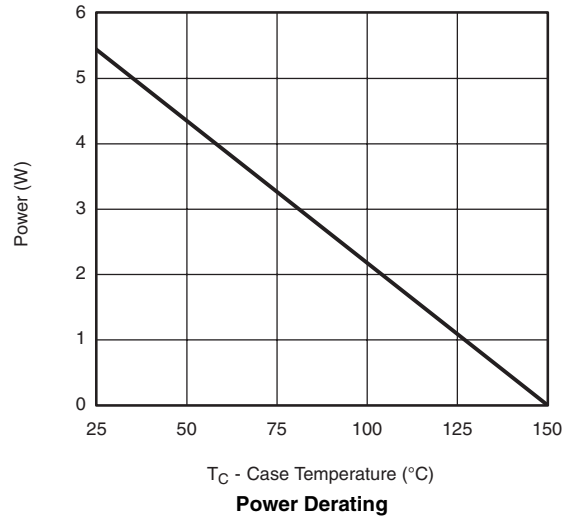
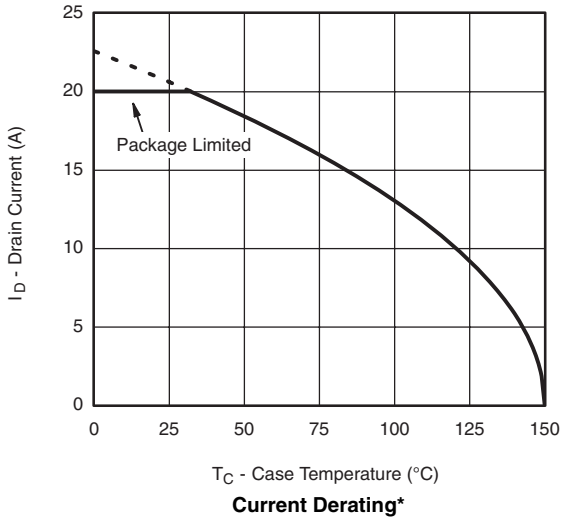
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

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CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

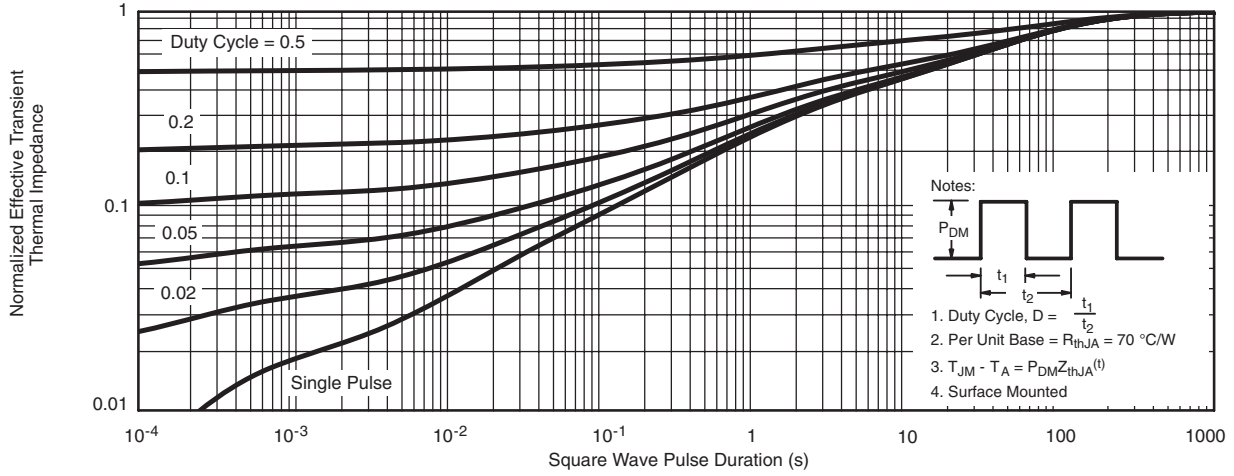


* The power dissipation P_D is based on $T_{J(max)} = 150\text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

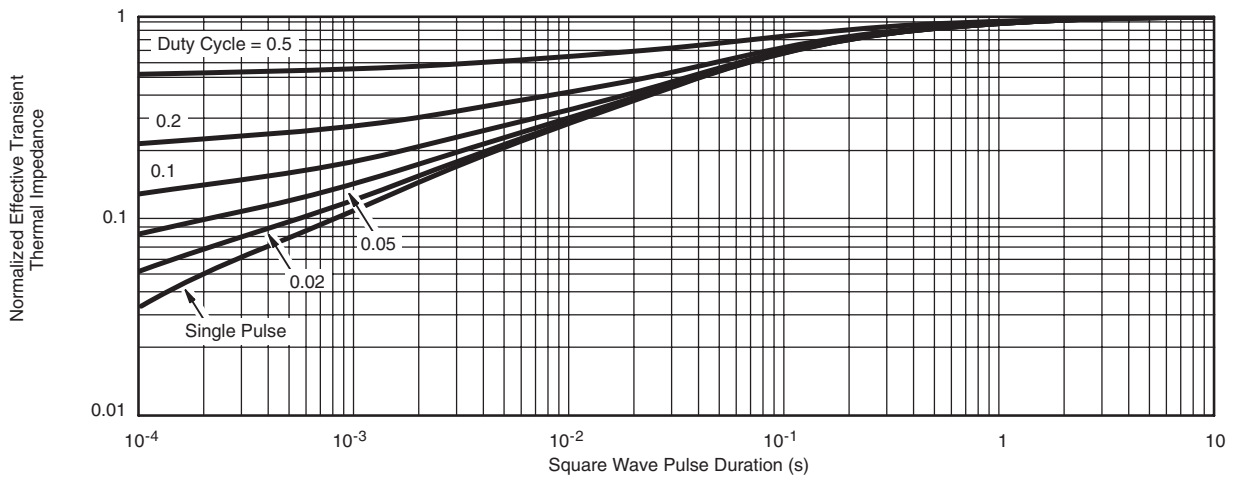


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CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68398.



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