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[Vishay/Siliconix](#)
[SIB422EDK-T1-GE3](#)

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sales@integrated-circuit.com


SiB422EDK
 Vishay Siliconix

N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
20	0.030 at V _{GS} = 4.5 V	9	6 nC
	0.041 at V _{GS} = 2.5 V	9	
	0.057 at V _{GS} = 1.8 V	9	
	0.082 at V _{GS} = 1.5 V	5	

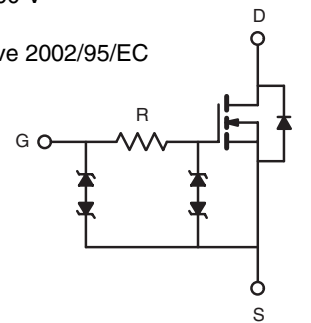
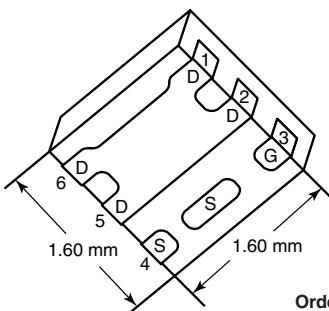
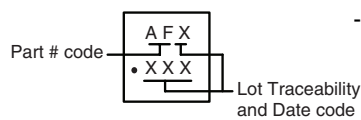
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® SC-75 Package
 - Small Footprint Area
 - Low On-Resistance
 - Thin 0.75 mm Profile
- Typical ESD Protection 4000 V
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC


RoHS
 COMPLIANT
 HALOGEN
FREE

APPLICATIONS

- Portable Devices
- Load Switch
- Battery Switch


PowerPAK SC-75-6L-Single

Marking Code

Ordering Information: SIB422EDK-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	± 8	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	9 ^a
		T _C = 70 °C	9 ^a
		T _A = 25 °C	7.1 ^{b, c}
		T _A = 70 °C	5.7 ^{b, c}
Pulsed Drain Current	I _{DM}	25	
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	9 ^a
		T _A = 25 °C	2.1 ^{b, c}
Maximum Power Dissipation	P _D	T _C = 25 °C	13
		T _C = 70 °C	8.4
		T _A = 25 °C	2.5 ^{b, c}
		T _A = 70 °C	1.6 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	41	51	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	7.5	9.5	

Notes:

- Package limited, T_C = 25 °C.
- Surface Mounted on 1" x 1" FR4 board.
- t = 5 s.
- See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK SC-75 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 105 °C/W.

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SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		18		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 2.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.4		1.0	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 4.5\text{ V}$			± 1.5	μA
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			± 25	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			1 10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 4.5\text{ V}$	15			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$		0.025	0.030	Ω
		$V_{GS} = 2.5\text{ V}, I_D = 4.3\text{ A}$		0.034	0.041	
		$V_{GS} = 1.8\text{ V}, I_D = 1.5\text{ A}$		0.046	0.057	
		$V_{GS} = 1.5\text{ V}, I_D = 1\text{ A}$		0.055	0.082	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 5\text{ A}$		28		S
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 8\text{ V}, I_D = 7.1\text{ A}$		11.5	18	nC
				6	9	
Gate-Source Charge	Q_{gs}	$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 7.1\text{ A}$		0.8		
Gate-Drain Charge	Q_{gd}			1.6		
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.46	2.3	4.6	k Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 1.8\text{ }\Omega$ $I_D \cong 5.7\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		0.3	0.45	μs
Rise Time	t_r			0.6	0.9	
Turn-Off Delay Time	$t_{d(off)}$			3.8	6	
Fall Time	t_f			1.7	2.6	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 1.8\text{ }\Omega$ $I_D \cong 5.7\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		0.15	0.25	
Rise Time	t_r			0.3	0.45	
Turn-Off Delay Time	$t_{d(off)}$			5.6	9	
Fall Time	t_f			1.6	2.5	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			9	A
Pulse Diode Forward Current	I_{SM}				25	
Body Diode Voltage	V_{SD}	$I_S = 5.7\text{ A}, V_{GS} = 0\text{ V}$		0.85	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 5.7\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		15	30	ns
Body Diode Reverse Recovery Charge	Q_{rr}			7.5	15	nC
Reverse Recovery Fall Time	t_a			8		ns
Reverse Recovery Rise Time	t_b			15		

Notes:

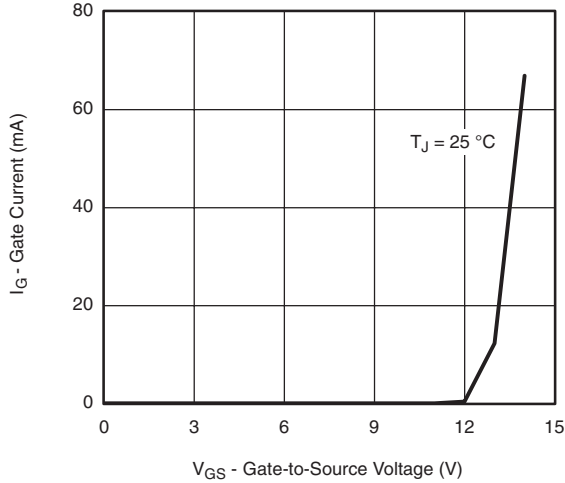
- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

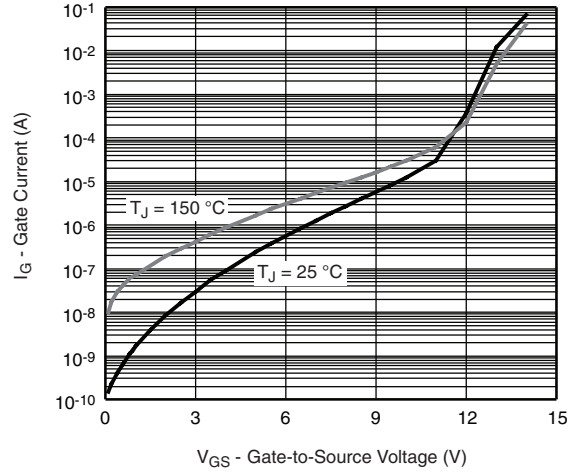


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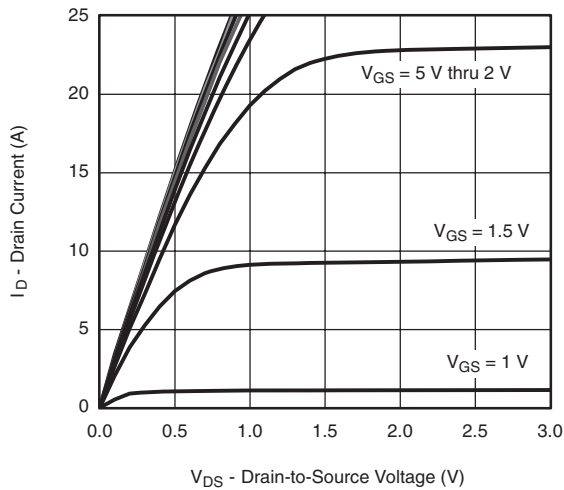
TYPICAL CHARACTERISTICS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted



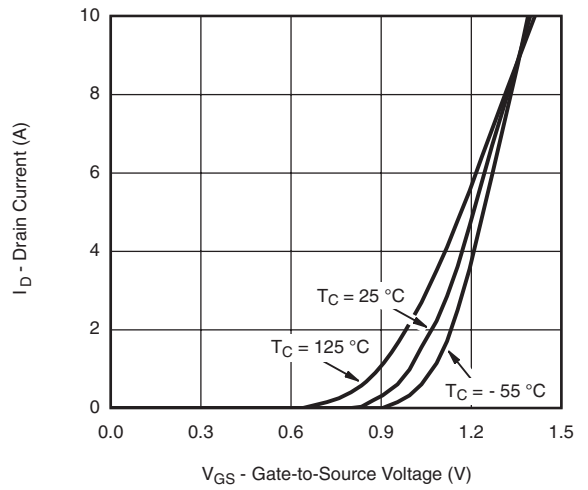
Gate Current vs. Gate-to-Source Voltage



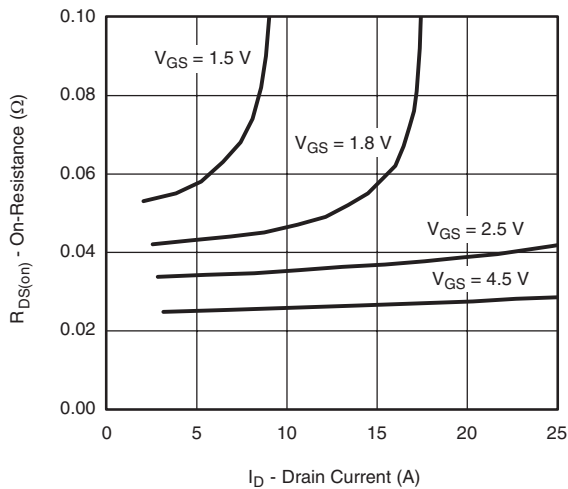
Gate Current vs. Gate-to-Source Voltage



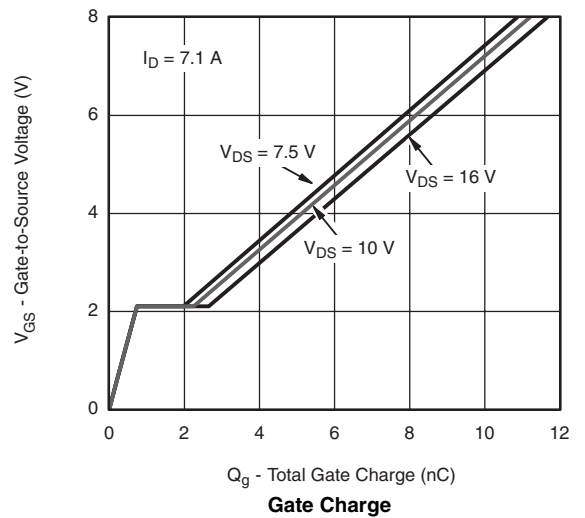
Output Characteristics



Transfer Characteristics



On-Resistance vs. Drain Current



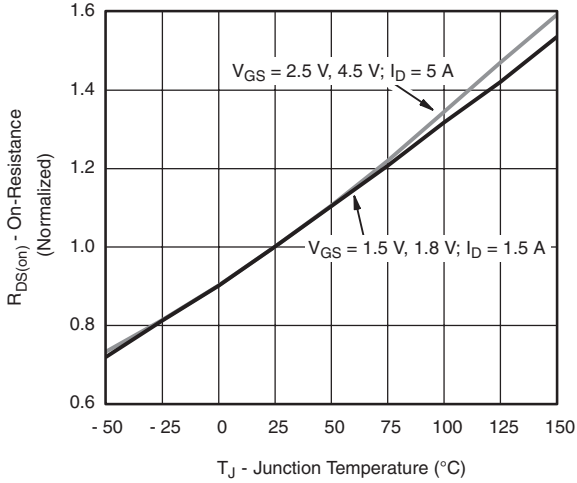
Gate Charge

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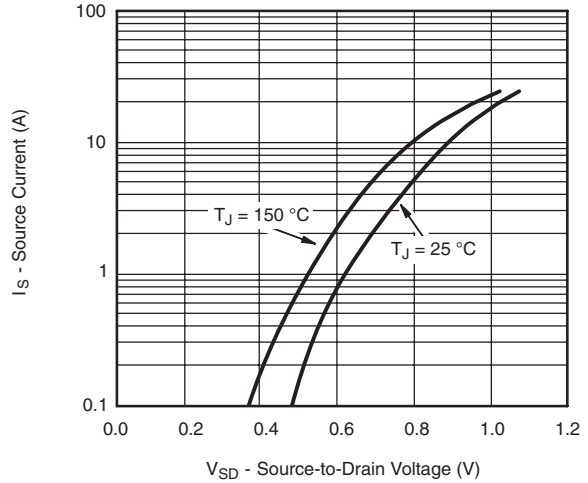
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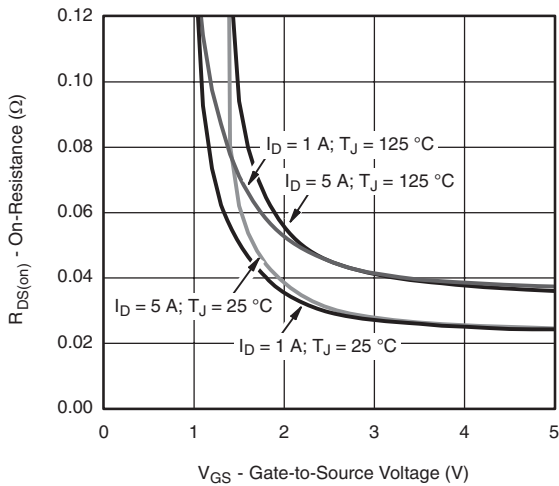
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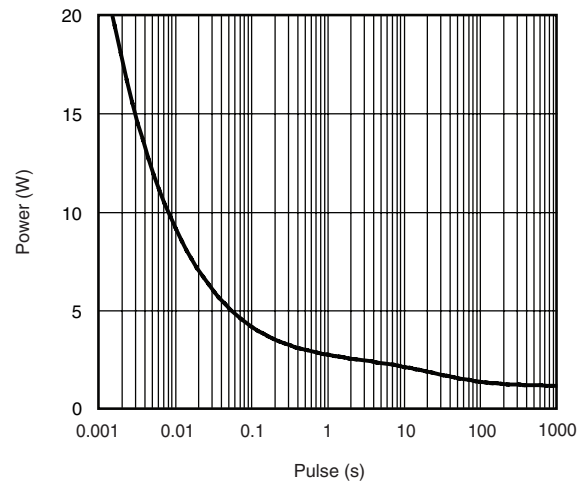
Normalized On-Resistance vs. Junction Temperature



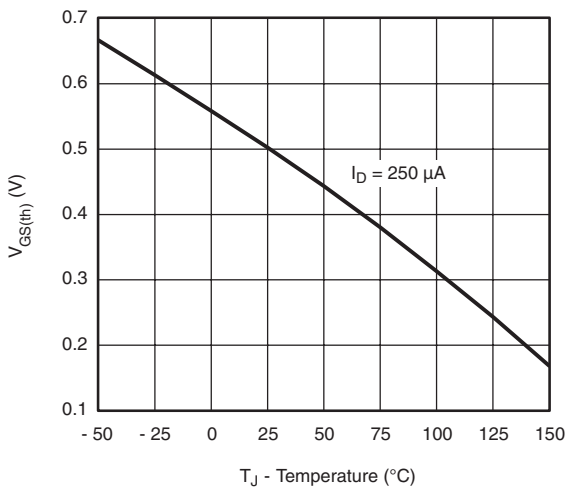
Source-Drain Diode Forward Voltage



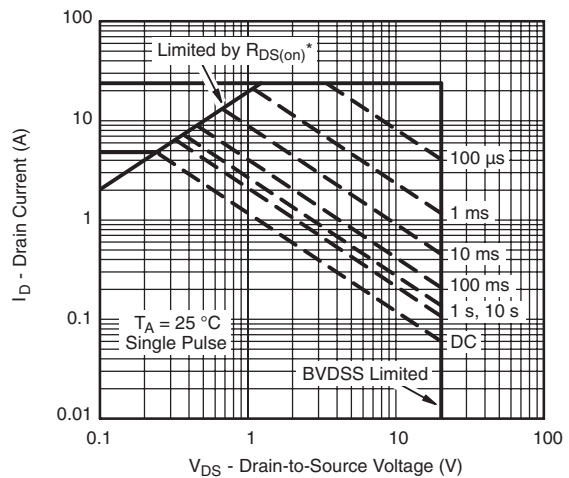
On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



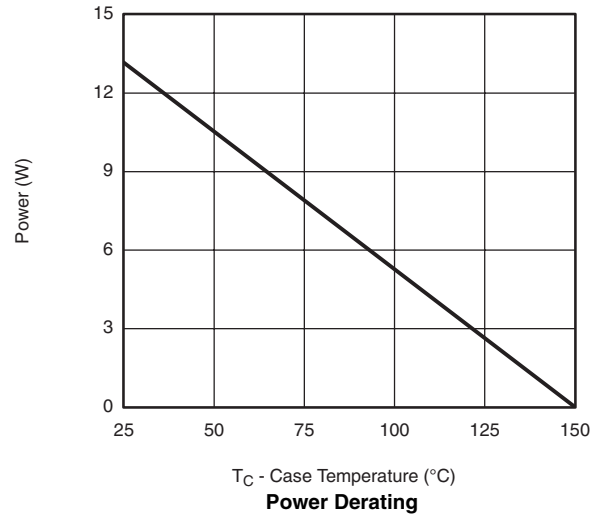
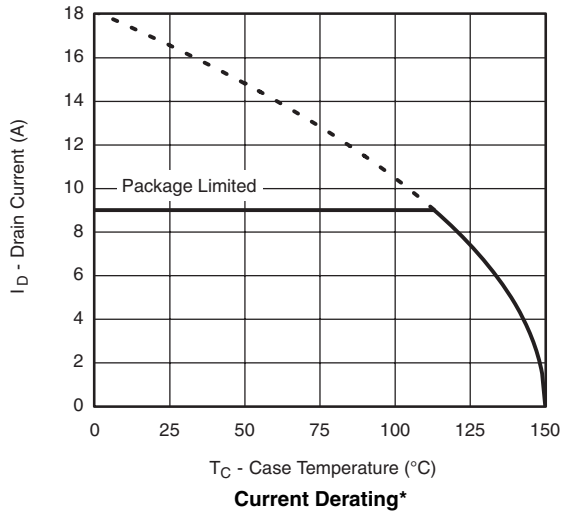
Threshold Voltage



Safe Operating Area, Junction-to-Ambient



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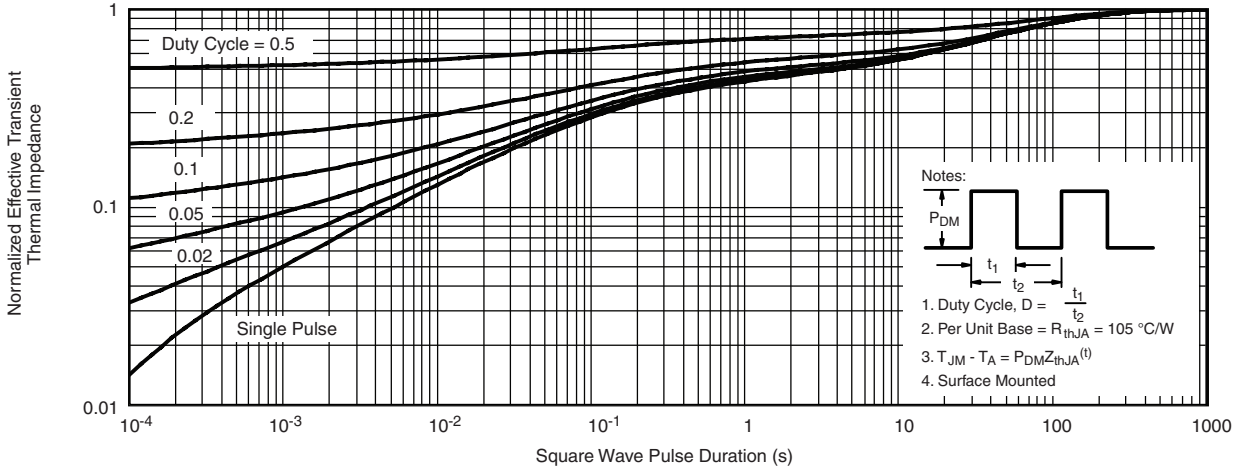
* The power dissipation P_D is based on $T_{J(max)} = 150\text{ }^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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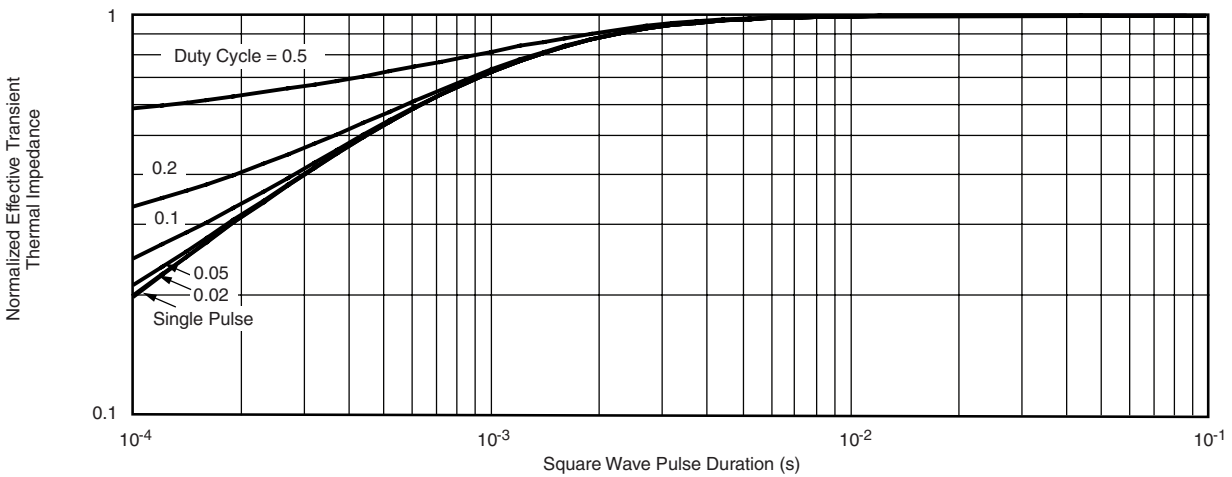
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TYPICAL CHARACTERISTICS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

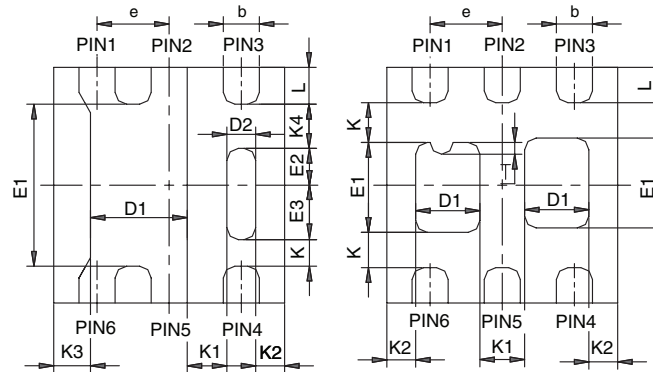
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65297.



Package Information

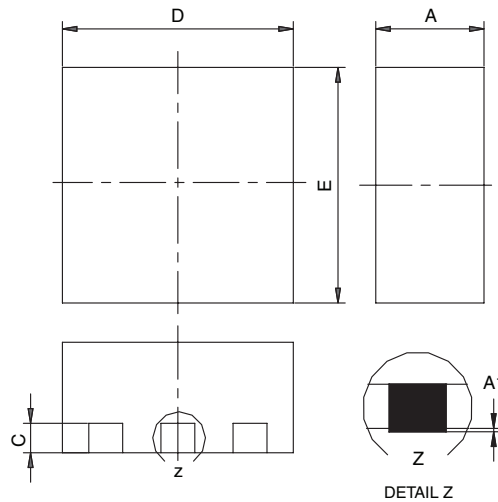
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PowerPAK® SC75-6L



BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



Notes:

1. All dimensions are in millimeters
2. Package outline exclusive of mold flash and metal burr
3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.18	0.25	0.33	0.007	0.010	0.013	0.18	0.25	0.33	0.007	0.010	0.013
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
D1	0.57	0.67	0.77	0.022	0.026	0.030	0.34	0.44	0.54	0.013	0.017	0.021
D2	0.10	0.20	0.30	0.004	0.008	0.012						
E	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
E1	1.00	1.10	1.20	0.039	0.043	0.047	0.51	0.61	0.71	0.020	0.024	0.028
E2	0.20	0.25	0.30	0.008	0.010	0.012						
E3	0.32	0.37	0.42	0.013	0.015	0.017						
e	0.50 BSC			0.020 BSC			0.50 BSC			0.020 BSC		
K	0.180 TYP			0.007 TYP			0.245 TYP			0.010 TYP		
K1	0.275 TYP			0.011 TYP			0.320 TYP			0.013 TYP		
K2	0.200 TYP			0.008 TYP			0.200 BSC			0.008 TYP		
K3	0.255 TYP			0.010 TYP								
K4	0.300 TYP			0.012 TYP								
L	0.15	0.25	0.35	0.006	0.010	0.014	0.15	0.25	0.35	0.006	0.010	0.014
T							0.03	0.08	0.13	0.001	0.003	0.005

ECN: C-07431 - Rev. C, 06-Aug-07

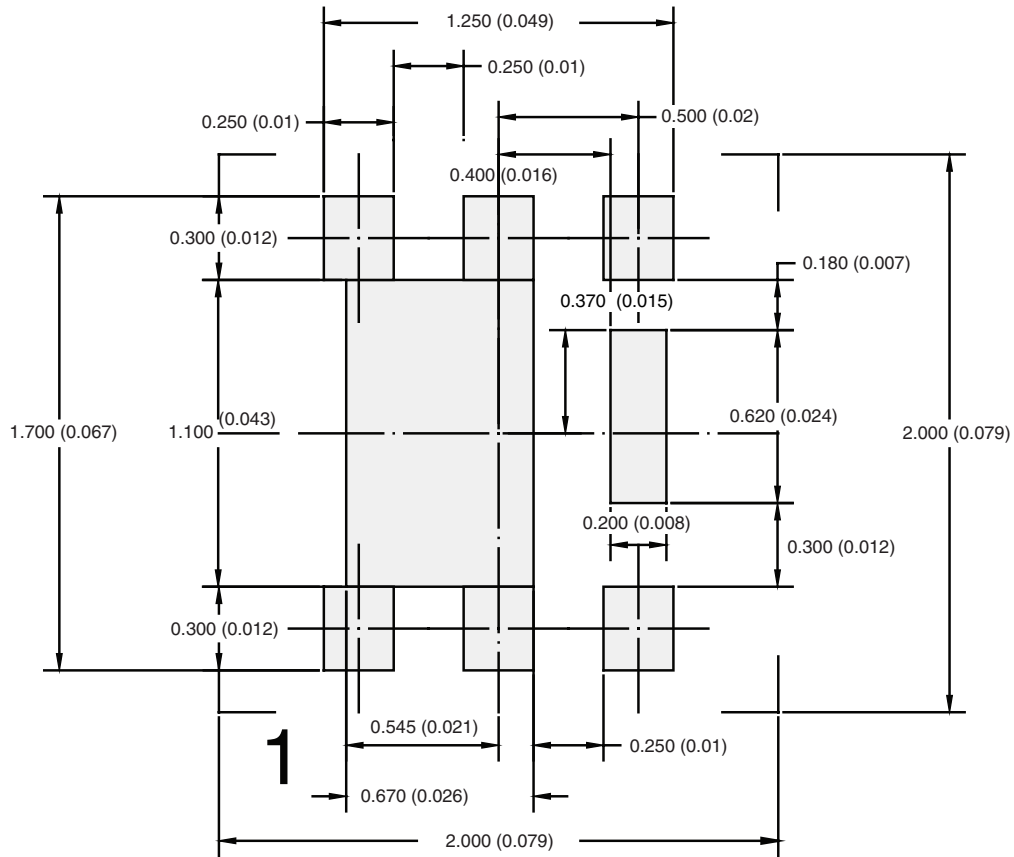
DWG: 5935



Application Note 826

Vishay Siliconix

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC75-6L Single



Dimensions in mm/(Inches)

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