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[Vishay/Siliconix](#)  
[SIS902DN-T1-GE3](#)

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**SiS902DN**  
 Vishay Siliconix

## Dual N-Channel 75-V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)
75	0.186 at V <sub>GS</sub> = 10 V	4 <sup>e</sup>	2.1 nC
	0.228 at V <sub>GS</sub> = 4.5 V	4 <sup>e</sup>	

### FEATURES

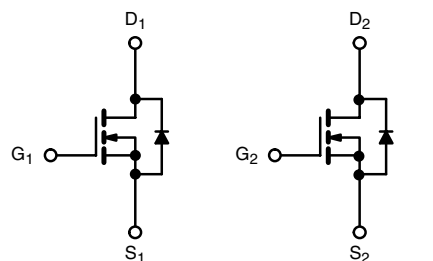
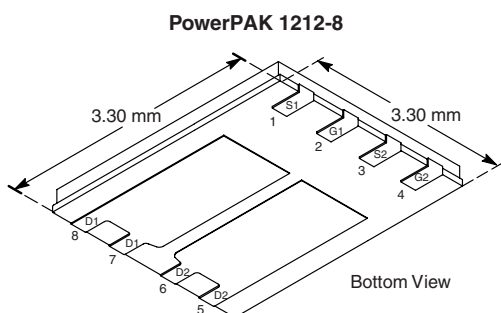
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- Low Thermal Resistance PowerPAK® Package with Small Size and Low 1.07 mm Profile
- 100 % R<sub>g</sub> Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC



**RoHS**  
 COMPLIANT  
 HALOGEN  
 FREE

### APPLICATIONS

- POL



Ordering Information: SiS902DN-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	75	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	A
		T <sub>C</sub> = 70 °C	
		T <sub>A</sub> = 25 °C	
		T <sub>A</sub> = 70 °C	
Pulsed Drain Current	I <sub>DM</sub>	8	
Avalanche Current	I <sub>AS</sub>	2	
Single-Pulse Avalanche Energy	E <sub>AS</sub>	0.2	mJ
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	W
		T <sub>C</sub> = 70 °C	
		T <sub>A</sub> = 25 °C	
		T <sub>A</sub> = 70 °C	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>c, d</sup>		260	

Notes:

- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- See Solder Profile ([www.vishay.com/ppg?73257](http://www.vishay.com/ppg?73257)). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Package limited.

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THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a, b</sup>	$t \leq 10 \text{ s}$	$R_{thJA}$	32	40	°C/W
Maximum Junction-to-Case (Drain)	Steady State	$R_{thJC}$	6.4	8.1	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. Maximum under Steady State conditions is 78 °C/W.

SPECIFICATIONS $T_J = 25 \text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \text{ } \mu\text{A}$	75			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \text{ } \mu\text{A}$		81		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		- 5			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \text{ } \mu\text{A}$	1.2		2.5	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 75 \text{ V}, V_{GS} = 0 \text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 75 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55 \text{ }^\circ\text{C}$			10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 10 \text{ V}$	8			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 3 \text{ A}$		0.155	0.186	$\Omega$
		$V_{GS} = 4.5 \text{ V}, I_D = 2.7 \text{ A}$		0.190	0.228	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15 \text{ V}, I_D = 3 \text{ A}$		10		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 38 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		175		pF
Output Capacitance	$C_{oss}$			30		
Reverse Transfer Capacitance	$C_{rss}$			18		
Total Gate Charge	$Q_g$	$V_{DS} = 38 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 3 \text{ A}$		3.9	6	nC
				2.1	3.2	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 38 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 3 \text{ A}$		0.8		
Gate-Drain Charge	$Q_{gd}$			0.6		
Gate Resistance	$R_g$	$f = 1 \text{ MHz}$	0.4	2	4	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 38 \text{ V}, R_L = 16 \text{ } \Omega$ $I_D \cong 2.4 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \text{ } \Omega$		17	26	ns
Rise Time	$t_r$			18	27	
Turn-Off Delay Time	$t_{d(off)}$			12	20	
Fall Time	$t_f$			9	18	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 38 \text{ V}, R_L = 16 \text{ } \Omega$ $I_D \cong 2.4 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \text{ } \Omega$		5	10	
Rise Time	$t_r$			8	16	
Turn-Off Delay Time	$t_{d(off)}$			10	20	
Fall Time	$t_f$			6	10	



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<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			4	A
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$				8	
Body Diode Voltage	$V_{SD}$	$I_S = 2\text{ A}$		0.85	1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 2.4\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$		20	30	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			17	26	nC
Reverse Recovery Fall Time	$t_a$			15		ns
Reverse Recovery Rise Time	$t_b$			5		

Notes:

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.

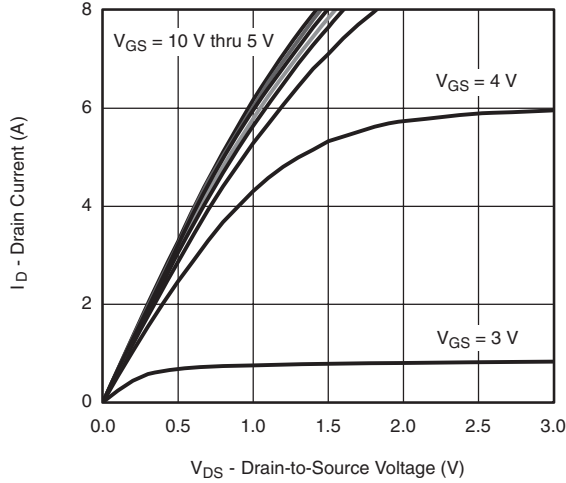
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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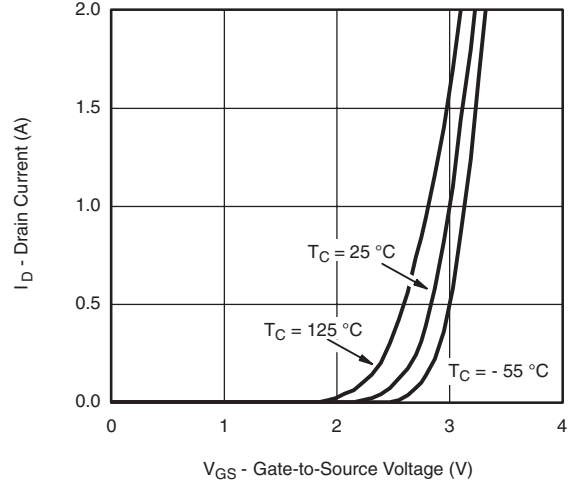
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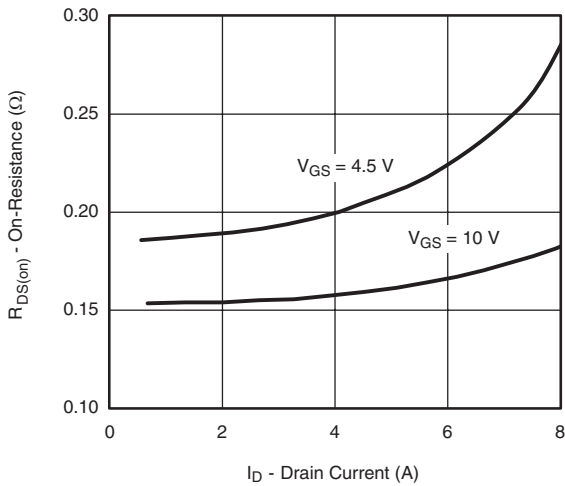
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



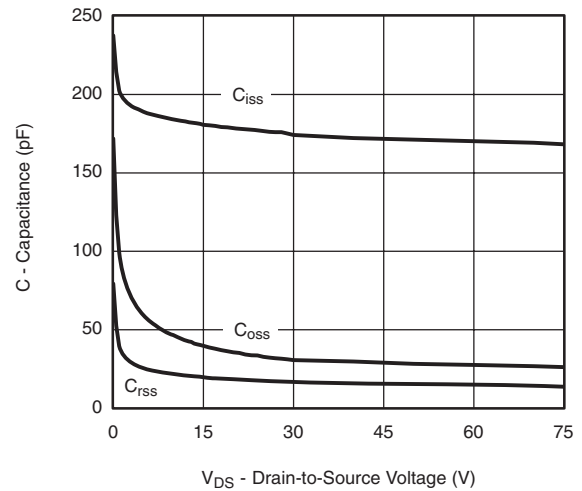
**Output Characteristics**



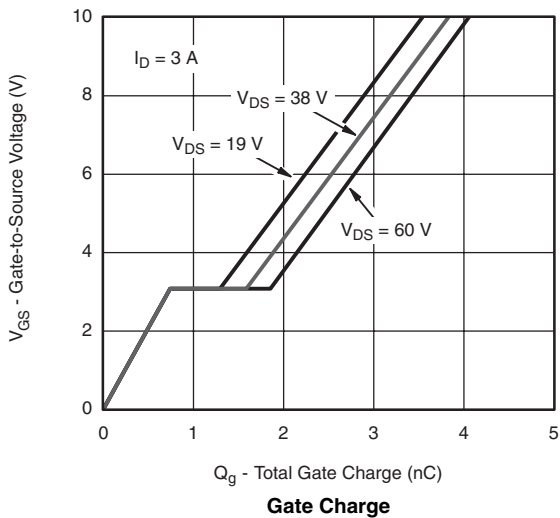
**Transfer Characteristics**



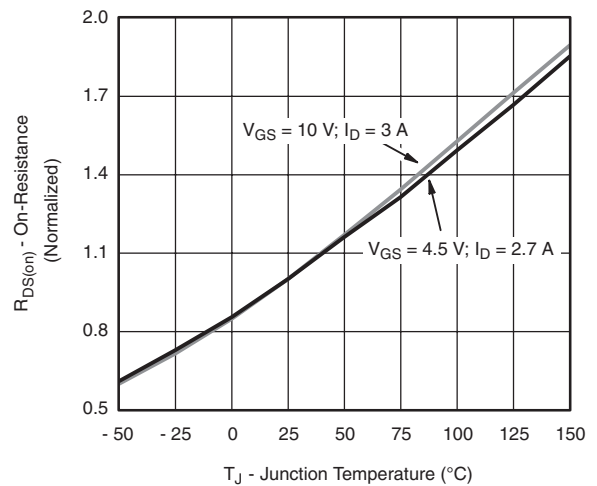
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**



**Gate Charge**

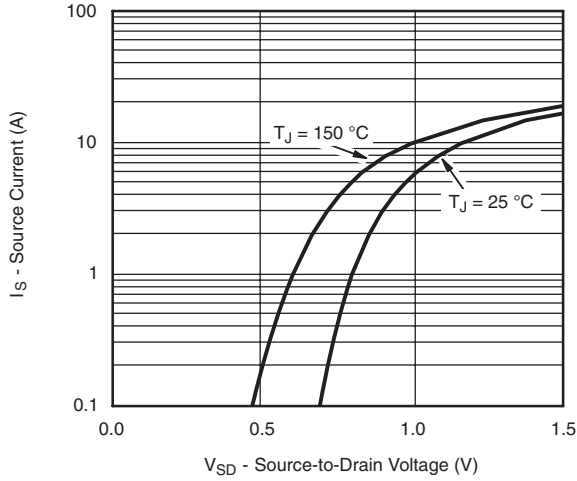


**On-Resistance vs. Junction Temperature**

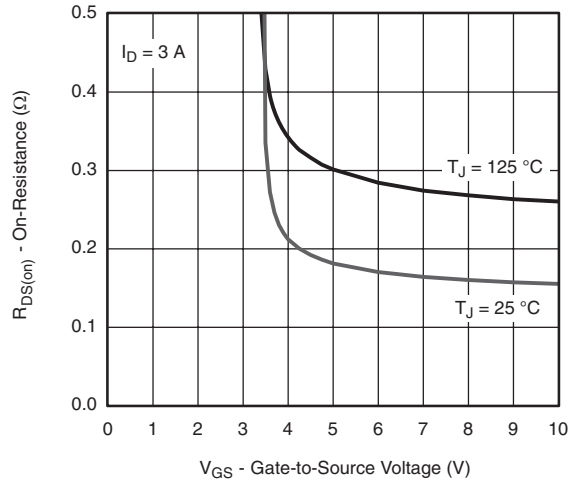


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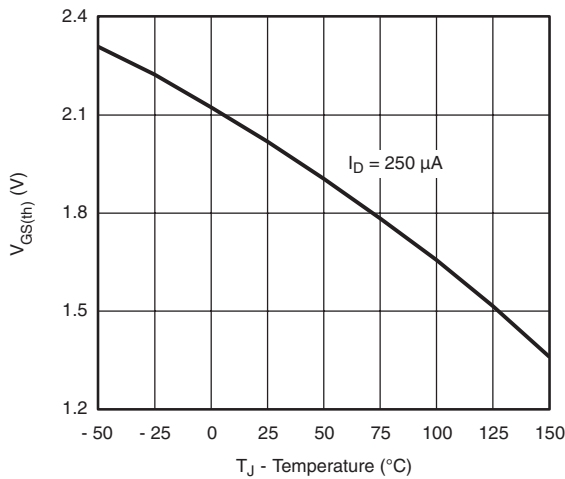
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



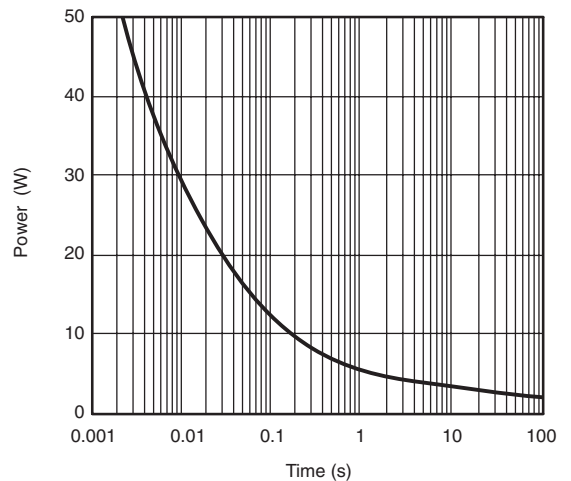
**Source-Drain Diode Forward Voltage**



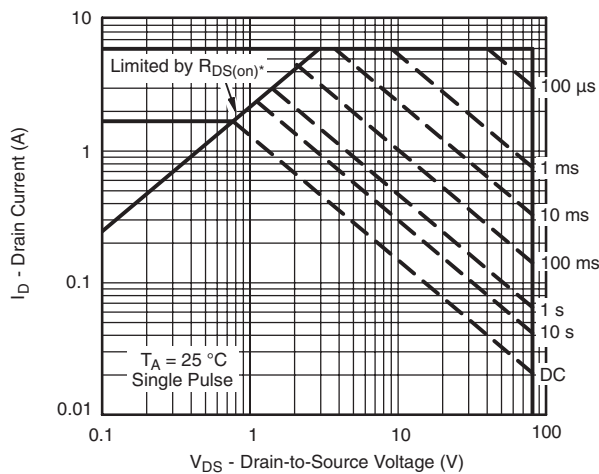
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



**Single Pulse Power, Junction-to-Ambient**



\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

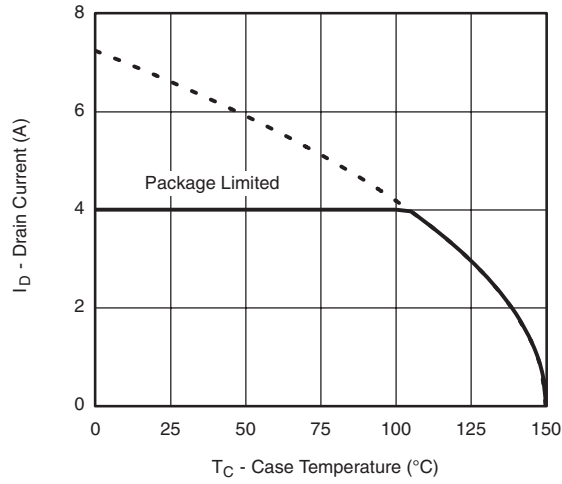
**Safe Operating Area, Junction-to-Ambient**

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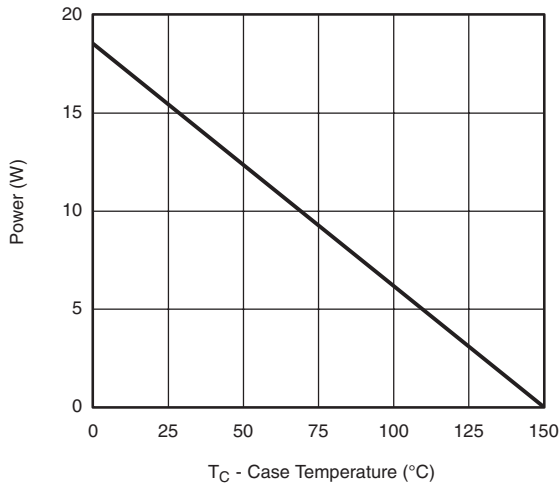
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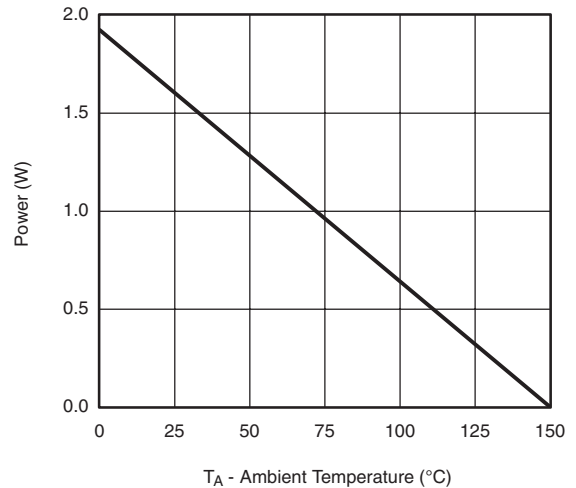
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**Current Derating\***



**Power, Junction-to-Case**



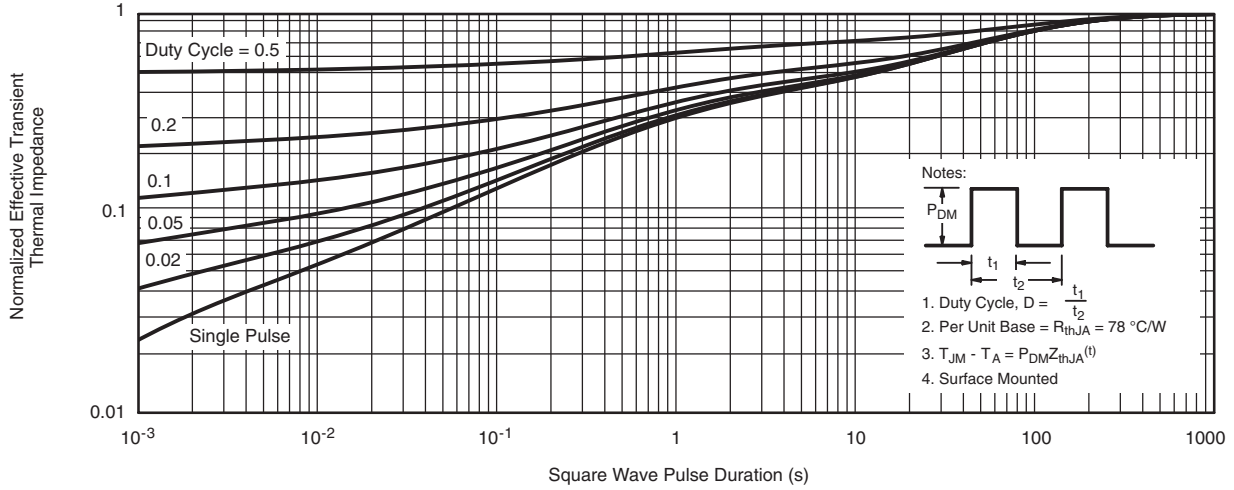
**Power, Junction-to-Ambient**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150\text{ °C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

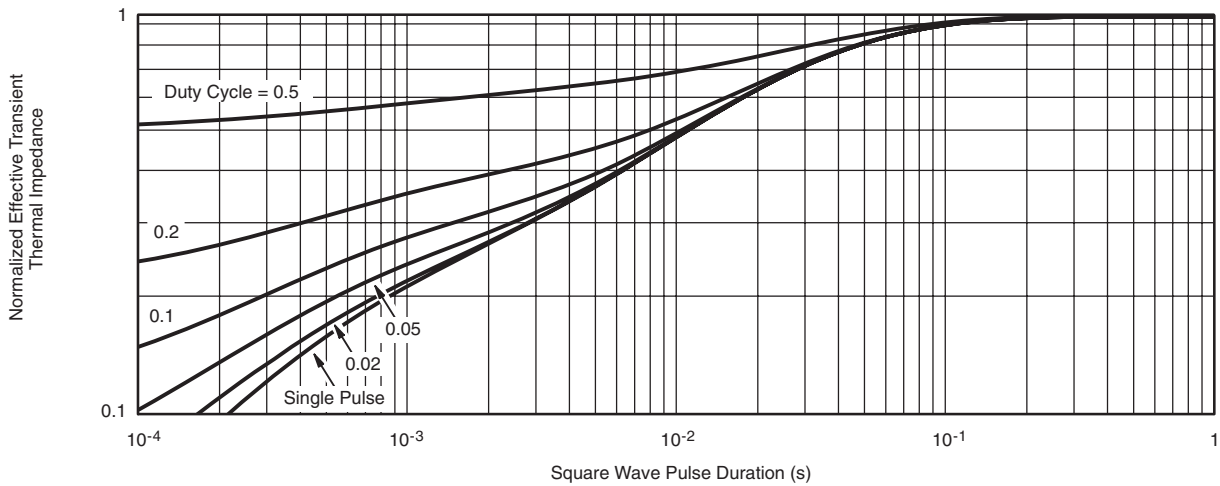


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**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

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