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September 1996

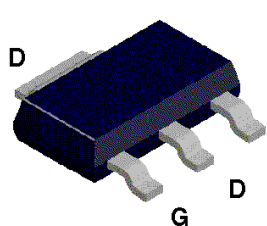
NDT453N N-Channel Enhancement Mode Field Effect Transistor

General Description

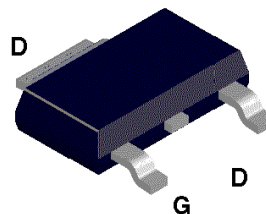
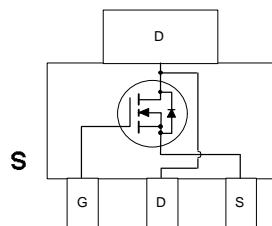
Power SOT N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

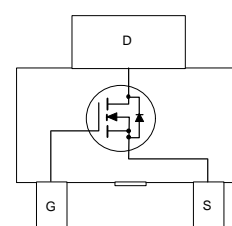
- 8A, 30V. $R_{DS(ON)} = 0.028\Omega$ @ $V_{GS} = 10V$.
 $R_{DS(ON)} = 0.042\Omega$ @ $V_{GS} = 4.5V$.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.



SOT-223



SOT-223*
(J23Z)



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise not

Symbol	Parameter	NDT453N	Units	
V_{DSS}	Drain-Source Voltage	30	V	
V_{GSS}	Gate-Source Voltage	± 20	V	
I_D	Drain Current - Continuous (Note 1a)	± 8	A	
	- Pulsed	± 15		
P_D	Maximum Power Dissipation (Note 1a)	3	W	
		(Note 1b)		1.3
		(Note 1c)		1.1
T_J, T_{STG}	Operating and Storage Temperature Range	-65 to 150	$^\circ\text{C}$	

THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	42	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	12	$^\circ\text{C/W}$

* Order option J23Z for cropped center drain lead.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)							
Symbol	Parameter	Conditions	Min	Typ	Max	Units	
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ $T_J = 55^\circ\text{C}$			1	μA	
					10	μA	
I_{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA	
I_{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA	
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ $T_J = 125^\circ\text{C}$	1	2	3	V	
			0.7	1.5	2.2		
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 8.0\text{ A}$ $T_J = 125^\circ\text{C}$		0.022	0.028	Ω	
			$V_{GS} = 4.5\text{ V}, I_D = 6.7\text{ A}$ $T_J = 125^\circ\text{C}$		0.03		0.045
					0.035		0.042
					0.047		0.075
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$ $V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	15			A	
			10				
g_{FS}	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 8.0\text{ A}$		14		S	
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		890		pF	
C_{oss}	Output Capacitance			560		pF	
C_{rss}	Reverse Transfer Capacitance			190		pF	
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = 25\text{ V}, I_D = 1\text{ A},$ $V_{GEN} = 10\text{ V}, R_{GEN} = 6\ \Omega$		10	15	ns	
t_r	Turn - On Rise Time			20	35	ns	
$t_{D(off)}$	Turn - Off Delay Time			40	50	ns	
t_f	Turn - Off Fall Time			35	50	ns	
Q_g	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 8.0\text{ A}, V_{GS} = 10\text{ V}$		28	35	nC	
Q_{gs}	Gate-Source Charge			4.5		nC	
Q_{gd}	Gate-Drain Charge			9.5		nC	

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				2.3	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 8.0\text{ A}$ (Note 2)		0.8	1.3	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 2\text{ A}, di_F/dt = 100\text{ A}/\mu\text{s}$			100	ns

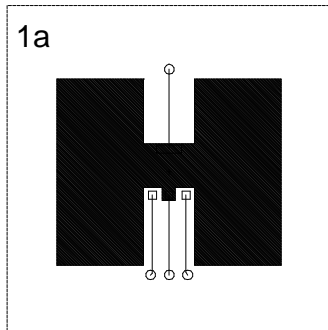
Notes:

- $R_{\theta_{jca}}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta_{jca}}$ is guaranteed by design while $R_{\theta_{jc}}$ is determined by the user's board design.

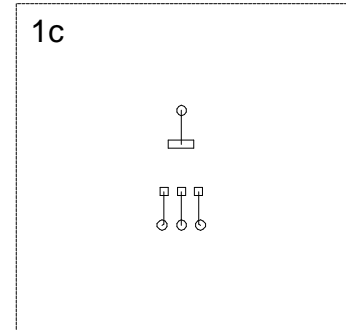
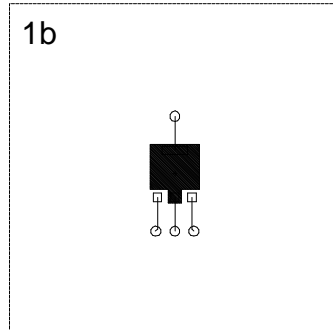
$$P_D(t) = \frac{T_j - T_A}{R_{\theta_{jA}}} = \frac{T_j - T_A}{R_{\theta_{jC}} + R_{\theta_{cA}}} = I_D^2(t) \times R_{DS(on)} \theta_{TJ}$$

Typical $R_{\theta_{jca}}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- 42°C/W when mounted on a 1 in² pad of 2oz copper.
- 95°C/W when mounted on a 0.066 in² pad of 2oz copper.
- 110°C/W when mounted on a 0.0123 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper



- Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

Typical Electrical Characteristics

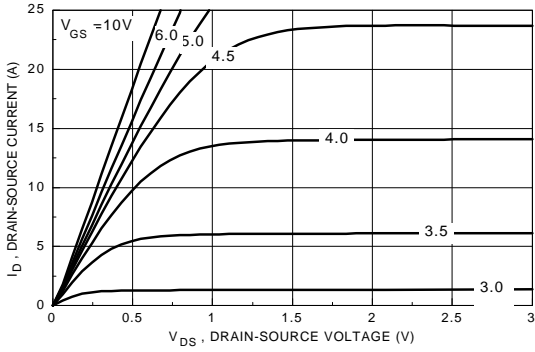


Figure 1. On-Region Characteristics.

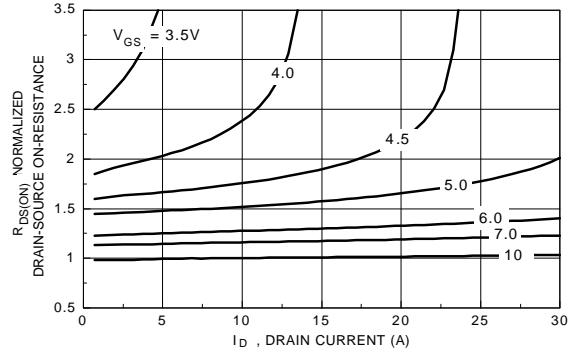


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

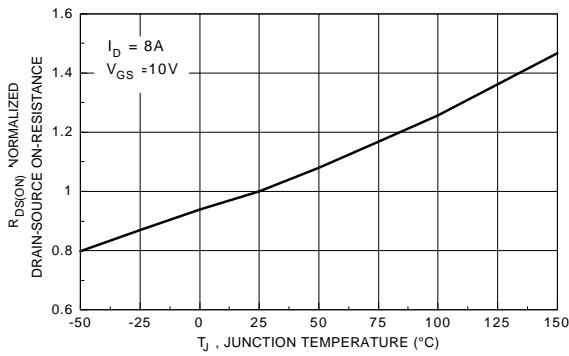


Figure 3. On-Resistance Variation with Temperature.

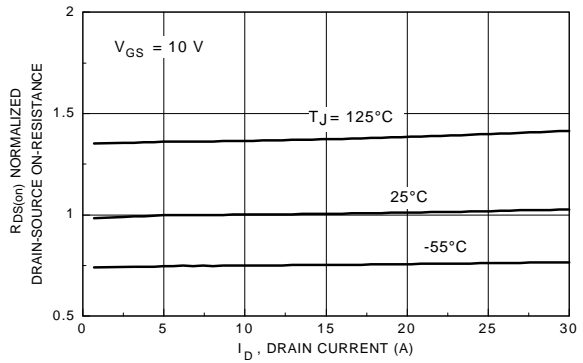


Figure 4. On-Resistance Variation with Drain Current and Temperature.

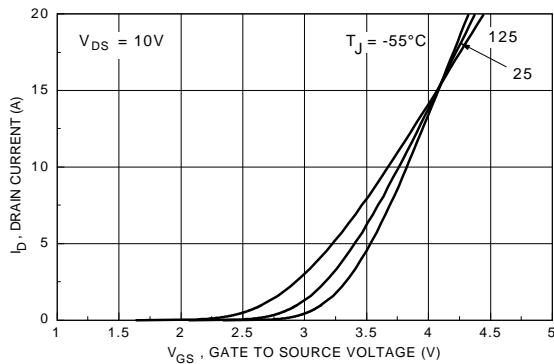


Figure 5. Transfer Characteristics.

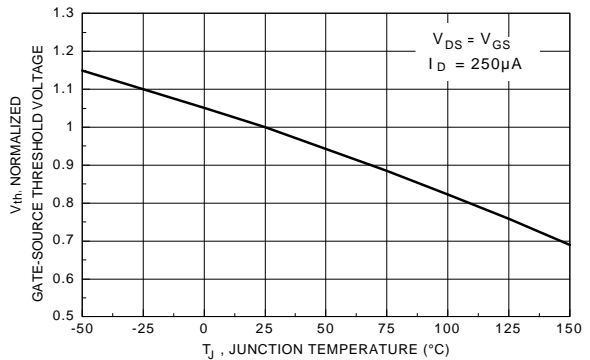


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

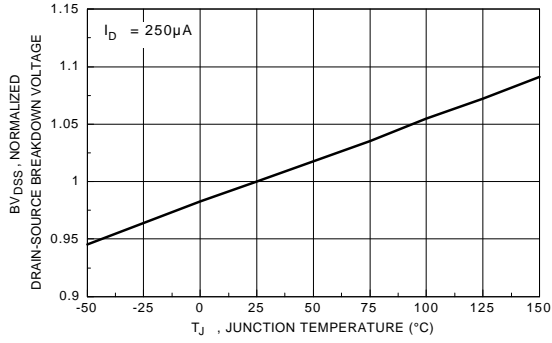


Figure 7. Breakdown Voltage Variation with Temperature.

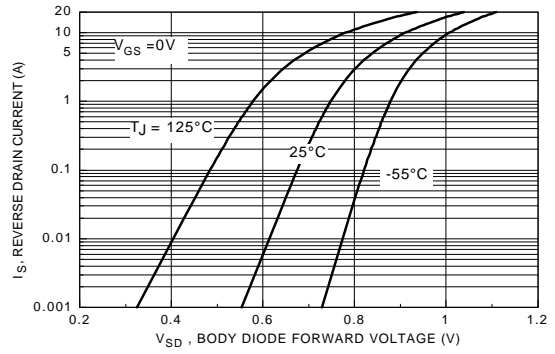


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

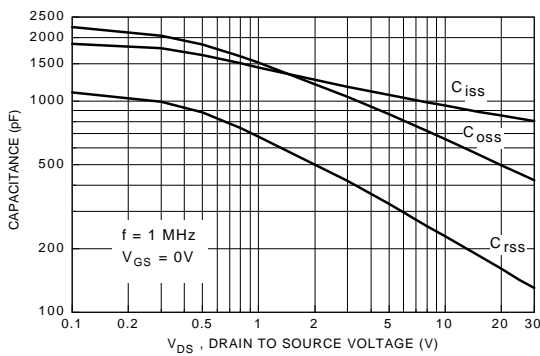


Figure 9. Capacitance Characteristics.

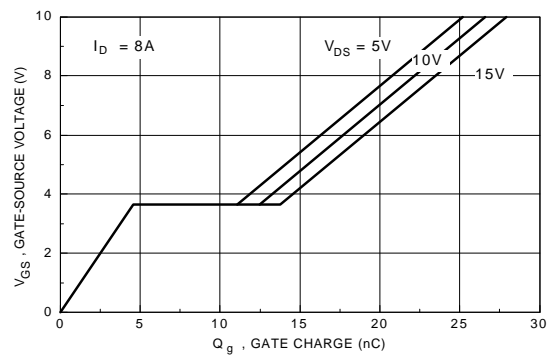


Figure 10. Gate Charge Characteristics.

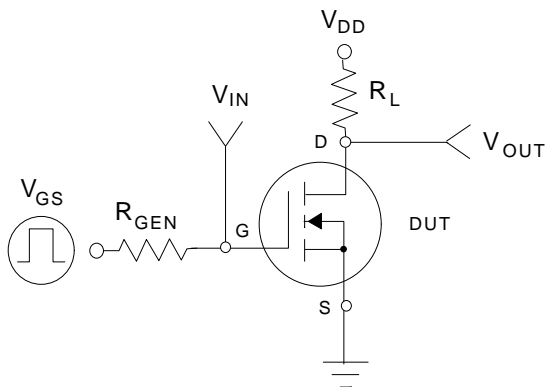


Figure 11. Switching Test Circuit.

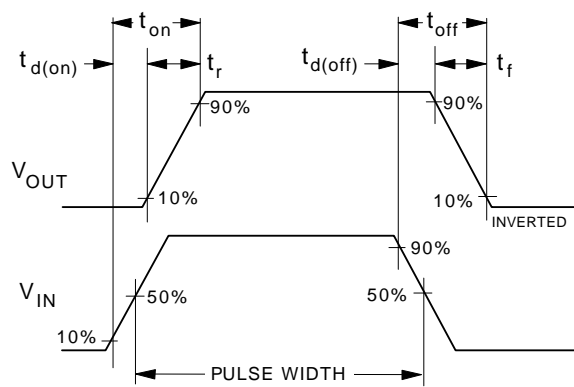


Figure 12. Switching Waveforms.

Typical Electrical and Thermal Characteristics

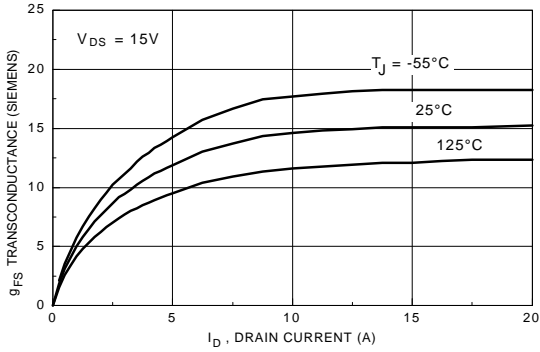


Figure 13. Transconductance Variation with Drain Current and Temperature.

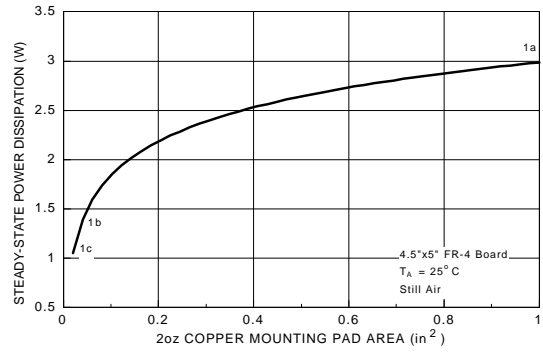


Figure 14. SOT-223 Maximum Steady- State Power Dissipation versus Copper Mounting Pad Area.

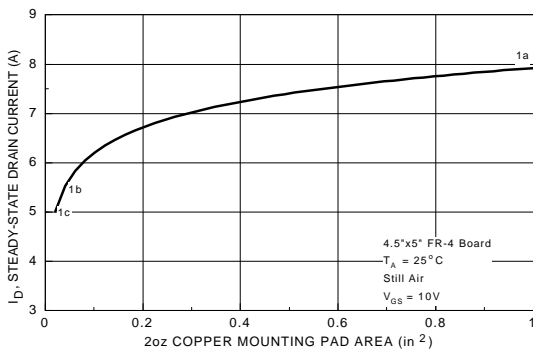


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

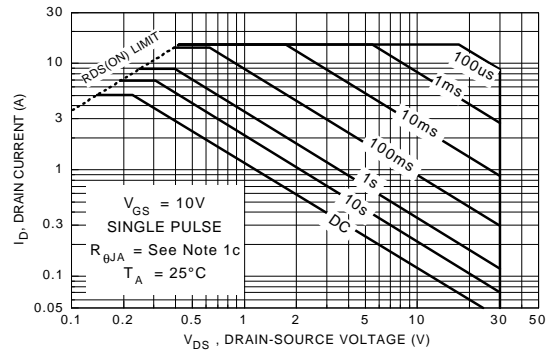


Figure 16. Maximum Safe Operating Area.

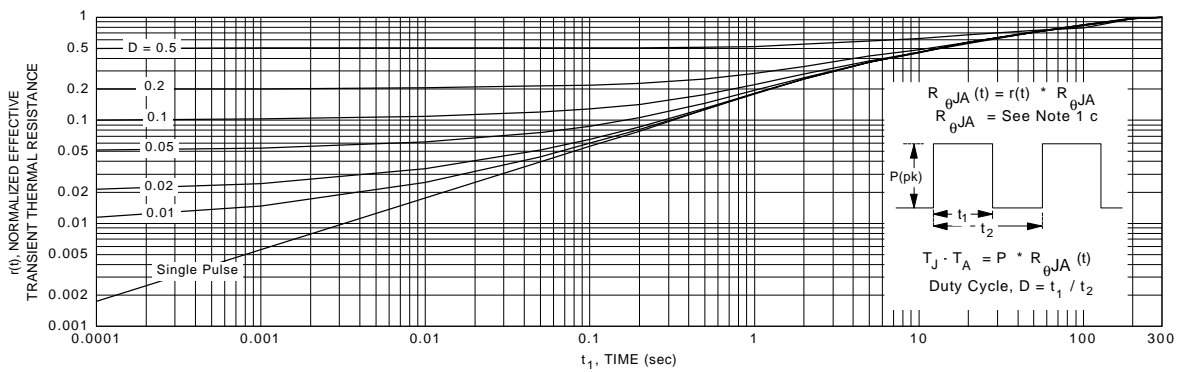


Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

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