

Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

[ON Semiconductor](#)
[NTLUS3A90PZTAG](#)

For any questions, you can email us directly:

sales@integrated-circuit.com

NTLUS3A90PZ

Power MOSFET

-20 V, -5.0 A, μ Cool™ Single P-Channel, ESD, 1.6x1.6x0.55 mm UDFN Package

Features

- UDFN Package with Exposed Drain Pads for Excellent Thermal Conduction
- Low Profile UDFN 1.6x1.6x0.55 mm for Board Space Saving
- Lowest RDS(on) in 1.6x1.6 Package
- ESD Protected
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- High Side Load Switch
- PA Switch and Battery Switch
- Optimized for Power Management Applications for Portable Products, such as Cell Phones, PMP, DSC, GPS, and others

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter		Symbol	Value	Units	
Drain-to-Source Voltage		V _{DSS}	-20	V	
Gate-to-Source Voltage		V _{GS}	±8.0	V	
Continuous Drain Current (Note 1)	Steady State	I _D	T _A = 25°C	-4.0	A
			T _A = 85°C	-2.9	
	t ≤ 5 s	T _A = 25°C	-5.0		
Power Dissipation (Note 1)	Steady State	P _D	T _A = 25°C	1.5	W
			t ≤ 5 s	T _A = 25°C	
Continuous Drain Current (Note 2)	Steady State	I _D	T _A = 25°C	-2.6	A
			T _A = 85°C	-1.9	
Power Dissipation (Note 2)		P _D	T _A = 25°C	0.6	W
Pulsed Drain Current		I _{DM}	t _p = 10 μs	-17	A
Operating Junction and Storage Temperature		T _J , T _{STG}	-55 to 150	°C	
Source Current (Body Diode) (Note 2)		I _S	-0.84	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T _L	260	°C	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm², 2 oz. Cu.

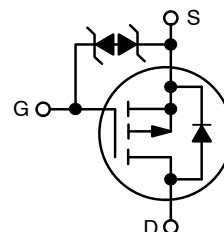


ON Semiconductor®

<http://onsemi.com>

MOSFET

V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX
-20 V	62 mΩ @ -4.5 V	-5.0 A
	95 mΩ @ -2.5 V	
	140 mΩ @ -1.8 V	
	230 mΩ @ -1.5 V	

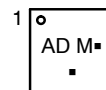


P-Channel MOSFET



UDFN6
CASE 517AU
 μ COOL™

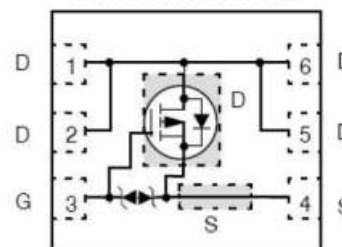
MARKING DIAGRAM



AD = Specific Device Code
 M = Date Code
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTLUS3A90PZ

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Units
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	84	°C/W
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	55	
Junction-to-Ambient – Steady State min Pad (Note 4)	$R_{\theta JA}$	200	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
-----------	--------	----------------	-----	-----	-----	-------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = -250$ μ A	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -250$ μ A, ref to 25°C		-8.0		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0$ V, $V_{DS} = -20$ V			-1.0	μ A
		$T_J = 25^\circ\text{C}$ $T_J = 85^\circ\text{C}$			-10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 8.0$ V			± 10	μ A

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = -250$ μ A	-0.4		-1.0	V
Negative Threshold Temp. Coefficient	$V_{GS(TH)}/T_J$			3.0		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -4.5$ V, $I_D = -4.0$ A		54	62	m Ω
		$V_{GS} = -2.5$ V, $I_D = -2.0$ A		74	95	
		$V_{GS} = -1.8$ V, $I_D = -1.2$ A		104	140	
		$V_{GS} = -1.5$ V, $I_D = -0.5$ A		137	230	
Forward Transconductance	g_{FS}	$V_{DS} = -10$ V, $I_D = -3.0$ A		10		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0$ V, $f = 1$ MHz, $V_{DS} = -10$ V		950		pF
Output Capacitance	C_{OSS}			90		
Reverse Transfer Capacitance	C_{RSS}			85		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5$ V, $V_{DS} = -10$ V; $I_D = -3.0$ A		12.3		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.9		
Gate-to-Source Charge	Q_{GS}			1.6		
Gate-to-Drain Charge	Q_{GD}			3.3		

SWITCHING CHARACTERISTICS, $V_{GS} = 4.5$ V (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -4.5$ V, $V_{DD} = -10$ V, $I_D = -3.0$ A, $R_G = 1$ Ω		7.9		ns
Rise Time	t_r			15.7		
Turn-Off Delay Time	$t_{d(OFF)}$			34.8		
Fall Time	t_f			28.5		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	VSD	$V_{GS} = 0$ V, $I_S = -1.0$ A	$T_J = 25^\circ\text{C}$		0.74	1.2	V
			$T_J = 125^\circ\text{C}$		0.62		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0$ V, $dis/dt = 100$ A/ μ s, $I_S = -1.0$ A			11.8		ns
Charge Time	t_a				8.5		
Discharge Time	t_b				3.3		
Reverse Recovery Charge	Q_{RR}				6.0		nC

- Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
- Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm², 2 oz. Cu.
- Pulse Test: pulse width ≤ 300 μ s, duty cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

NTLUS3A90PZ

TYPICAL CHARACTERISTICS

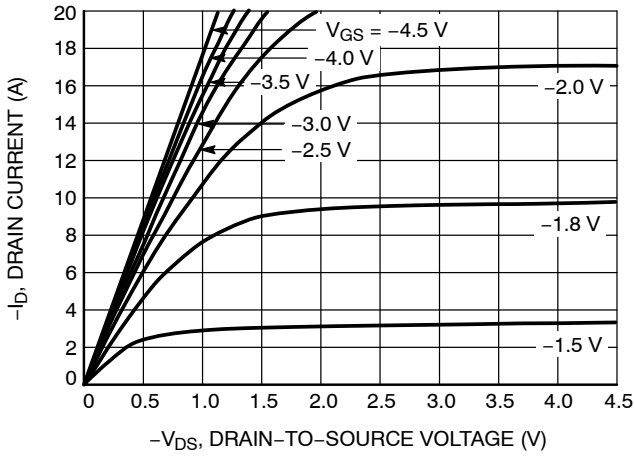


Figure 1. On-Region Characteristics

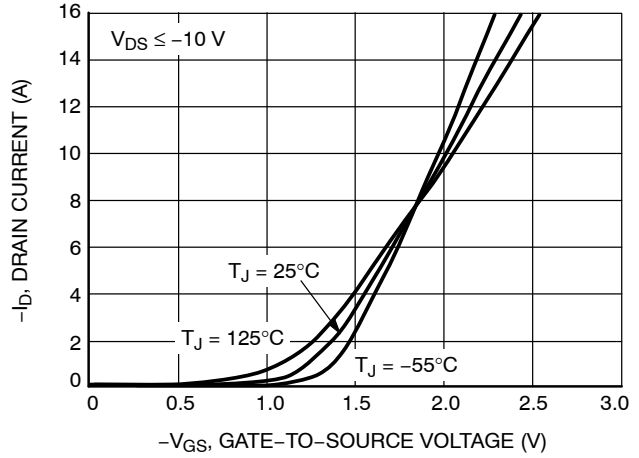


Figure 2. Transfer Characteristics

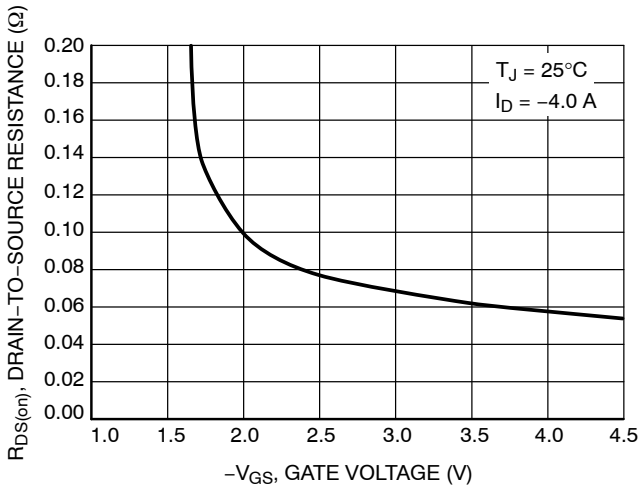


Figure 3. On-Resistance vs. Gate-to-Source Voltage

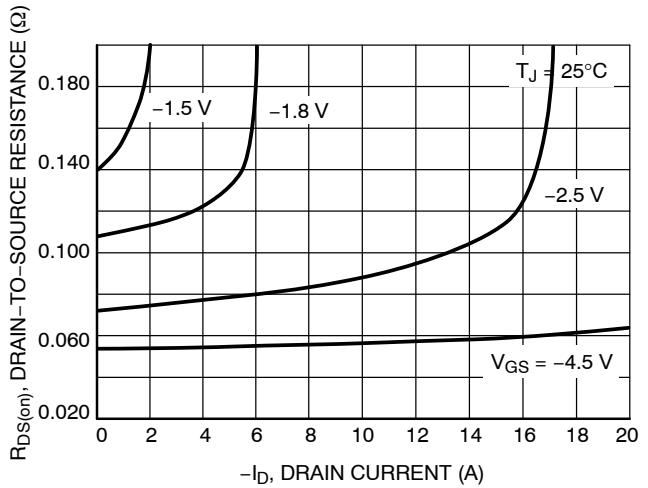


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

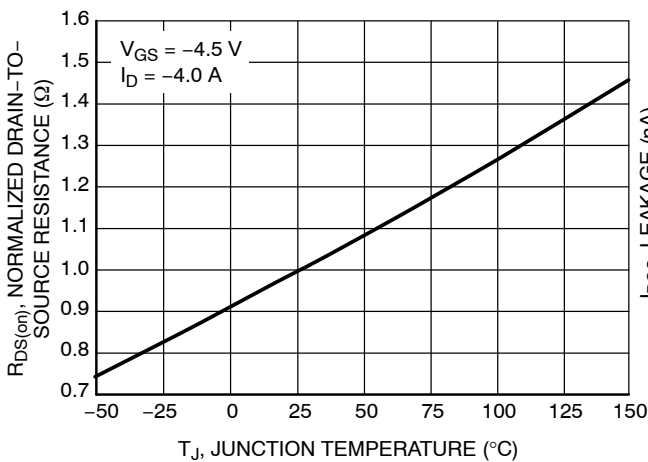


Figure 5. On-Resistance Variation with Temperature

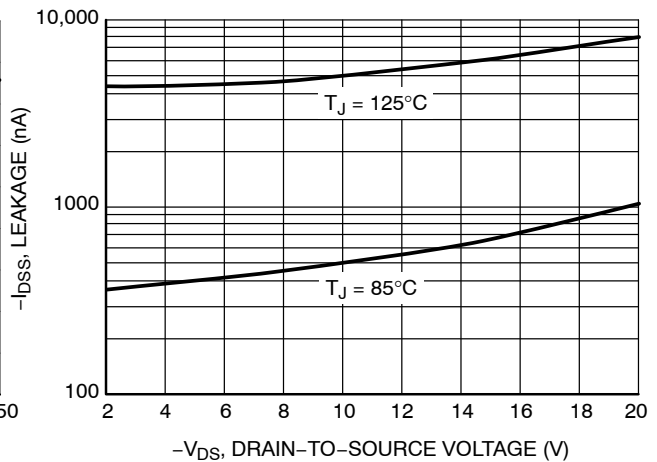


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NTLUS3A90PZ

TYPICAL CHARACTERISTICS

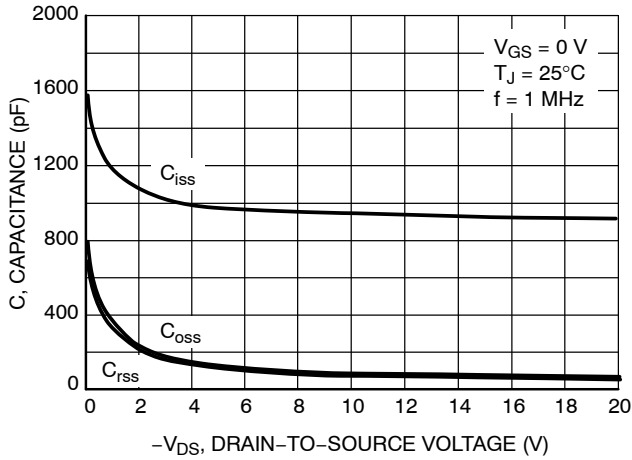


Figure 7. Capacitance Variation

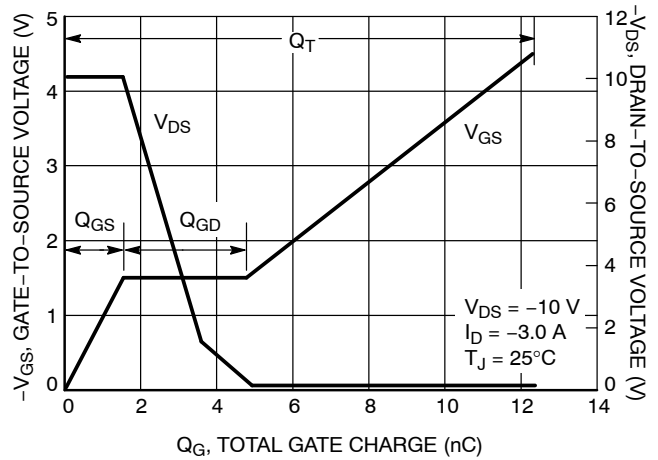


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

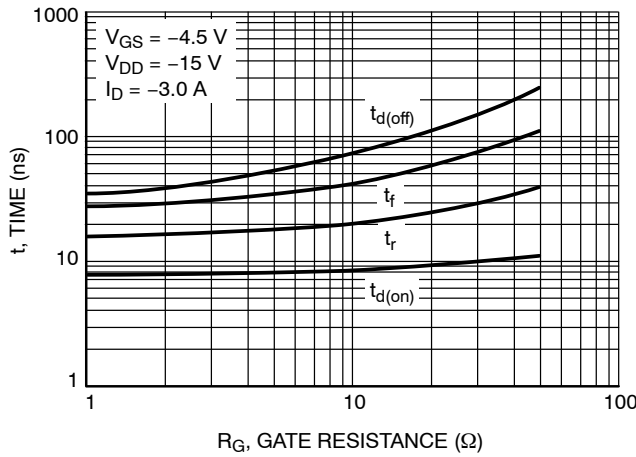


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

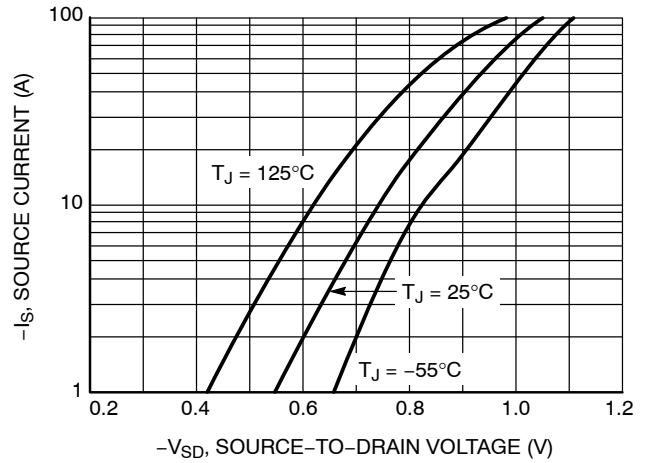


Figure 10. Diode Forward Voltage vs. Current

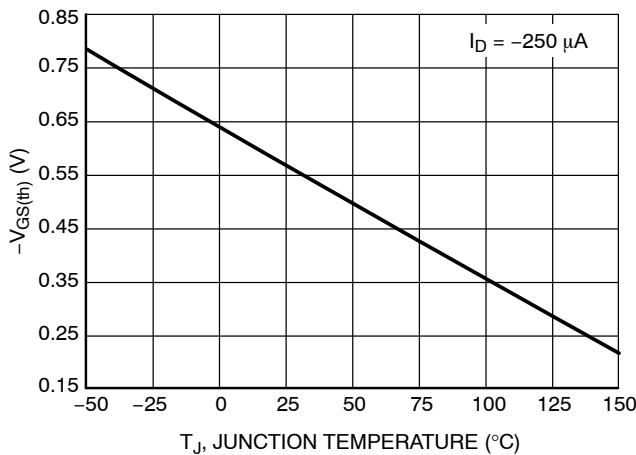


Figure 11. Threshold Voltage

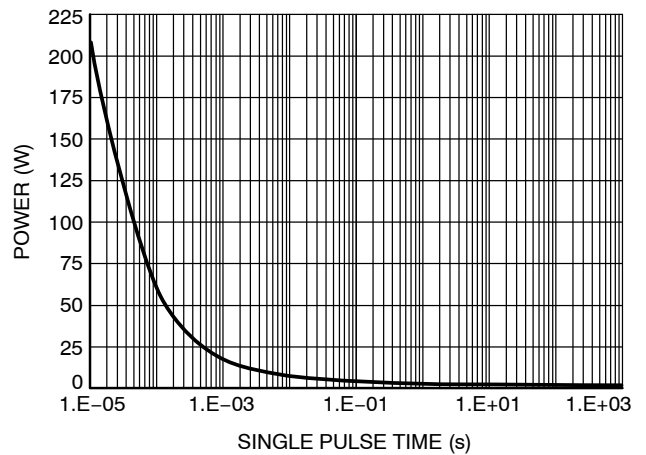


Figure 12. Single Pulse Maximum Power Dissipation

NTLUS3A90PZ

TYPICAL CHARACTERISTICS

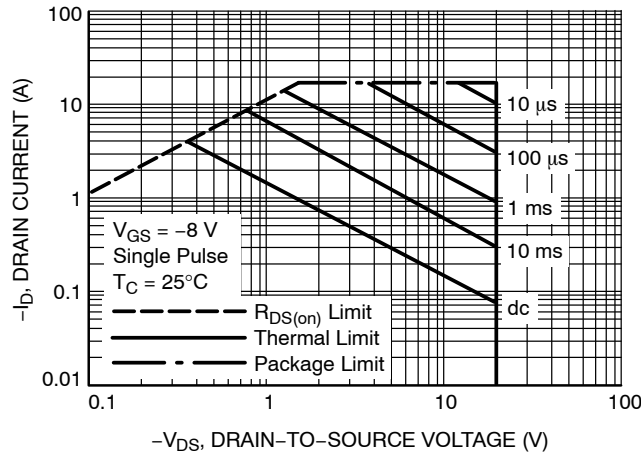


Figure 13. Maximum Rated Forward Biased Safe Operating Area

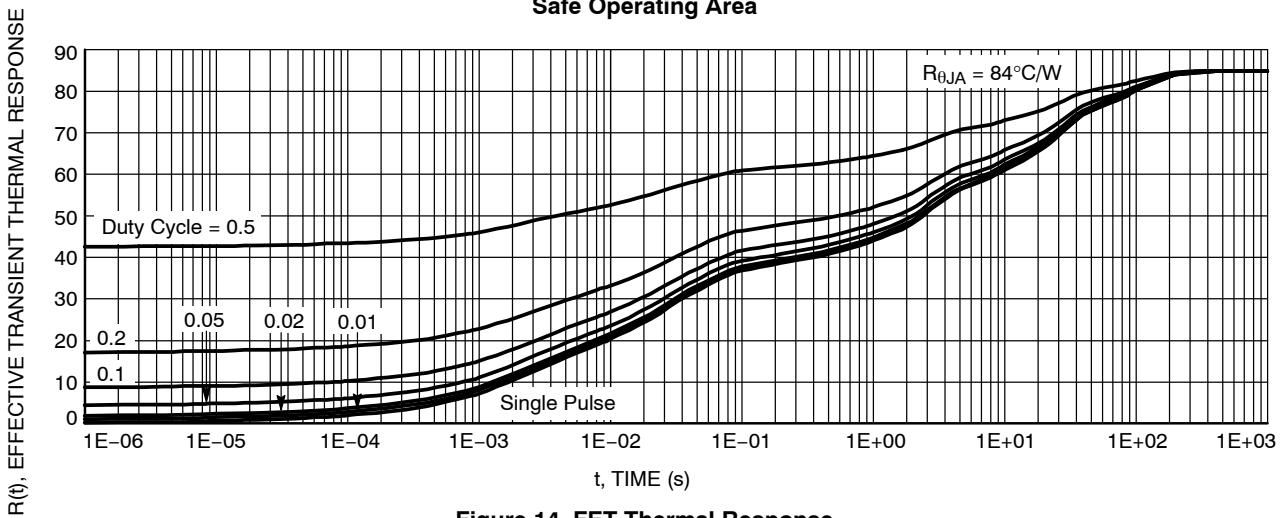


Figure 14. FET Thermal Response

DEVICE ORDERING INFORMATION

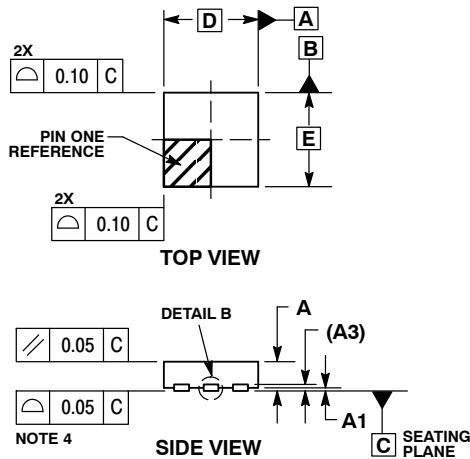
Device	Package	Shipping [†]
NTLUS3A90PZTAG	UDFN6 (Pb-Free)	3000 / Tape & Reel
NTLUS3A90PZTBG	UDFN6 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTLUS3A90PZ

PACKAGE DIMENSIONS

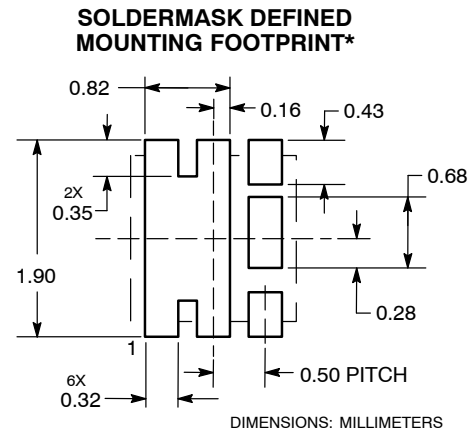
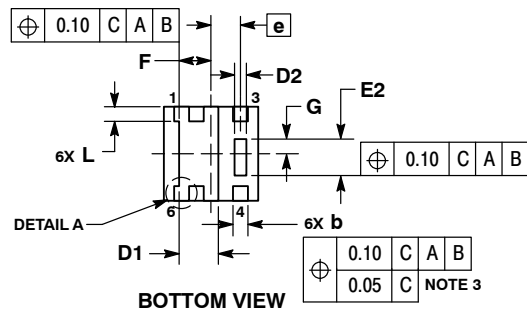
UDFN6 1.6x1.6, 0.5P
 CASE 517AU-01
 ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.20	0.30
D	1.60	BSC
E	1.60	BSC
e	0.50	BSC
D1	0.62	0.72
D2	0.15	0.25
E2	0.57	0.67
F	0.55	BSC
G	0.25	BSC
L	0.20	0.30
L1	---	0.15



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

µCool is a trademark of Semiconductor Components Industries, LLC (SCILLC).

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
 P.O. Box 5163, Denver, Colorado 80217 USA
 Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
 Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
 Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

Europe, Middle East and Africa Technical Support: Phone: 421 33 790 2910

Japan Customer Focus Center Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative