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OPA132U

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OPAx132 High-Speed FET-Input Operational Amplifiers

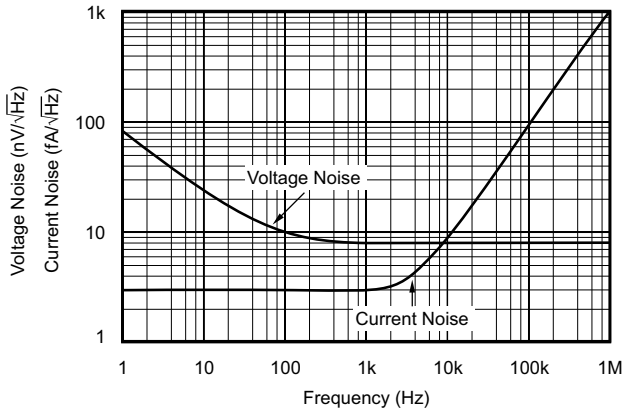
1 Features

- FET input: I_B = 50 pA Maximum
- Wide Bandwidth: 8 MHz
- High Slew Rate: 20 V/µs
- Low Noise: 8nV/√Hz (1 kHz)
- Low Distortion: 0.00008%)
- High Open-loop Gain: 130 dB (600-Ω load)
- Wide Supply Range: ±2.5 to ±18V
- Low Offset Voltage: 500 µV Maximum
- Single, Dual, and Quad Versions

2 Applications

- SAR ADC Driver
- Voltage Reference Buffer
- Trans-impedance Amplifier
- Photodiode Amplifier
- Active Filters
- Integrators

Low Noise JFET Input



3 Description

The OPAx132 series of FET-input operational amplifiers provides highspeed and excellent DC performance. The combination of high slew rate and wide bandwidth provide fast settling time. Single, dual, and quad versions have identical specifications for maximum design flexibility. High performance grades are available in the single and dual versions. All are ideal for general-purpose, audio, data acquisition and communications applications, especially where high source impedance is encountered.

The OPAx132 operational amplifiers are easy to use and free from phase inversion and overload problems often found in common FET-input operational amplifiers. Input cascode circuitry provides excellent common-mode rejection and maintains low input bias current over its wide input voltage range. The OPAx132 series of operational amplifiers are stable in unity gain and provide excellent dynamic behavior over a wide range of load conditions, including high load capacitance. Dual and quad versions feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

Single and dual versions are available in 8-pin DIP and SO-8 surface-mount packages. Quad is available in 14-pin DIP and SO-14 surface-mount packages. All are specified for –40°C to 85°C operation

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPAx132	PDIP (8) (P)	9.81 mm × 6.35 mm
	SOIC (8) (D)	4.90 mm × 3.91 mm
OPA2132	PDIP (8) (P)	9.81 mm × 6.35 mm
	SOIC (8) (D)	4.90 mm × 3.91 mm
OPA4132	PDIP (14) (N)	19.30 mm × 6.35 mm
	SOIC (14) (D)	8.65 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2004) to Revision B	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

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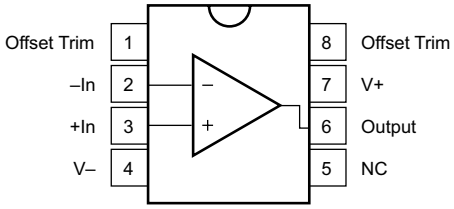
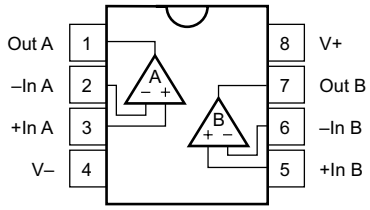
5 Pin Configuration and Functions

OPA132: P and D Packages
8-Pin PDIP and 8-Pin SOIC
Top View



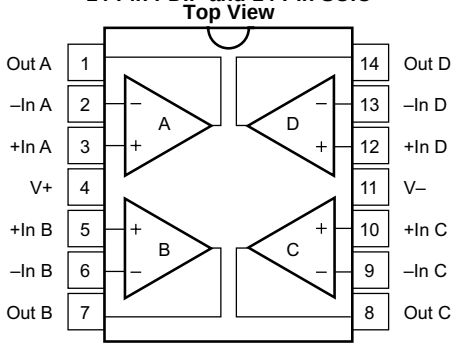
8-Pin DIP, SO-8

OPA2132: P and D Packages
8-Pin PDIP and 8-Pin SOIC
Top View



8-Pin DIP, SO-8

OPA4132: P and D Packages
14-Pin PDIP and 14-Pin SOIC
Top View



14-Pin DIP
SO-14

Pin Functions OPA132

PIN		I/O	DESCRIPTION
NAME	NO.		
Offset Trim	1	I	Input offset voltage adjust
–In	2	I	Inverting input
+In	3	I	Noninverting input
V–	4	—	Negative power supply
NC	5	—	No internal connection. Can be left floating.
Output	6	O	Output
V+	7	—	Positive power supply
Offset Trim	8	I	Input offset voltage adjust

Pin Functions OPA2132 and OPA4132

PIN			I/O	DESCRIPTION
NAME	OPA2132 NO.	OPA4132 NO.		
Out A	1	1	O	Output channel A
–In A	2	2	I	Inverting input channel A
+In A	3	3	I	Noninverting input channel A
V+	8	4	—	Positive power supply
+In B	5	5	I	Noninverting input channel B
–In B	6	6	I	Inverting input channel B
Out B	7	7	O	Output channel B
Out C	–	8	O	Output channel C
–In C	–	9	I	Inverting input channel C

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Pin Functions OPA2132 and OPA4132 (continued)

PIN			I/O	DESCRIPTION
NAME	OPA2132 NO.	OPA4132 NO.		
+In C	–	10	I	Noninverting input channel C
V–	4	11	—	Negative power supply
+In D	–	12	I	Noninverting input channel D
–In D	–	13	I	Inverting input channel D
Out D	–	14	O	Output channel D

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
	Supply voltage, V+ to V–		36	V
	Input voltage	(V–) –0.7	(V+) +0.7	V
	Output short-circuit (2)	Continuous		
	Operation temperature	–40	125	°C
	Junction temperature		150	°C
T_{stg}	Storage temperature	–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
OPA132 in PDIP and SOIC Package, OPA2132 and OPA4132 in PDIP Package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
OPA2132 in SOIC Package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	
OPA4132 in SOIC Package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VS	Supply voltage, VS = (V+) – (V–)	±2.5	±15	±18	V
T_A	Specified temperature range	–40		85	°C

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6.4 Electrical Characteristics

At T_A = 25°C, V_S = ±15 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS		OPAx132P, U OPA2132P, U			OPAx132PA, UA OPA2132PA, UA OPA4132PA, UA			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE										
Input Offset Voltage					±0.25	±0.5		±0.5	±2	mV
vs Temperature(1)		Operating temperature range			±2	±10		±2	±10	µV/°C
vs Power Supply		V_S = ±2.5 V to ±18 V			5	15		5	30	µV/V
Channel Separation (dual and quad)		R_L = 2 kΩ			0.2			0.2		µV/V
INPUT BIAS CURRENT										
Input Bias Current(2)		V_{CM} = 0 V			5	±50		5	±50	pA
vs Temperature					See Figure 5			See Figure 5		
Input Offset Current(2)		V_{CM} = 0 V			±2	±50		±2	±50	pA
NOISE										
Input Voltage Noise										
Noise Density	f = 10 Hz				23			23		nV/√Hz
	f = 100 H				10			10		
	f = 1 kHz				8			8		
	f = 10 kHz				8			8		
Current Noise Density,	f = 1 kHz				3			3		fA/√Hz
INPUT VOLTAGE RANGE										
Common-Mode Voltage Range				(V–) +2.5	±13	(V+) –2.5	(V–) +2.5	±13	(V+) –2.5	V
Common-Mode Rejection		V_{CM} = –12.5 V to 12.5 V		96	100		86	94		dB
INPUT IMPEDANCE										
Differential					10^{13} || 2			10^{13} || 2		Ω || pF
Common-Mode		V_{CM} = –12.5 V to 12.5 V			10^{13} || 6			10^{13} || 6		Ω || pF
OPEN-LOOP GAIN										
Open-Loop Voltage Gain		R_L = 10 kΩ, V_O = –14.5 V to 13.8 V		110	120		104	120		dB
		R_L = 2 kΩ, V_O = –13.8 V to 13.5 V		110	126		104	120		
		R_L = 600 Ω, V_O = –12.8 V to 12.5 V		110	130		104	120		
FREQUENCY RESPONSE										
Gain-Bandwidth Product					8			8		MHz
Slew Rate					±20			±20		V/µs
Settling Time:	0.1%	G = –1, 10 V Step, CL = 100 pF			0.7			0.7		µs
	0.01%	G = –1, 10 V Step, C_L = 100 pF			1			1		µs
Overload Recovery Time		G = ±			0.5			0.5		µs
Total Harmonic Distortion + Noise		1 kHz, G = 1, V_O = 3.5 Vrms	R_L = 2 kΩ		0.00008%			0.00008%		
			R_L = 600 Ω		0.00009%			0.00009%		

(1) Specified by wafer test.
(2) High-speed test at T_J = 25°C.

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Electrical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPAx132P, U OPA2132P, U			OPAx132PA, UA OPA2132PA, UA OPA4132PA, UA			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT									
Voltage Output	Positive	R_L = 10 kΩ	(V+) –1.2	(V+) –0.9		(V+) –1.2	(V+) –0.9		V
	Negative		(V–) +0.5	(V–) +0.3		(V–) +0.5	(V–) +0.3		
	Positive	R_L= 2 kΩ	(V+) –1.5	(V+) –1.1		(V+) –1.5	(V+) –1.1		
	Negative		(V–) +1.2	(V–) +0.9		(V–) +1.2	(V–) +0.9		
	Positive	R_L = 600 Ω	(V+) –2.5	(V+) –2.0		(V+) –2.5	(V+) –2.0		
	Negative		(V–) +2.2	(V–) +1.5		(V–) +2.2	(V–) +1.5		
Short-Circuit Current				±40			±40		mA
Capacitive Load Drive (Stable Operation)				See Figure 17			See Figure 17		
POWER SUPPLY									
Specified Operating Voltage				±15			±15		V
Operating Voltage Range			±2.5		±18	±2.5		±18	V
Quiescent Current (per amplifier)		I_O = 0		±4	±4.8		±4	±4.8	mA
TEMPERATURE RANGE									
Operating Range			–40		85	–40		85	°C
Storage			–40		125	–40		125	°C

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6.5 Typical Characteristics

At T_A = 25°C, V_S = ±15 V, R_L = 2 kΩ, unless otherwise noted.

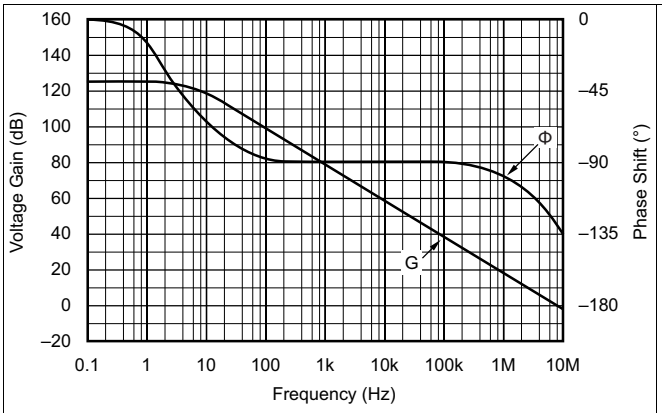

Figure 1. Open-Loop Gain and Phase vs Frequency

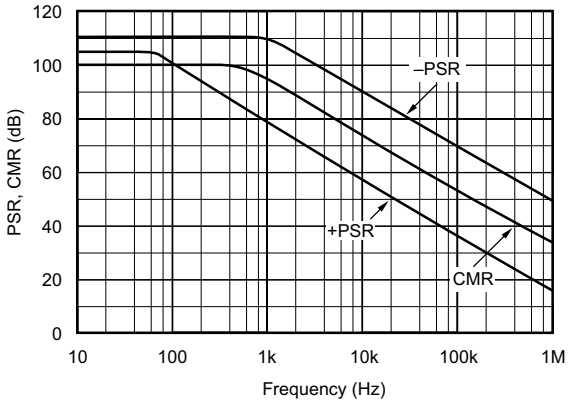

Figure 2. Power Supply and Common-Mode Rejection vs Frequency

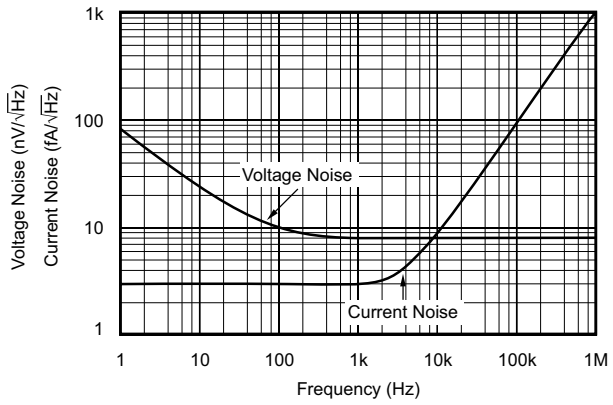

Figure 3. Input Voltage and Current Noise Spectral Density vs Frequency

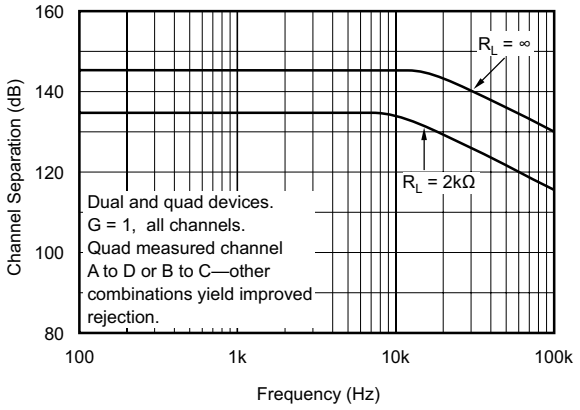

Figure 4. Channel Separation vs Frequency

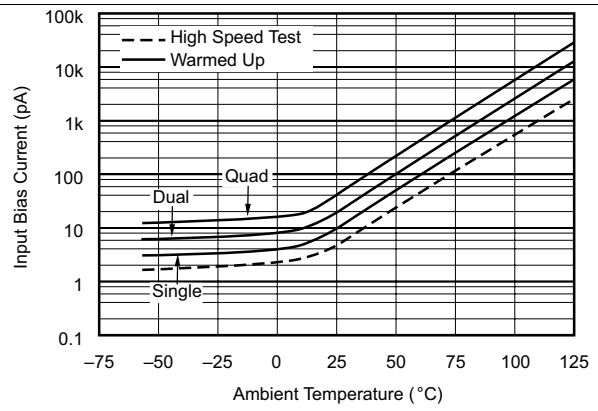

Figure 5. Input Bias Current vs Temperature

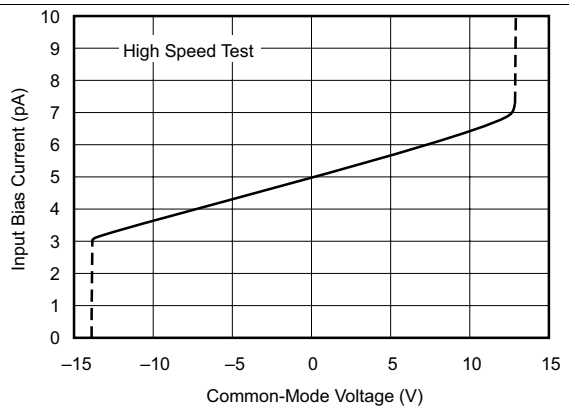

Figure 6. Input Bias Current vs Input Common-Mode Voltage

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Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, R_L = 2 kΩ, unless otherwise noted.

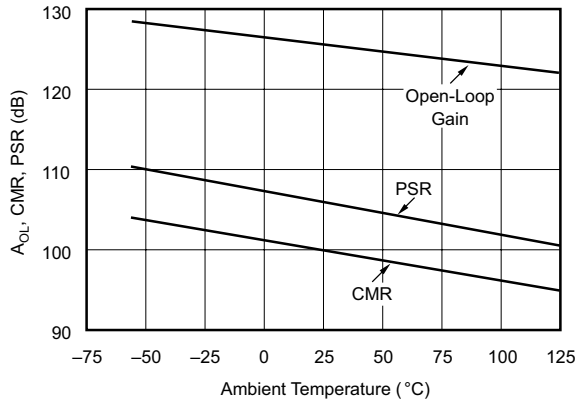

Figure 7. A_{OL}, CMR, PSR vs Temperature

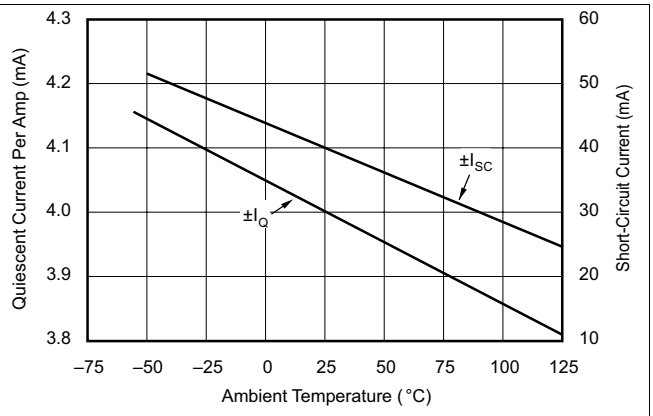

Figure 8. Quiescent Current and Short-Circuit Current vs Temperature

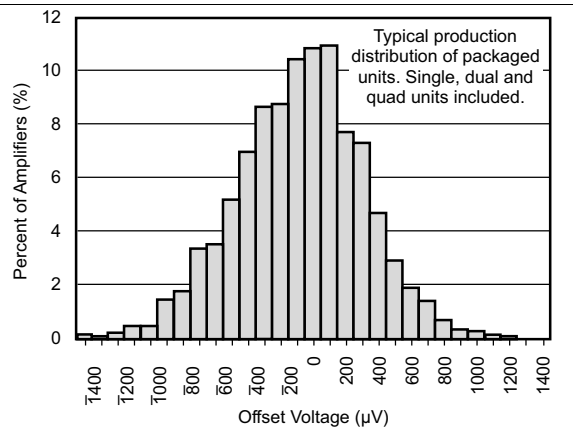

Figure 9. Offset Voltage Production Distribution

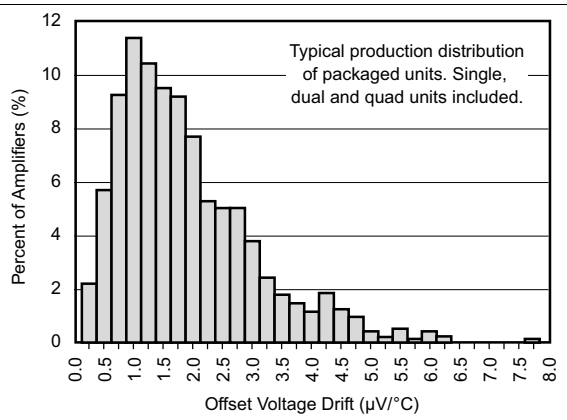

Figure 10. Offset Voltage Drift Production Distribution

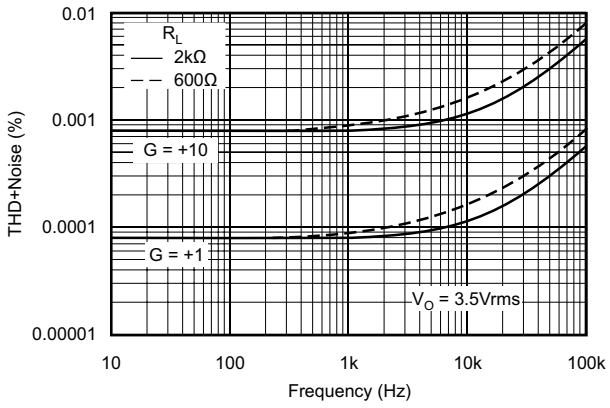

Figure 11. Total Harmonic Distortion + Noise vs Frequency

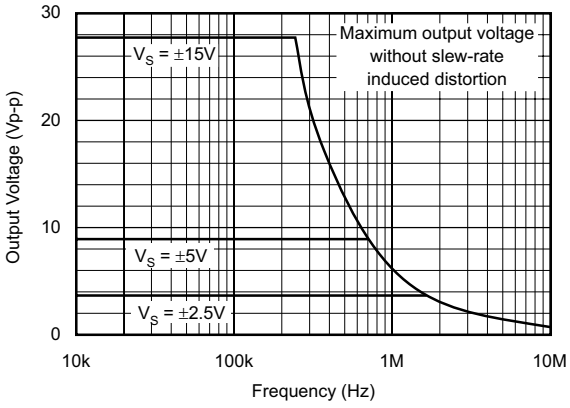

Figure 12. Maximum Output Voltage vs Frequency

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At T_A = 25°C, V_S = ±15 V, R_L = 2 kΩ, unless otherwise noted.

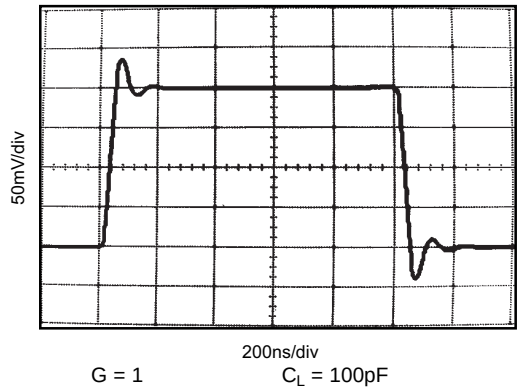

Figure 13. Small-Signal Step Response

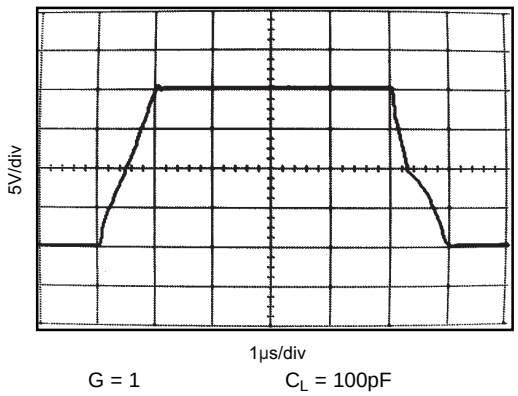

Figure 14. Large-Signal Step Response

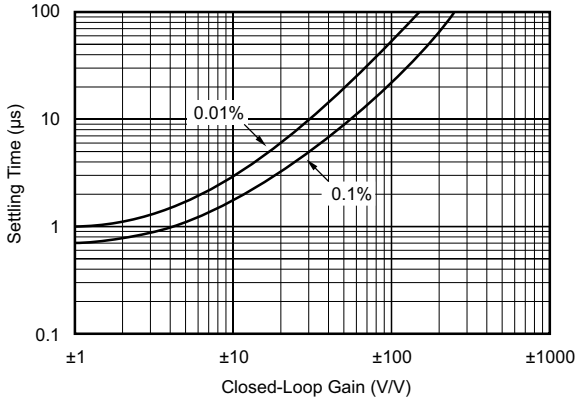

Figure 15. Settling Time vs Closed-Loop Gain

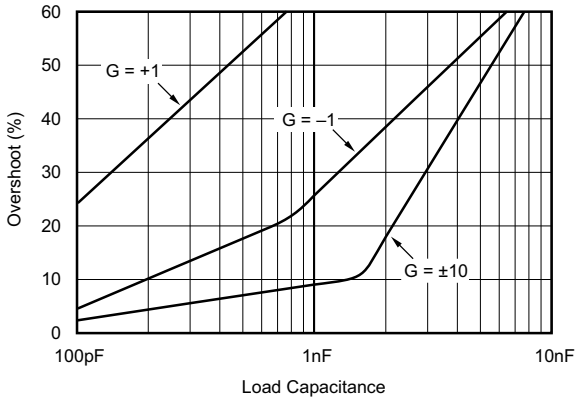

Figure 16. Small-Signal Overshoot vs Load Capacitance

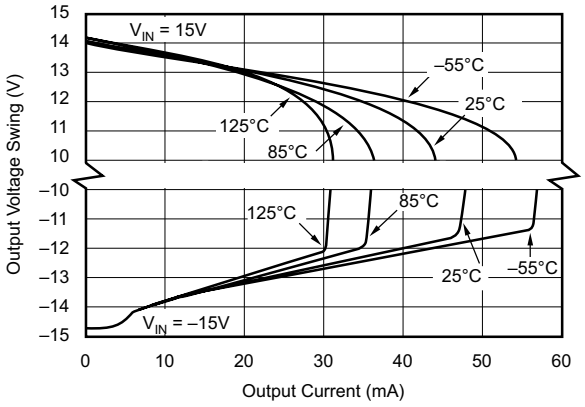

Figure 17. Output Voltage Swing vs Output Current

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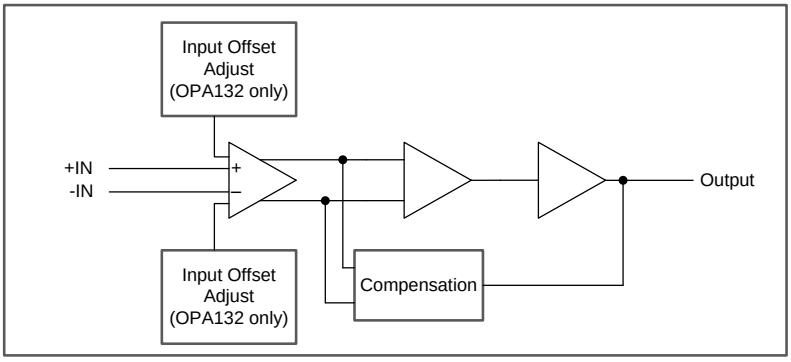
7 Detailed Description

7.1 Overview

The OPAx132 series of FET-input operational amplifiers provides highspeed and excellent dc performance. The combination of high slew rate and wide bandwidth provide fast settling time. Single, dual, and quad versions have identical specifications for maximum design flexibility. High performance grades are available in the single and dual versions. All are ideal for general-purpose, audio, data acquisition and communications applications, especially where high source impedance is encountered.

7.2 Functional Block Diagram



7.3 Feature Description

The OPAx132 series of JFET operational amplifiers combine low noise and wide bandwidth with precision and low input bias current to make them the ideal choice for applications with a high source impedance. The OPAx132 is unity-gain stable and features high slew rate (±20 V/μs) and wide bandwidth (8 MHz).

7.4 Device Functional Modes

The OPAx132 has a single functional mode and is operational when the power-supply voltage is greater than 5 V (±2.5 V). The maximum power supply voltage for the OPAx132 is 36 V (±18 V).

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx132 series operational amplifiers are unity-gain stable and suitable for a wide range of general-purpose applications. Power supply pins should be bypassed with 10-nF ceramic capacitors or larger.

The OPAx132 series operational amplifiers are free from unexpected output phase reversal common with FET operational amplifiers. Many FET-input operational amplifiers exhibit phase-reversal of the output when the input common-mode voltage range is exceeded. This can occur in voltage-follower circuits, causing serious problems in control loop applications. The OPAx132 series of operational amplifiers are free from this undesirable behavior. All circuitry is completely independent in dual and quad versions, assuring normal behavior when one amplifier in a package is overdriven or short-circuited.

8.1.1 Operating Voltage

The OPAx132 series of operation amplifiers operate with power supplies from ±2.5 V to ±18 V with excellent performance. Although specifications are production tested with ±15 V supplies, most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the *Typical Characteristics* section.

8.1.2 Offset Voltage Trim

Offset voltage of the OPAx132 series of amplifiers is laser trimmed and usually requires no user adjustment. The OPAx132 amplifier (single op amp version) provides offset voltage trim connections on pins 1 and 8. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 18. This adjustment should be used only to null the offset of the operational amplifier, not to adjust system offset or offset produced by the signal source. Nulling offset could degrade the offset voltage drift behavior of the operational amplifier. While it is not possible to predict the exact change in drift, the effect is usually small.

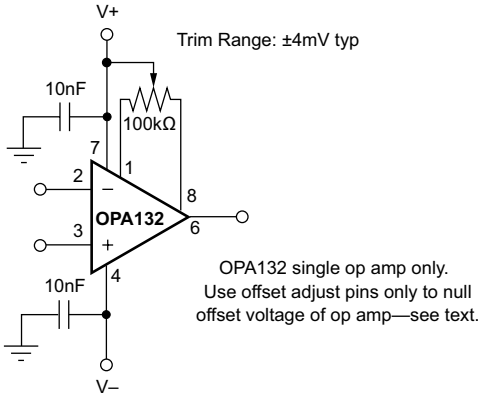

Figure 18. OPAx132 Offset Voltage Trim Circuit

8.1.3 Input Bias Current

The FET-inputs of the OPAx132 series provide very low input bias current and cause negligible errors in most applications. For applications where low input bias current is crucial, junction temperature rise should be minimized. The input bias current of FET-input operational amplifiers increases with temperature as shown in Figure 5.

The OPAx132 series may be operated at reduced power supply voltage to minimize power dissipation and temperature rise. Using ±3 V supplies reduces power dissipation to one-fifth that at ±15 V.

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Application Information (continued)

The dual and quad versions have higher total power dissipation than the single, leading to higher junction temperature. Thus, a warmed-up quad will have higher input bias current than a warmed-up single. Furthermore, an SOIC will generally have higher junction temperature than a DIP at the same ambient temperature because of a larger θ_{JA}.

Printed-circuit-board layout can also help minimize junction temperature rise. Temperature rise can be minimized by soldering the devices to the circuit board rather than using a socket. Wide copper traces will also help dissipate the heat by acting as an additional heat sink.

Input stage cascode circuitry assures that the input bias current remains virtually unchanged throughout the full input common-mode range of the OPAx132 series. See Figure 6.

8.2 Typical Application

The OPAx132 family offers outstanding dc precision and ac performance. These devices operate up to 36-V supply rails and offer ultralow input bias current and input bias current noise, as well as 8-MHz bandwidth and high capacitive load drive. These features make the OPAx132 a robust, high-performance operational amplifier for high-voltage industrial applications with high source impedance.

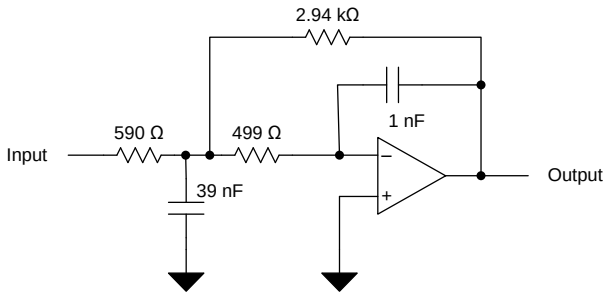

Figure 19. OPA132 2nd Order 30 kHz, Low Pass Filter Schematic

8.2.1 Design Requirements

Use the following parameters for this application:

- Gain = 5 V/V
- Low pass cutoff frequency = 30 kHz
- -40 db/dec filter response
- Maintain less than 3-dB gain peaking in the gain versus frequency response

8.2.2 Detailed Design Procedure

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

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Typical Application (continued)

8.2.3 Application Curve

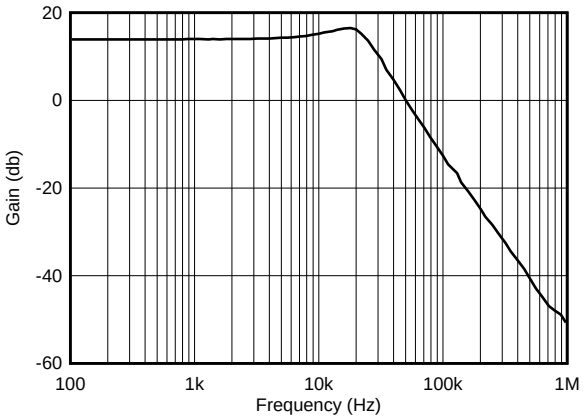

Figure 20. OPA132 2nd Order 30-kHz, Low Pass Filter Response

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9 Power Supply Recommendations

The OPAx132 is specified for operation from 5 V to 36 V (±2.5 V to ±18 V); many specifications apply from –40°C to 85°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the Typical Characteristics.

CAUTION

Supply voltages larger than 36 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 10-nF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines*.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 10 nF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to *Circuit Board Layout Techniques*, SLOA089.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in *Layout Example*, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

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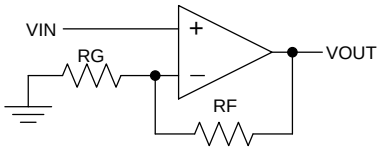
10.2 Layout Example



(Schematic Representation)

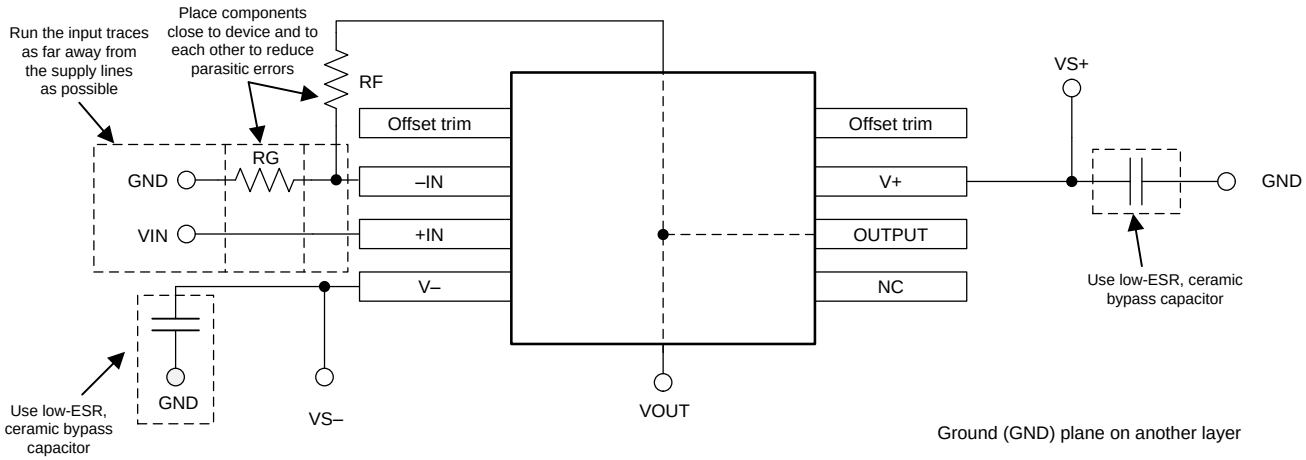


Figure 21. OPA132 Layout Example for the Noninverting Configuration

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 WEBENCH Filter Designer Tool

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

11.1.1.2 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.1.3 TI Precision Designs

The OPAx132 is featured in several TI Precision Designs, available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- *EMI Rejection Ratio of Operational Amplifiers*, SBOA128
- *Circuit Board Layout Techniques*, SLOA089

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA132	Click here	Click here	Click here	Click here	Click here
OPA2132	Click here	Click here	Click here	Click here	Click here
OPA4132	Click here	Click here	Click here	Click here	Click here

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11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA132P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI			
OPA132P1	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI			
OPA132PA	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI			
OPA132PA2	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI			
OPA132U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 132U	Samples
OPA132U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 132U	Samples
OPA132U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 132U	Samples
OPA132U1	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI			
OPA132UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 132U A	Samples
OPA132UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 132U A	Samples
OPA132UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 132U A	Samples
OPA132UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 132U A	Samples
OPA132UA2	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI			
OPA132UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 132U A	Samples
OPA132UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 132U A	Samples
OPA132UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 132U	Samples
OPA2132P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2132P	Samples

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2132PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2132P A	Samples
OPA2132PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2132P A	Samples
OPA2132PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2132P	Samples
OPA2132U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U	Samples
OPA2132U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U	Samples
OPA2132U/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U	Samples
OPA2132U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U	Samples
OPA2132UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U A	Samples
OPA2132UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U A	Samples
OPA2132UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U A	Samples
OPA2132UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U A	Samples
OPA2132UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U A	Samples
OPA2132UE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U	Samples
OPA2132UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U	Samples
OPA4132PA	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI			
OPA4132UA	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4132UA	Samples

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4132UA/2K5	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4132UA	Samples
OPA4132UA/2K5E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4132UA	Samples
OPA4132UA/2K5G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4132UA	Samples
OPA4132UAE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4132UA	Samples
OPA4132UAG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4132UA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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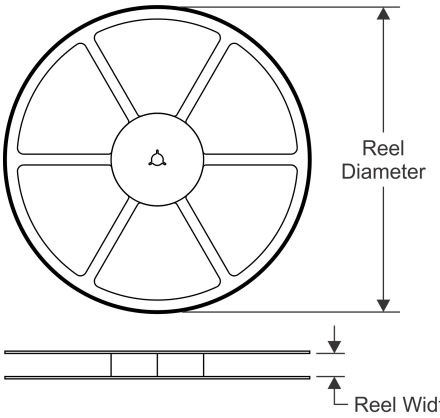
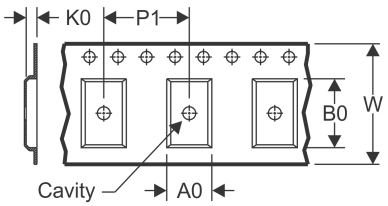
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

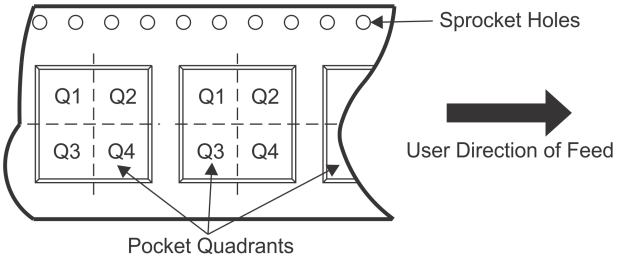


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA132U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA132UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2132U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2132UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4132UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

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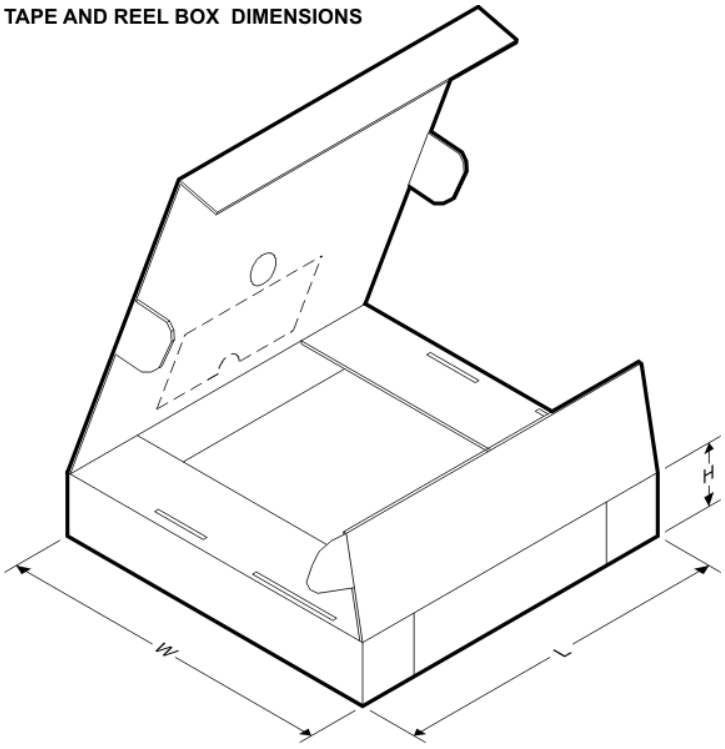
PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA132U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA132UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA2132U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA2132UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA4132UA/2K5	SOIC	D	14	2500	367.0	367.0	38.0

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Datasheet of OPA132U - IC OPAMP GP 8MHZ 8SOIC
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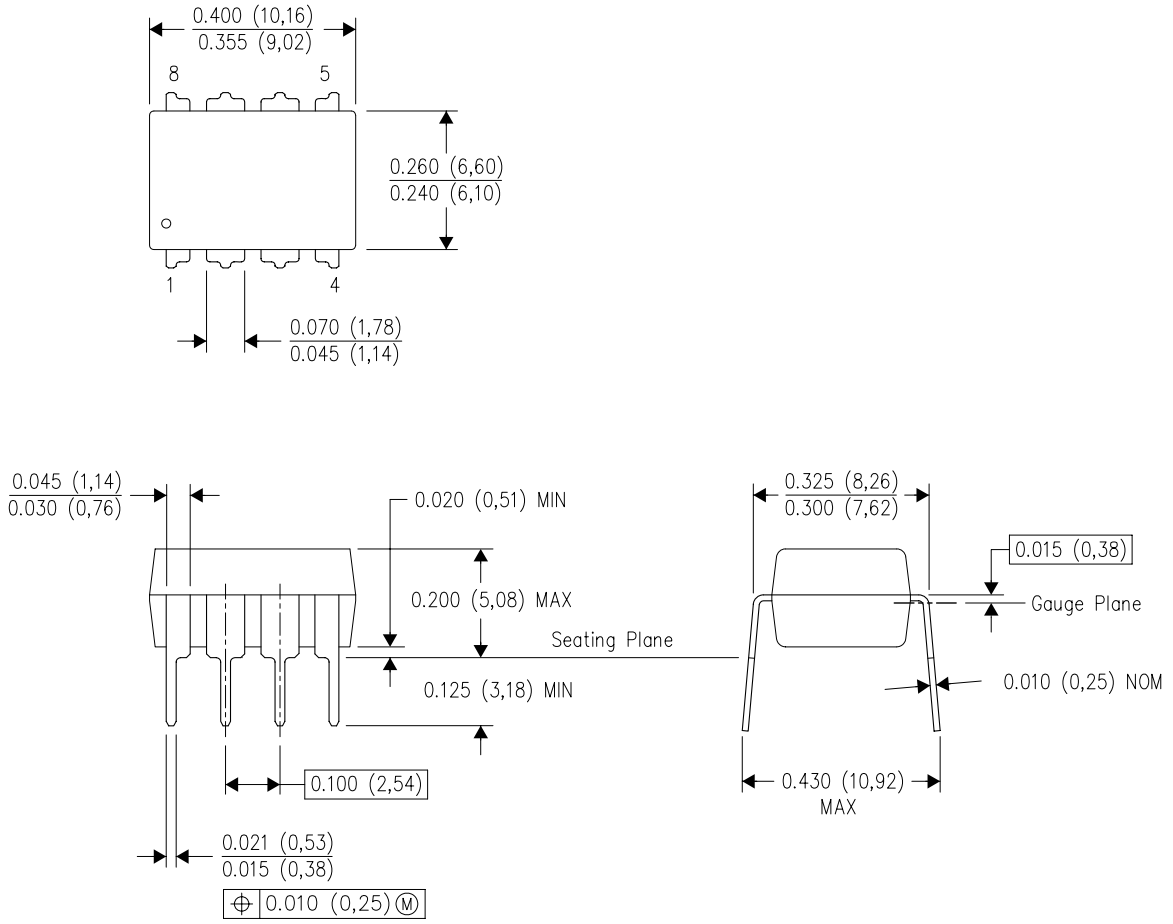
MECHANICAL DATA

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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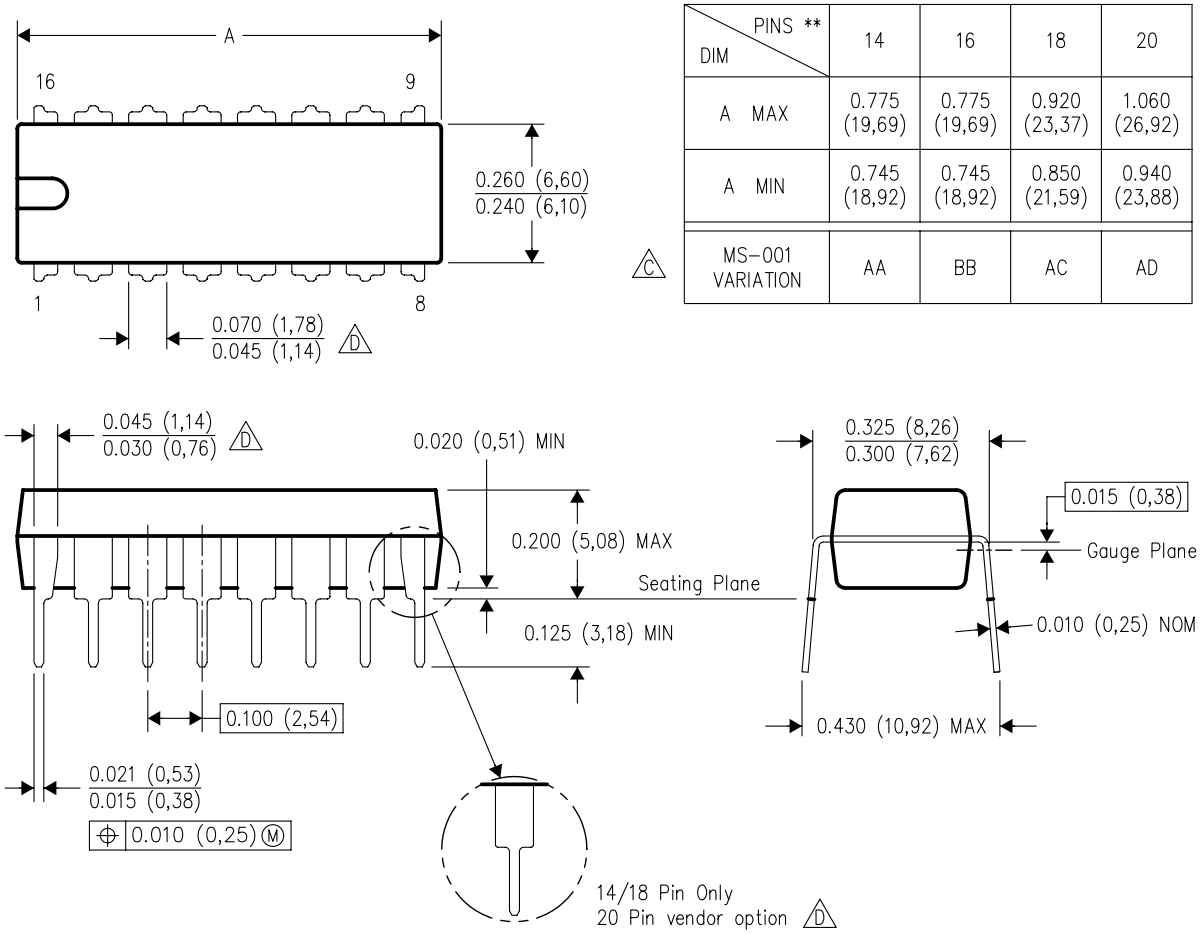
MECHANICAL DATA

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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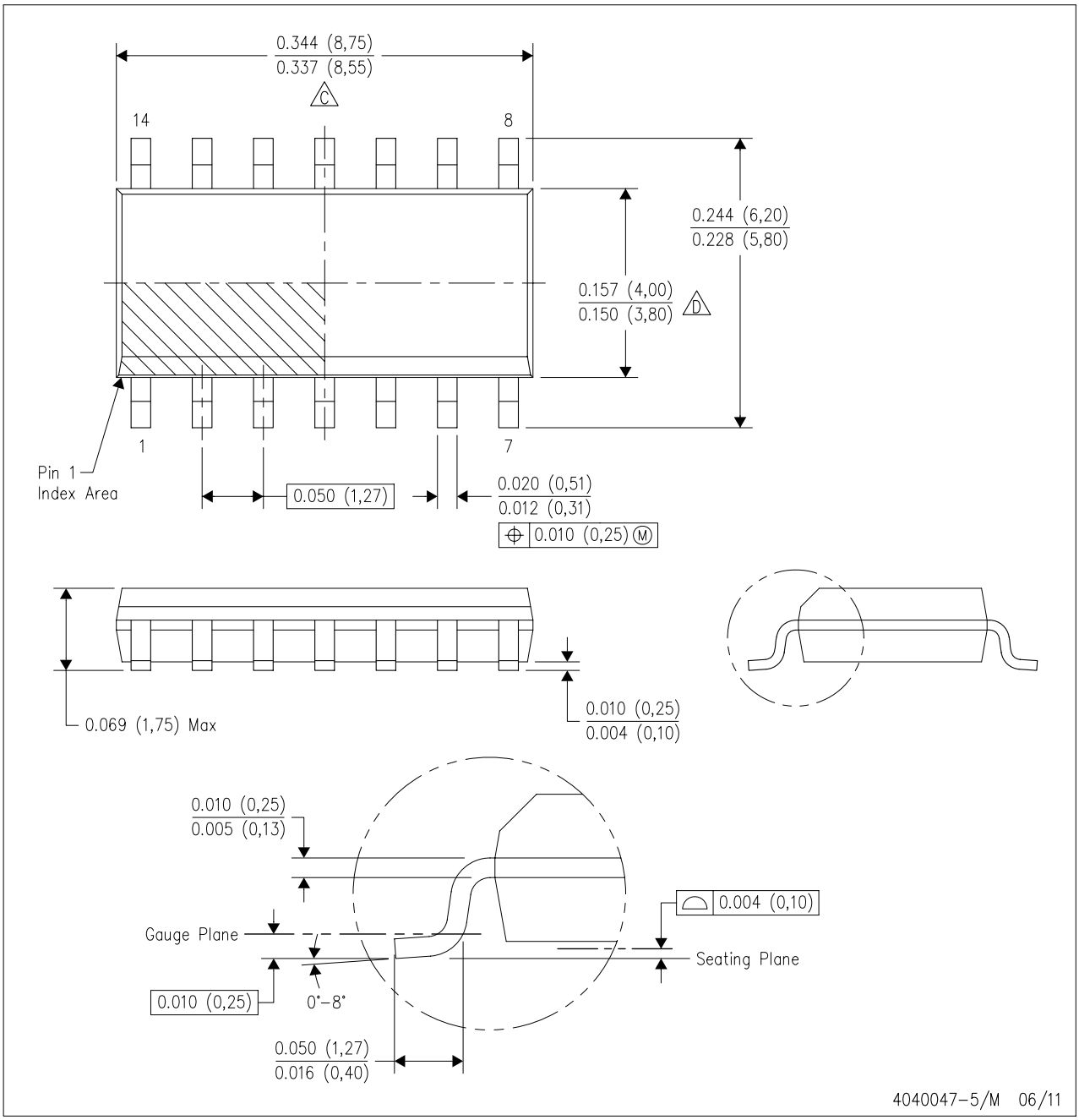
MECHANICAL DATA

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

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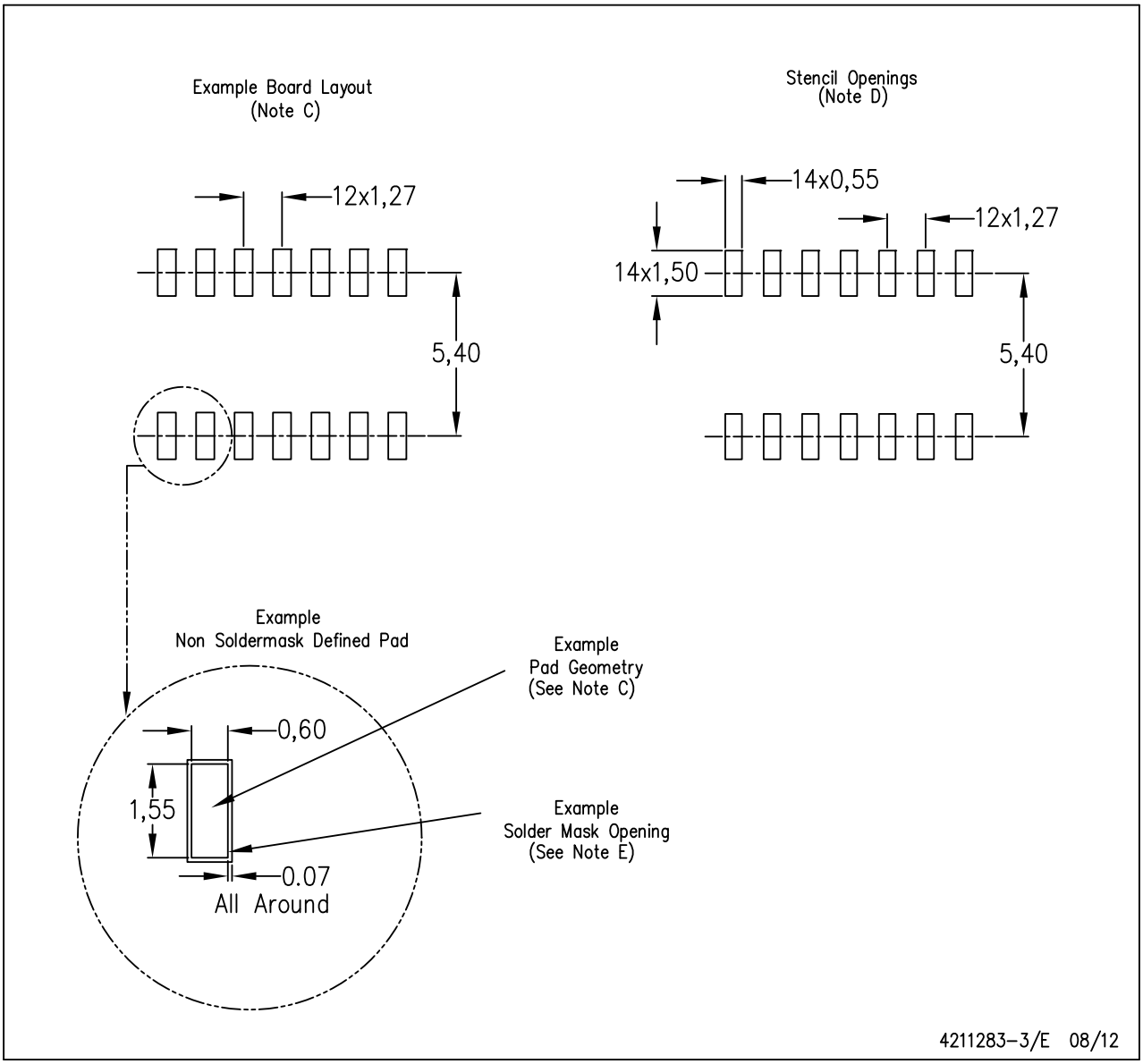
LAND PATTERN DATA

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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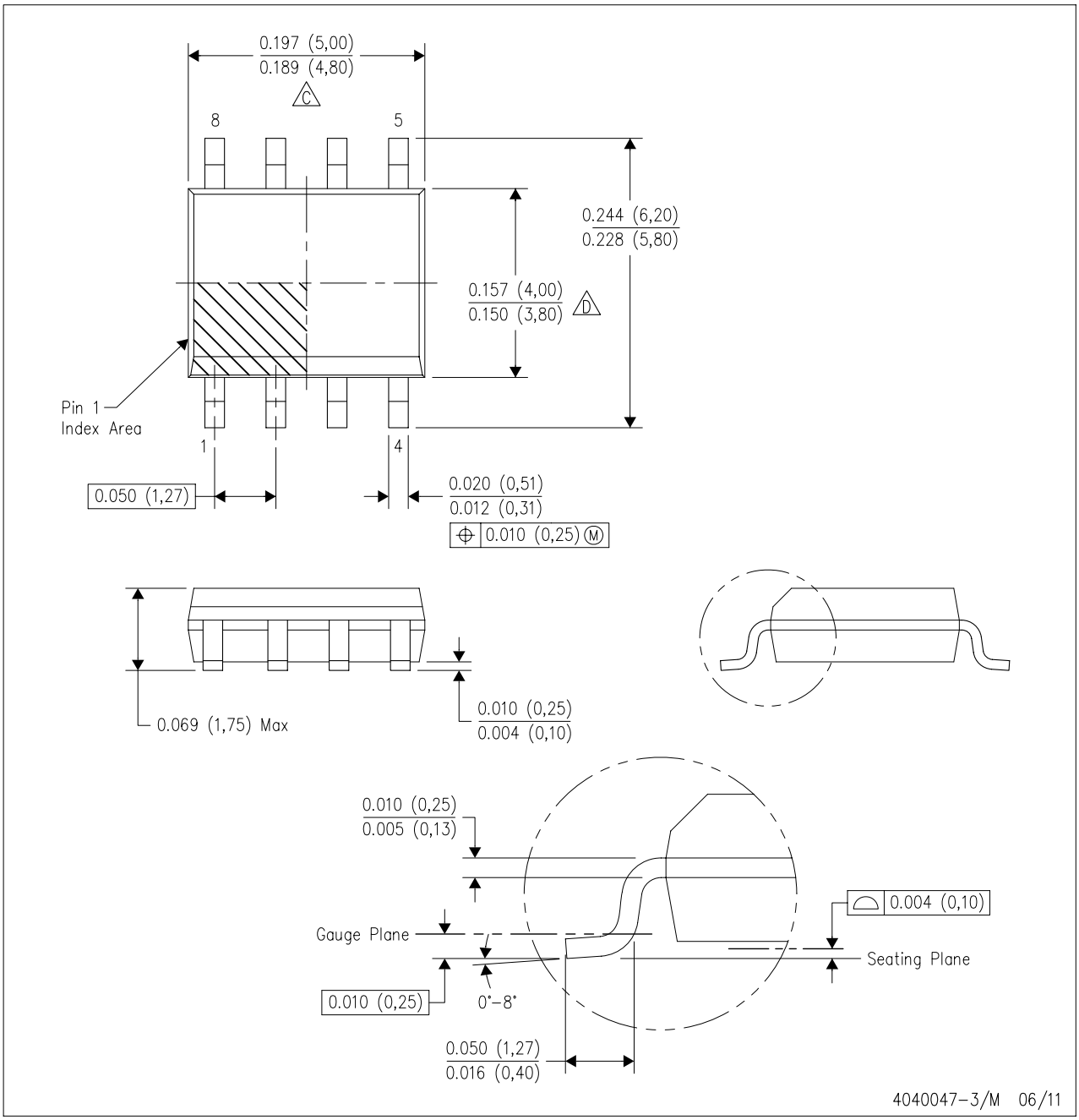
MECHANICAL DATA

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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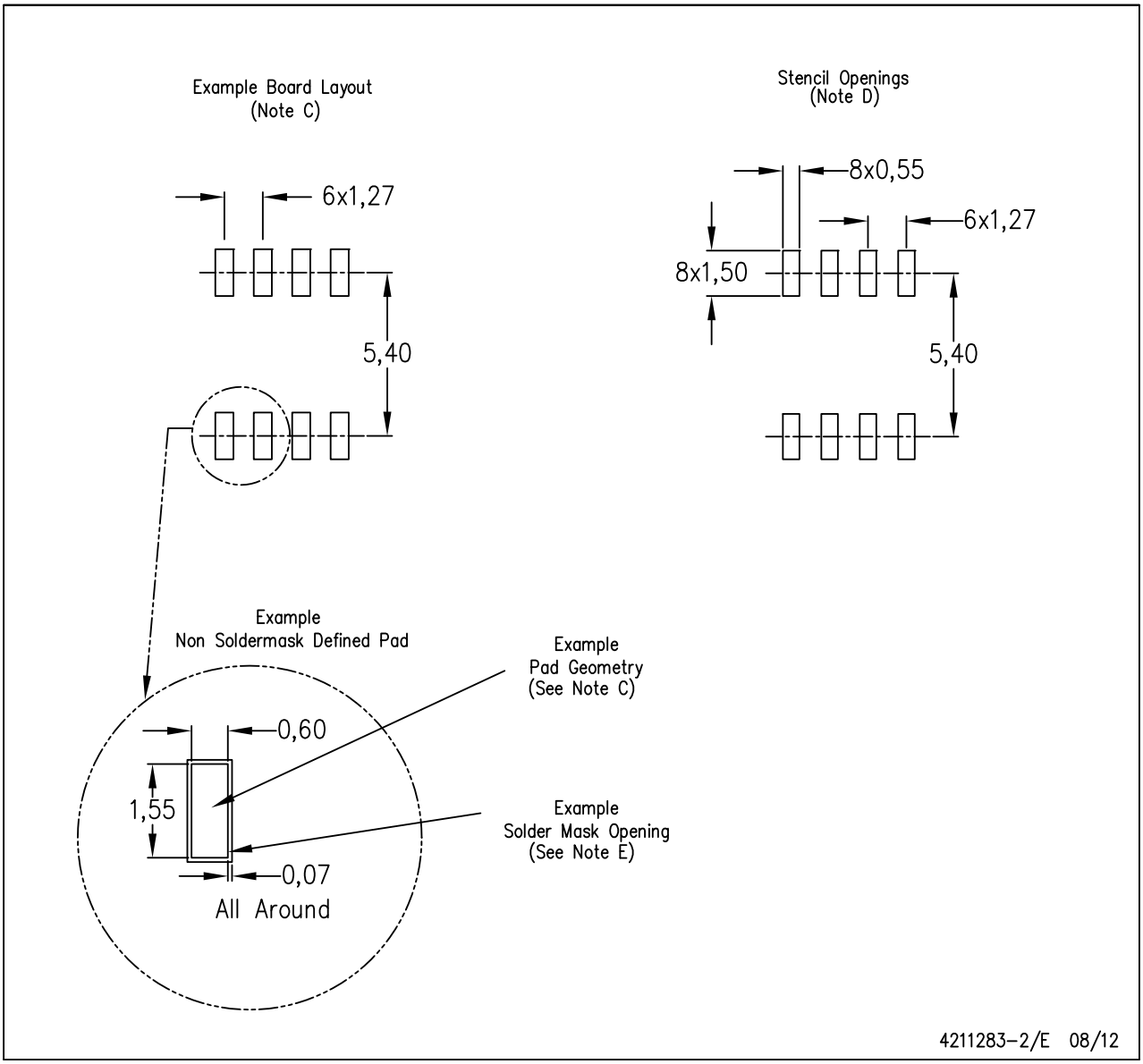
LAND PATTERN DATA

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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