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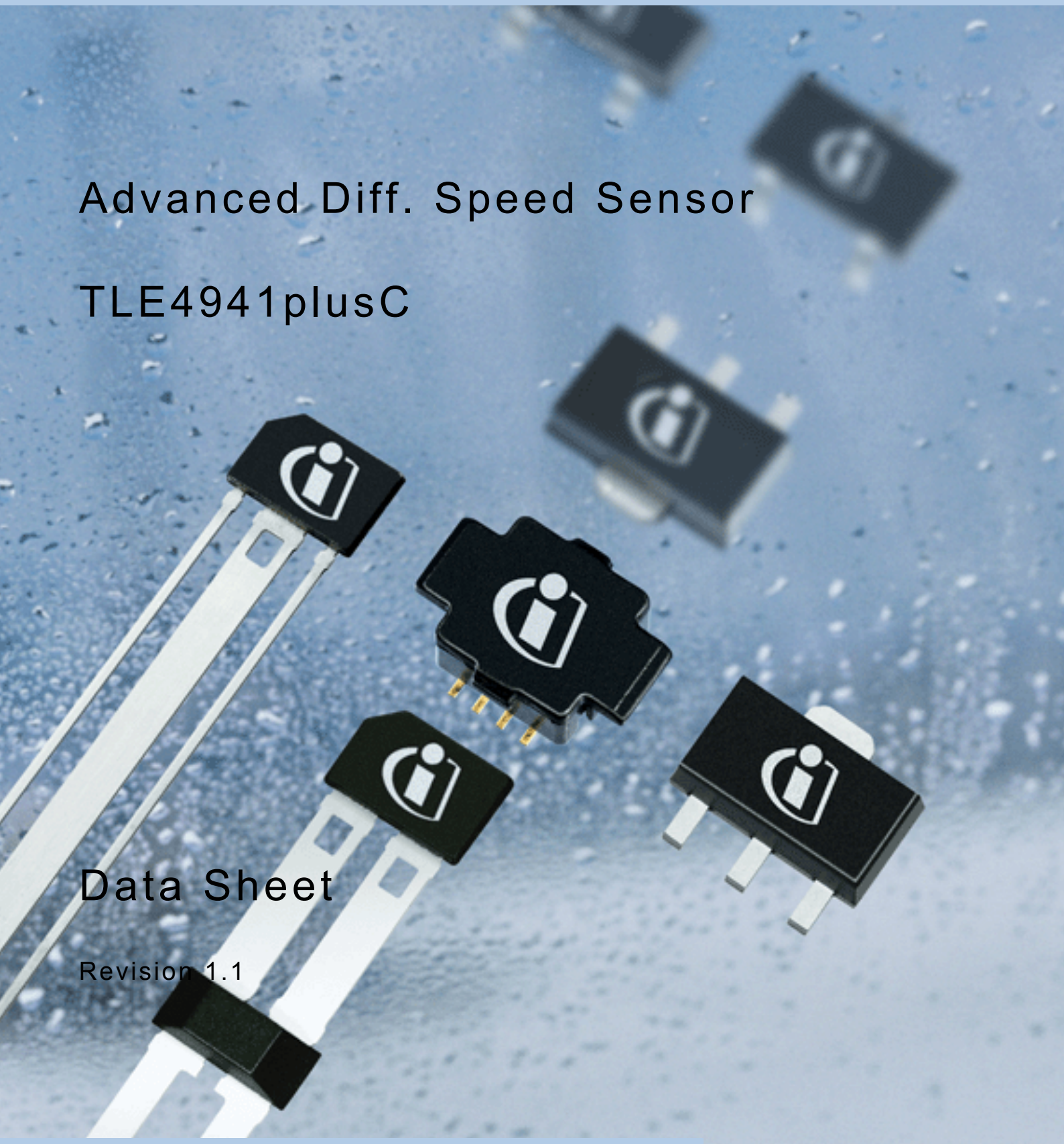
Advanced Diff. Speed Sensor

TLE4941plusC



Data Sheet

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Page	Subjects (major changes since revision 1.0)
13, 14	Footnote at “junction temperature” changed

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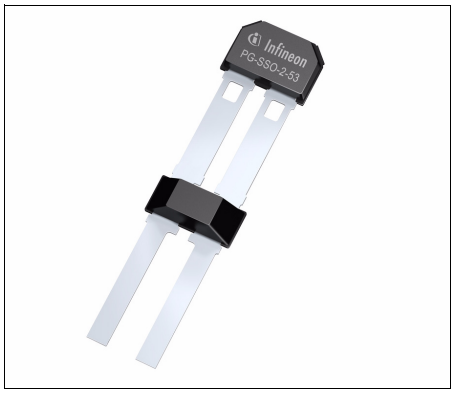
Advanced Differential Two-Wire Hall Effect Sensor IC **TLE4941plusC**

1 Product Description



1.1 Overview

The Hall Effect sensor IC TLE4941plusC is designed to provide information about rotational speed to modern vehicle dynamics control systems and Anti-Lock Braking Systems (ABS). The output has been designed as a two wire current interface. The sensor operates without external components and combines a fast power-up time with a low cut-off frequency. Designed specifically to meet harsh automotive requirements, excellent accuracy and sensitivity is specified over a wide temperature range and robustness to ESD and EMC has been maximized. State-of-the art BiCMOS technology is used for monolithic integration of the active sensor areas and the signal conditioning circuitry.

Finally, the optimized piezo compensation and the integrated dynamic offset compensation enables ease of manufacturing and the elimination of magnetic offsets.

The TLE4941plusC is additionally provided with an overmolded 1.8 nF capacitor for improved EMC performance.

1.2 Features

- Two-wire current interface
- Dynamic self-calibration principle
- Single chip solution
- No external components needed
- High sensitivity
- South and north pole pre-induction possible
- High resistive to piezo effects
- Large operating air-gaps
- Wide operating temperature range
- TLE4941plusC: 1.8 nF overmolded capacitor
- Applicable for small pitches (2mm Hall element distance)

Product Name	Product Type	Ordering Code	Packing
Advanced Diff. Speed Sensor	TLE4941plusC	SP000478508	PG-SSO-2-53

2 Functional Description

2.1 General

The differential Hall sensor IC detects the motion of ferromagnetic and permanent magnet structures by measuring the differential flux density of the magnetic field. To detect the motion of ferromagnetic objects the magnetic field must be provided by a back biasing permanent magnet. Either south or north pole of the magnet can be attached to the back side of the IC package.

Magnetic offsets of up to ± 30mT and device offsets are cancelled by a self-calibration algorithm. Only a few magnetic edges are necessary for self-calibration. After the offset calibration sequence, switching occurs when the input signal crosses the arithmetic mean of its max. and min. value (e.g. zero-crossing for sinusoidal signals).

The ON and OFF state of the IC are indicated by ***High*** and ***Low*** current consumption.

2.2 Pin Configuration and sensitive area description

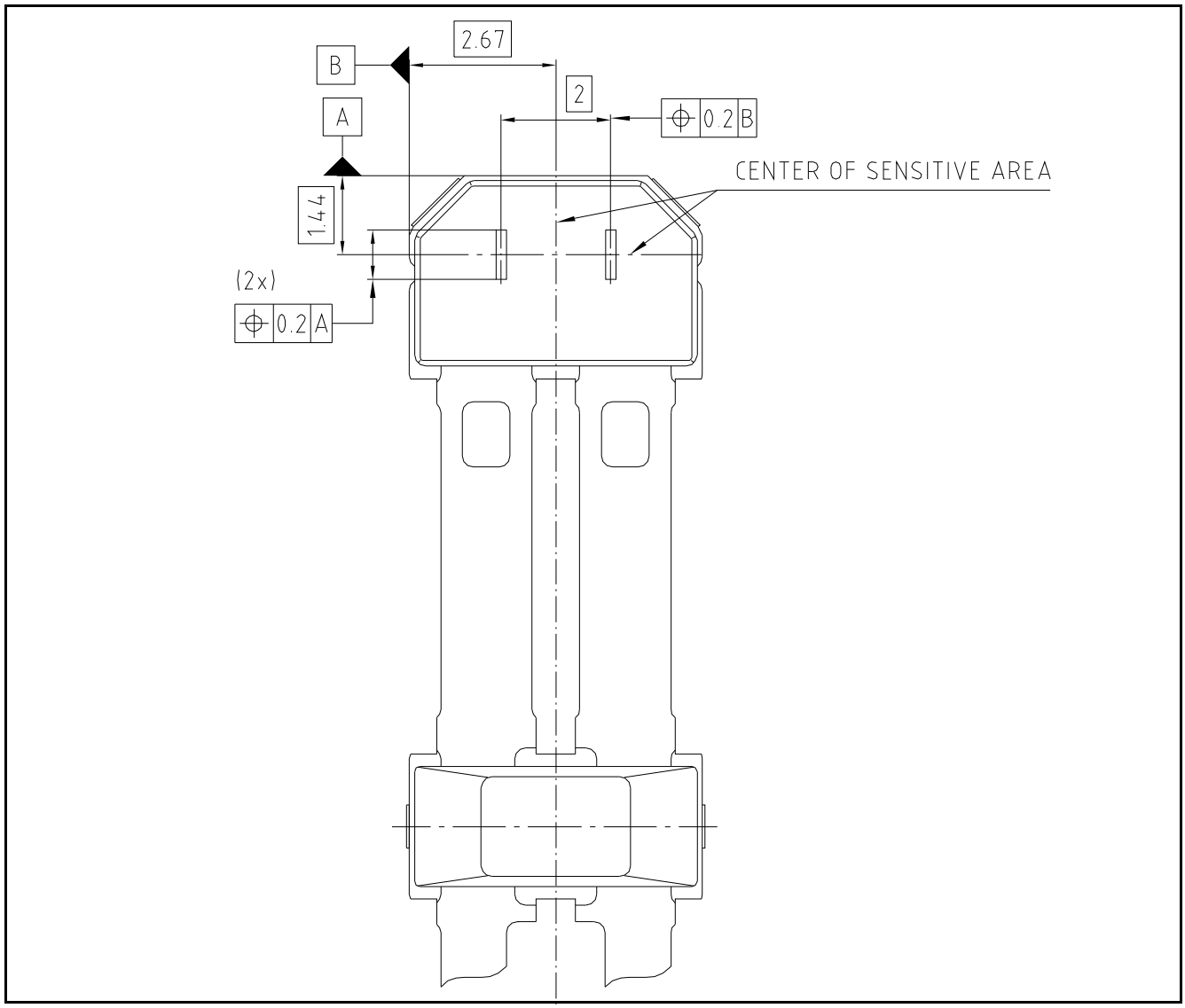
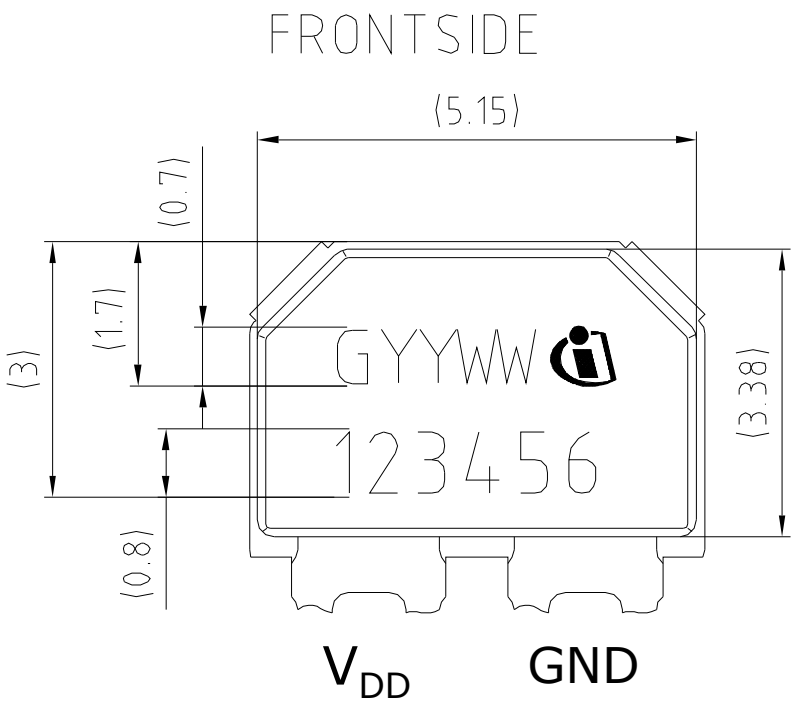
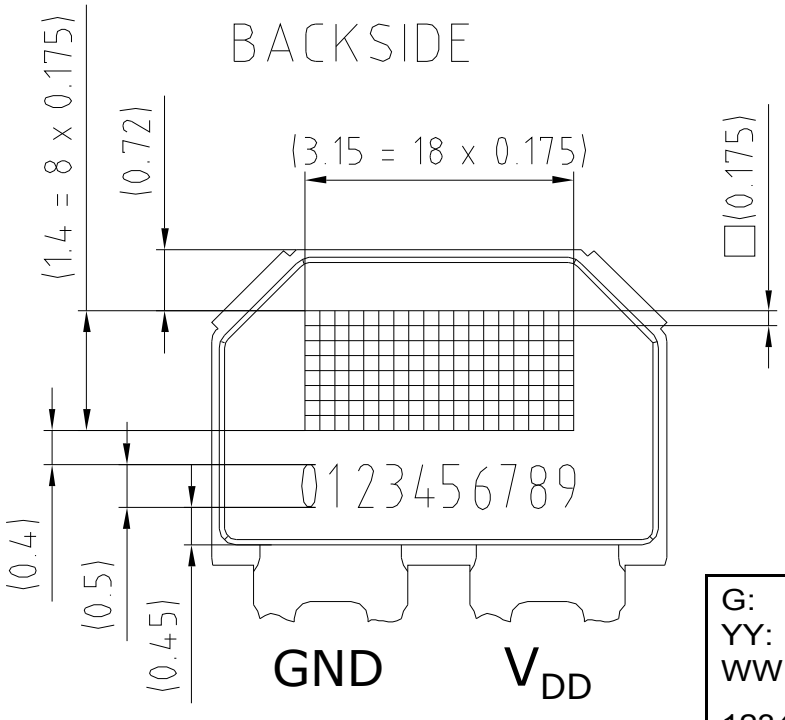


Figure 1 Pin Description and sensitive area (view on front side marking of component)

2.3 Marking and data matrix code description





G:	green package
YY:	production year
WW:	production week
123456:	
41CPA → TLE4941plusC	

Figure 2 Front side and Backside Marking of PG-SSO-2-53

2.4 Block Diagram

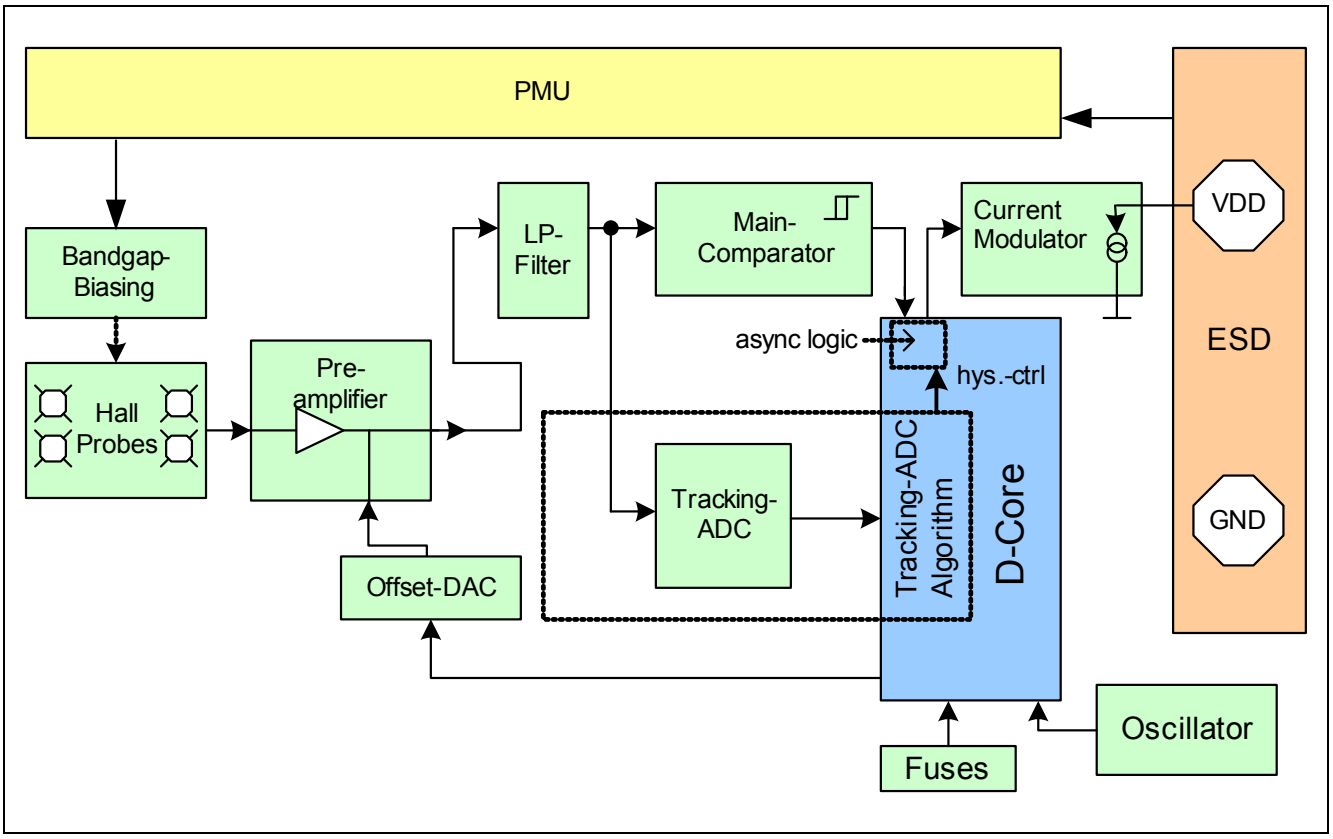


Figure 3 Block Diagram

The circuit is supplied internally by a 3V voltage regulator. An on-chip oscillator serves as clock generator for the digital part of the circuit.

TLE4941plusC signal path is comprised of a Hall probe pair, spaced at 2.0 mm, a differential amplifier, including a noise-limiting low-pass filter, and a comparator feeding a switched current output stage. In addition an offset cancellation feedback loop is provided by a tracking AD-converter, a digital core and an offset cancellation D/A converter.

The differential input signal is digitized in the tracking A/D converter and fed into the digital core. The minimum and maximum values of the input signal are extracted and their corresponding arithmetic mean value is calculated. The offset of this mean value is determined and fed back into the offset cancellation DAC.

In running mode (calibrated mode) the offset correction algorithm of the DSP is switched into a low-jitter mode, avoiding oscillation of the offset DAC LSB. Switching occurs at zero-crossing. It is only affected by the (small) remaining offset of the comparator and by the remaining propagation delay time. Signals below a defined threshold ΔB_{Limit} (see description **Figure 8**) are not detected to avoid unwanted parasitic switching.

2.4.1 Uncalibrated Mode

The short initial offset settling time $t_{\text{d,input}}$ may delay the detection of the input signal (the sensor is not yet “awake“). The magnetic input signal is tracked by the tracking ADC and monitored within the digital core. For detection the signal transient needs to exceed a threshold DNC (digital noise constant d1). When the signal slope is identified as a rising edge (or falling edge), a trigger pulse is issued to current modulator. A second trigger pulse is issued as soon as a falling edge (or rising edge respectively) is detected (and vice versa).

The digital noise constant value changes (d1 → d2) with the magnetic field amplitude, leading to a phase shift between the magnetic input signal and output signal. This value of the digital noise constant is determined by the signal amplitude and initial offset value. The smallest DNC, indicated as d1 in figure 4, represents parameter “dB_startup”. After calibration, consecutive output edges should have a nominal delay of about 180°.

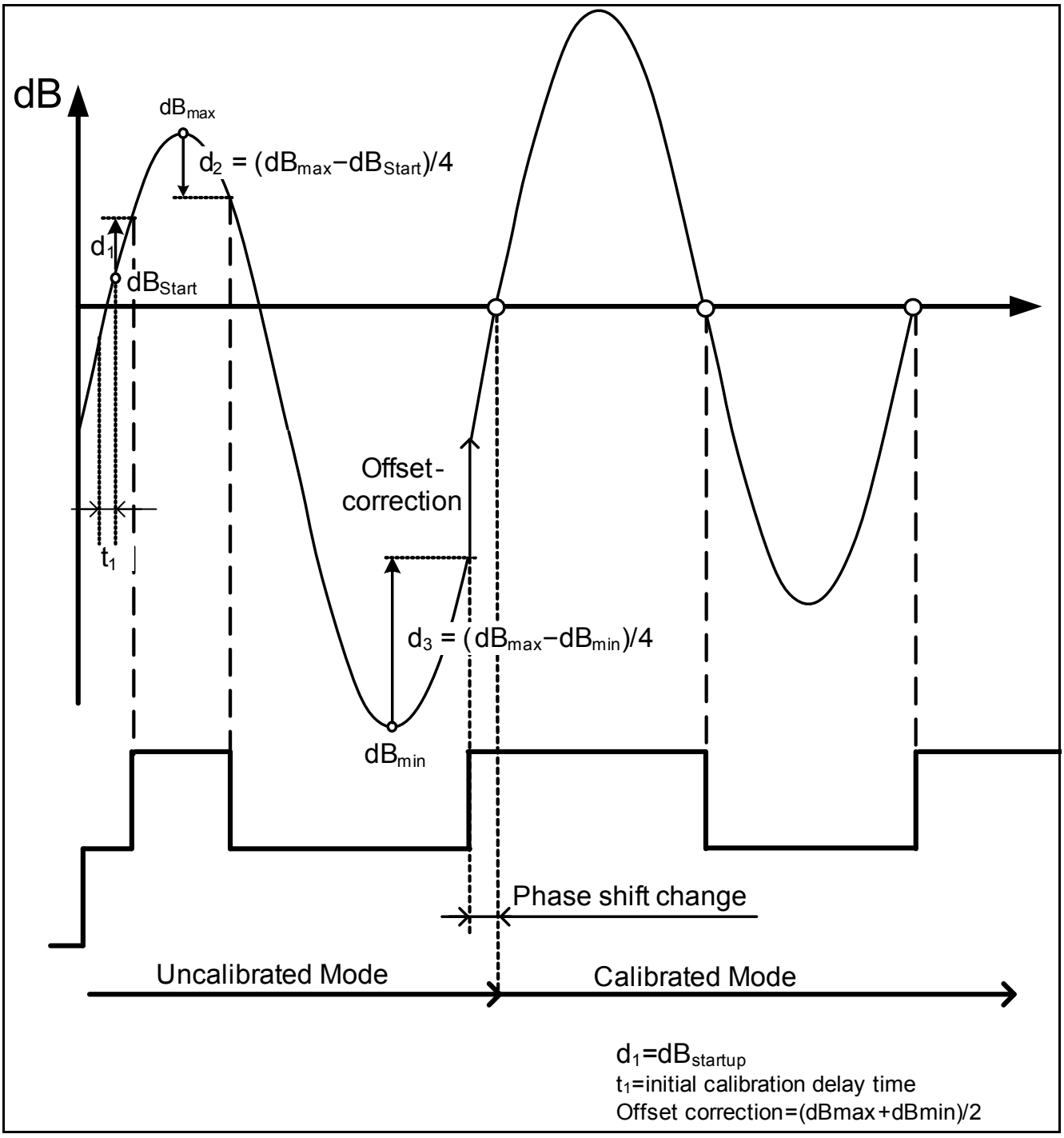


Figure 4 Example for Start-up Behavior

2.4.2 Transition to Calibrated Mode

In the calibrated mode the output will switch at zero-crossing of the input signal. The phase shift between input and output signal is no longer determined by the ratio between digital noise constant and signal amplitude. Therefore a sudden change in the phase shift may occur during the transition from uncalibrated to calibrated mode.

2.4.3 Additional Notes

The summed up change in phase shift from the first output edge issued to the output edges in calibrated mode will not exceed ± 90°.

2.4.4 Output Description

Under ideal conditions, the output shows a duty cycle of 50%. Under real conditions, the duty cycle is determined by the mechanical dimensions of the target wheel and its tolerances (40% to 60% might be exceeded for pitch >> 4mm due to the zero-crossing principle).

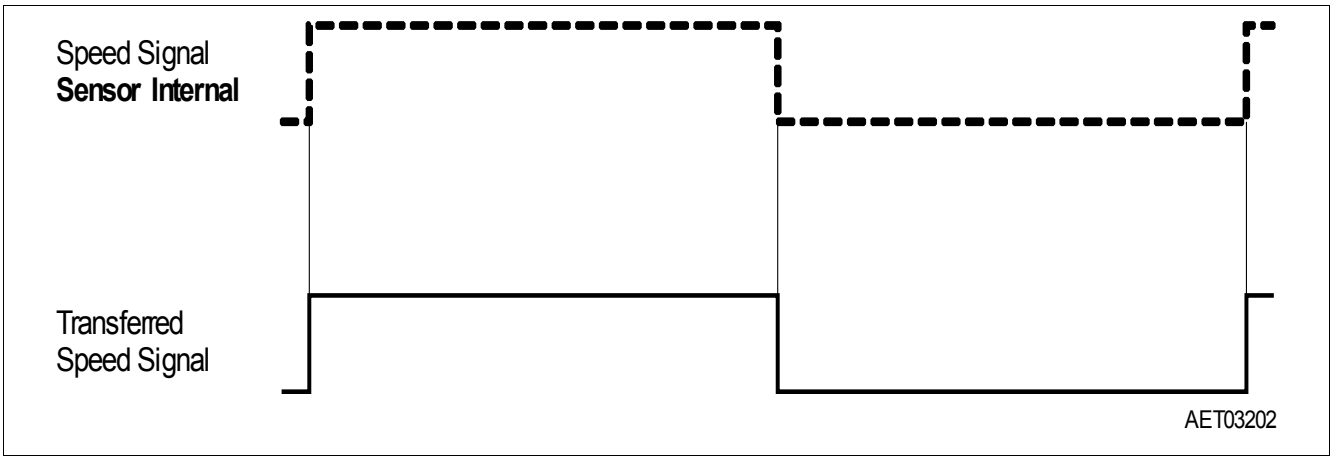


Figure 5 Speed Signal (half a period = 0.5 x 1/f_{speed})

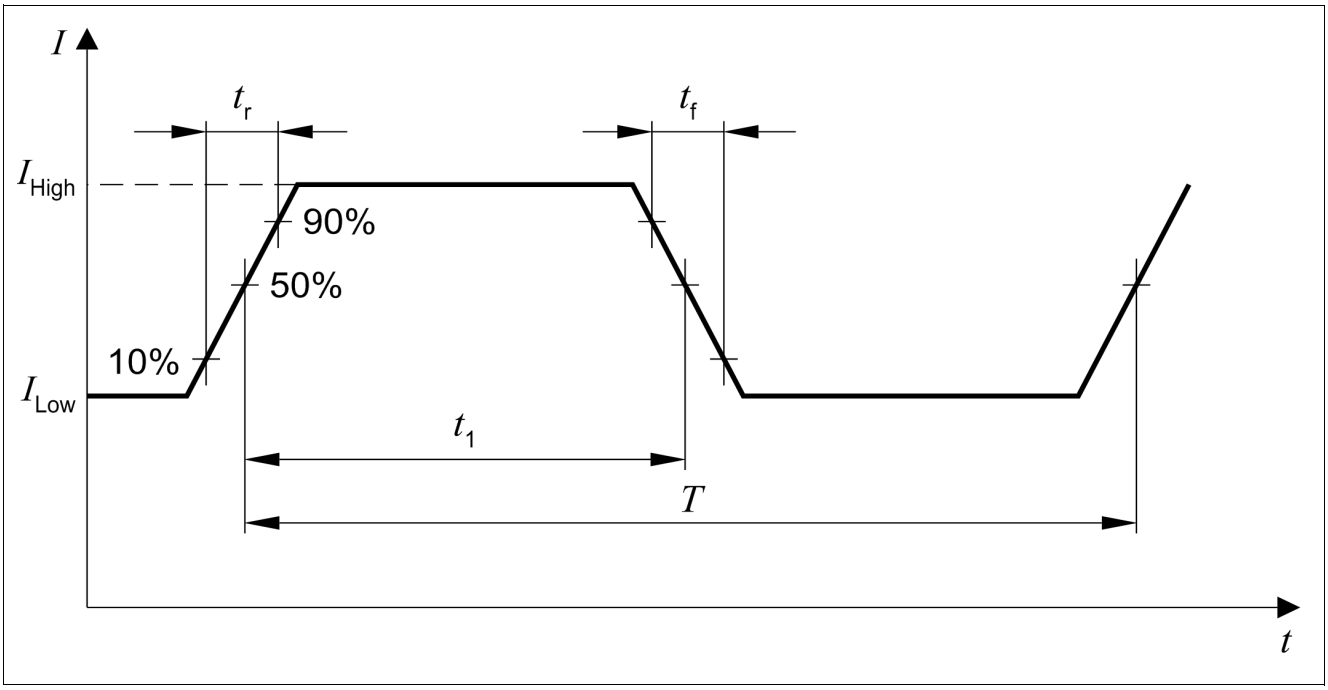


Figure 6 Definition of Rise and Fall Time; Duty Cycle = t_1/T x 100%

2.4.5 Behavior at Magnetic Input Signals Slower than f$_{mag}$ < 1Hz

Magnetic changes exceeding $\Delta\hat{B}_{startup}$ can cause output switching of the TLE4941plusC, even at f_{mag} significantly lower than 1 Hz. Depending on their amplitude edges slower than $\Delta t_{startup}$ might be detected. If the digital noise constant ($\Delta\hat{B}_{startup}$) is not exceeded before $\Delta t_{startup}$ a new initial self-calibration is started. In other words $\Delta\hat{B}_{startup}$ needs to be exceeded before $\Delta t_{startup}$. Output switching strongly depends on signal amplitude and initial phase.

2.4.6 Undervoltage Behavior

The voltage supply comparator has an integrated hysteresis V_{hys} with the maximum value of the release level V_{rel} < 4.5V. This determines the minimum required supply voltage V_{DD} of the chip. A minimum hysteresis V_{hys} of 0.7V is implemented thus avoiding a toggling of the output when the supply voltage V_{DD} is modulated due to the additional voltage drop at R_M when switching from low to high current level and V_{DD} = 4.5V (designed for use with R_{M}=75Ω).

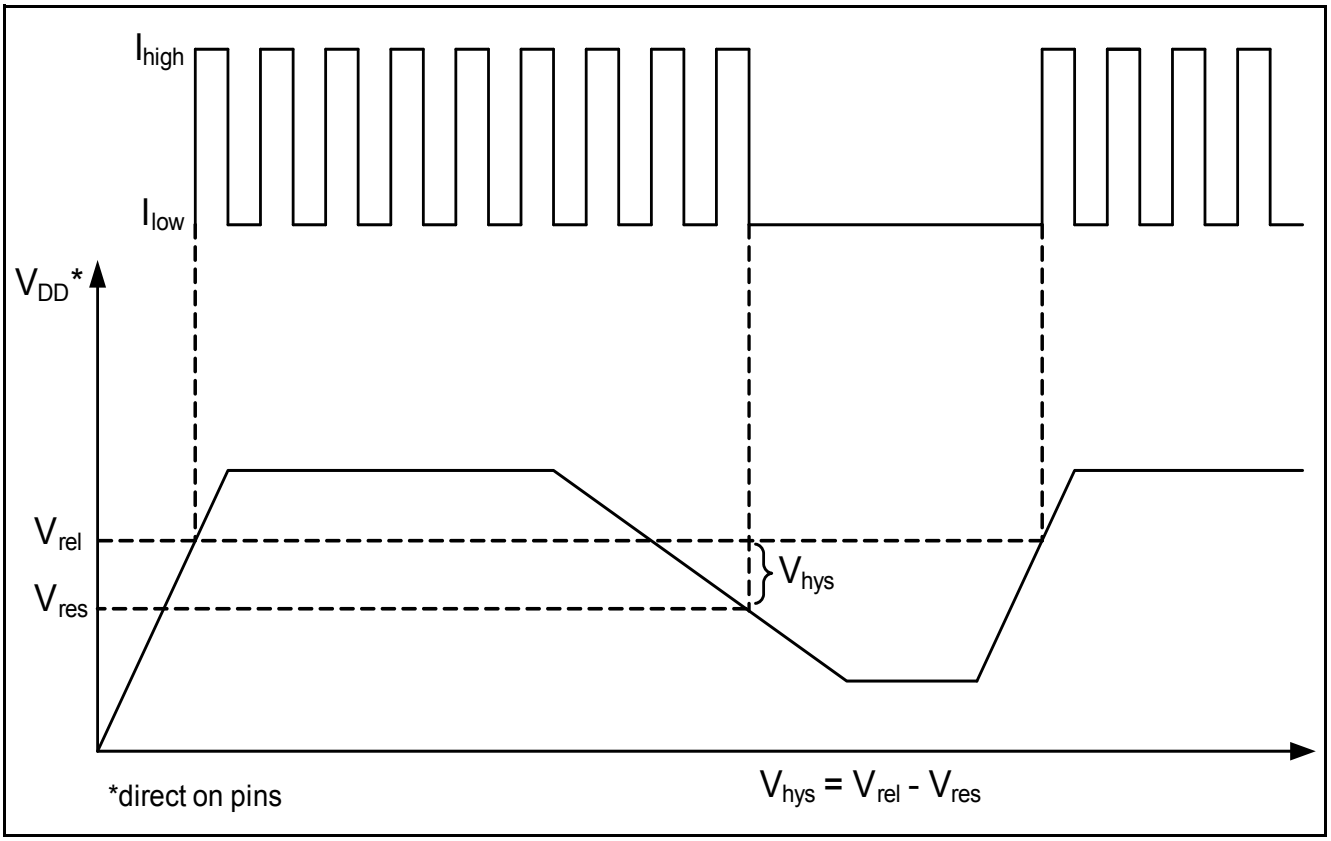


Figure 7 Start-up and undervoltage behavior

3 Specification

3.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings
T_j = – 40°C to 150°C, 4.5 V ≤ V_{DD} ≤ 20 V if not indicated otherwise

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_{DD}	-0.3	–	V	T_j < 80°C
		–	20		T_j = 150°C
		–	22		t = 10 × 5 min.
		–	24		t = 10 × 5 min. R_M ≥ 75 Ω included in V_{DD}
		–	27		t = 400 ms, R_M ≥ 75 Ω included in V_{DD}
Reverse polarity voltage	U_{rev}	-22		V	R_M ≥ 75 Ω included in V_{DD}, t<1 h
Reverse polarity current	I_{rev}	–	200	mA	External current limitation required, t<4 h
			300	mA	External current limitation required, t<1 h
Junction temperature[1]	T_j				
	EITHER	-40	125		10.000h
	OR		150		5000 h
	OR		160		2500 h,
	OR		170		500 h
	Additional		190		4 h, V_{DD} < 16.5 V
Number of power on cycles		500.000		times	
Immunity to external fields			1	Tesla	is equivalent to 800kA/m; T_j=-40..175°C[2]
Thermal resistance PG-SSO-2-53	R_{thJA}	–	190	K/W	[3]

1) This lifetime statement is an anticipation based on an extrapolation of Infineon's qualification test results. The actual lifetime of a component depends on its form of application and type of use etc. and may deviate from such statement. The lifetime statement shall in no event extend the agreed warranty period.
2) Conversion: B=μ_0*H (μ_0=4*π*10^{-7});
3) Can be significantly improved by further processing like overmolding

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

3.1.1 ESD Robustness

Table 2 ESD Protection
Characterized according to Human Body Model (HBM) tests in compliance with Standard EIA/JESD22-A114-B HBM (covers MIL STD 883D)

Parameter	Symbol	Test Result	Unit	Notes
ESD-Protection	V_{ESD}	±12	kV	$R = 1.5\ k\Omega$, $C = 100\ pF$

or >8000V for TLE4941plusC (H3B according AEC Q100)

Note: Tested at room temperature

3.2 Operating Range

Table 3 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_{DD} Extended Range	4.5 20	20 24[1)]	V	Directly on IC leads; includes not the voltage drop at R_M
Supply voltage modulation	V_{AC}	–	6	Vpp	V_{DD} = 13 V 0 < f_{mod} < 150 kHz[2)]
Junction temperature[3)]	T_j			°C	
	EITHER	-40	125		10.000h
	OR		150		5000 h
	OR		160		2500 h
	OR		170		500 h
Pre-induction	B_0	-500	+500	mT	
Pre-induction offset between outer probes	$\Delta B_{stat.,\ l/r}$	-30	+30	mT	
Differential Induction	ΔB	-120	+120	mT	
Magnetic signal frequency	f_{mag}	1	10000	Hz	

1) Extended range of 20..24V is not recommended. Latch-up test with factor 1.5 is not covered. Please see max ratings also.
2) sin wave
3) This lifetime statement is an anticipation based on an extrapolation of Infineon's qualification test results. The actual lifetime of a component depends on its form of application and type of use etc. and may deviate from such statement. The lifetime statement shall in no event extend the agreed warranty period.

3.3 Electrical Characteristics

Table 4 **[1]All values specified at constant amplitude and offset of input signal, over operating range, unless otherwise specified. Typical values correspond to V_{DD} = 12 V and T_A = 25°C**

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Supply current	I_{Low}	5.9	7	8.4	mA	
Supply current	I_{High}	11.8	14	16.8	mA	
Supply current ratio	I_{High} / I_{Low}	1.9	2.1	2.3		
Output rise/fall slew rate TLE4941plusC	t_r, t_f	 8 8	 – –	 22 26	mA/µs	R_M = 75 Ω +/-5% T_j < 125°C T_j < 170°C See Figure 6
Line regulation	dI_x/dV_{DD}			90	µA/V	quasi static[7]
Initial calibration delay time	$t_{d,input}$	–	120	300	µs	Additional to n_{start}[2)7]
Power up time				100	us	[3)7]
Magnetic edges required for offset calibration	n_{start}	–	-	4	magn. edges	5th edge correct [4)7]
Number of edges in uncalibrated mode	$n_{DZ\text{-}Startup}$	–	–	4	edges	[7]
Number of edges suppressed				0		after power on or reset
Magnetic edges required for first output pulse		1		2		after power on or reset
Duty cycle	DC	40	50	60	%	@$\Delta B \geq$2 mT sine wave see Figure 6 [5]
Signal frequency	f	1 2500	– –	2500 10000	Hz	[6]
Jitter, T_j < 150°C T_j < 170°C 1 Hz < f_{mag} < 2500 Hz	$S_{Jit\text{-}close}$	– –	– –	± 2 ± 3	%	1σ value V_{DD} = 12 V $\Delta B \geq$ 2 mT [7]
Jitter, T_j < 150°C T_j < 170°C 2500 Hz < f_{mag} < 10000 Hz	$S_{Jit\text{-}close}$	– –	– –	± 3 ± 4.5	%	1σ value V_{DD} = 12 V $\Delta B \geq$ 2 mT [7]
Jitter, T_j < 150°C T_j < 170°C 1 Hz < f_{mag} < 2500 Hz	$S_{Jit\text{-}far}$	– –	– –	± 4 ± 6	%	1σ value V_{DD} = 12 V 2 mT $\geq \Delta B >$ ΔB_{Limit} [7]
Jitter, T_j < 150°C T_j < 170°C 2500 Hz < f_{mag} < 10000 Hz	$S_{Jit\text{-}far}$	– –	– –	± 6 ± 9	%	1σ value V_{DD} = 12 V 2 mT $\geq \Delta B >$ ΔB_{Limit} [7]
Jitter at board net ripple f_{mag}<10kHz	$S_{Jit\text{-}AC}$			± 0.5	%	$V_{DD} = 13\,V \pm 6\,V_{pp}$ $0 < f_{mod} < 150\,kHz$ ΔB = 15 mT [7)8]
Permitted time for edge to exceed $\Delta \hat{B}_{startup}$	$\Delta t_{startup}$	–	–	590	ms	[7]
Time before chip reset[9]	Δt_{Reset}	590	–	848	ms	[7]

Table 4 **[1]All values specified at constant amplitude and offset of input signal, over operating range, unless otherwise specified. Typical values correspond to V_{DD} = 12 V and T_A = 25°C**

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Signal behavior after undervoltage or standstill > t_{Reset} Number of magnetic edges where the first switching occur	$n_{DZ\text{-}Start}$	1	–	2	edge	Magnetic edge amplitude according to $\Delta\hat{B}_{startup}$. $t_{d,input}$ has to be taken into account[7)10)]
Systematic phase error of output edges during start-up and uncalibrated mode		-90	–	+90	°	Systematical phase error of “uncal” edge; n^{th} vs. $n + 1^{th}$ edge (does not include random phase error)[7)]
Phase shift change during transition from uncalibrated to calibrated mode	$\Delta\Phi_{switch}$	 -45 -90	–	 +45 +90	°	[7)] $dB_{pp}>4*dB_{startup}$ $dB_{pp}<4*dB_{startup}$

1) All parameters refer to described test circuit in this document. See chapter 3.6 test circuit
2) Occurrence of “Initial calibration delay time $t_{d,input}$“
   If there is no input signal (standstill), a new initial calibration is triggered each Δt_{Reset}. This calibration has a duration $t_{d,input}$ of max. 300 µs. No input signal change is detected during that initial calibration time. In normal operation (signal startup) the probability of $t_{d,input}$ to come into effect is: $t_{d,input}$ / time frame for new calibration 300 µs/700 ms = 0.05%. After IC resets (e.g. after a significant undervoltage) $t_{d,input}$ will always come into effect.
3) V_{DD}>=4.5V
4) One magnetic edge is defined as a monotonic signal change of more than 3.3 mT
5) During fast offset alterations, due to the calibration algorithm, exceeding the specified duty cycle is permitted for short time periods
6) Frequency behavior not subject to production test - verified by design/characterization. Frequency above 2500 Hz may have influence on jitter performance and magnetic thresholds.
7) Not subject to production test, verified by design/characterization
8) Disturbances are sine-wave shaped: 1sigma value
9) When no output switching occurs for t > Δt_{Reset} the sensor is internally reset after each Δt_{Reset} time frame. See also chapter “2.4.5 Behavior at Magnetic Input Signals Slower than f_{mag} < 1Hz”
10) A loss of edges may occur at high frequencies

3.4 Magnetic Characteristics

Table 5 **[1]All values specified at constant amplitude and offset of input signal, over operating range, unless otherwise specified. Typical values correspond to V_{DD} = 12 V and T_A = 25°C**

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Limit threshold 1 Hz < f_{mag} < 2500 Hz 2500 Hz < f_{mag} < 10000 Hz	ΔB_{Limit}	 0.35	 0.7 –	 1.5 1.7	mT	[2] [3]
Magnetic differential field change necessary for startup 1 Hz < f < 2500 Hz 2500 Hz < f < 10000 Hz	$\Delta \hat{B}_{startup}$	– 0.7 –	– 1.4 –	– 3.3 3.9	mT	Magnetic field change for startup with the first edge (see “Uncalibrated Mode” on 2.4.1)

1) All parameters refer to described test circuit in this document. See chapter 3.6 test circuit.
2) Magnetic amplitude values, sine magnetic field, limits refer to the 50% criteria. 50% of edges are missing
3) ΔB_{Limit} is calculated out of measured sensitivity

3.5 Description of Magnetic Field

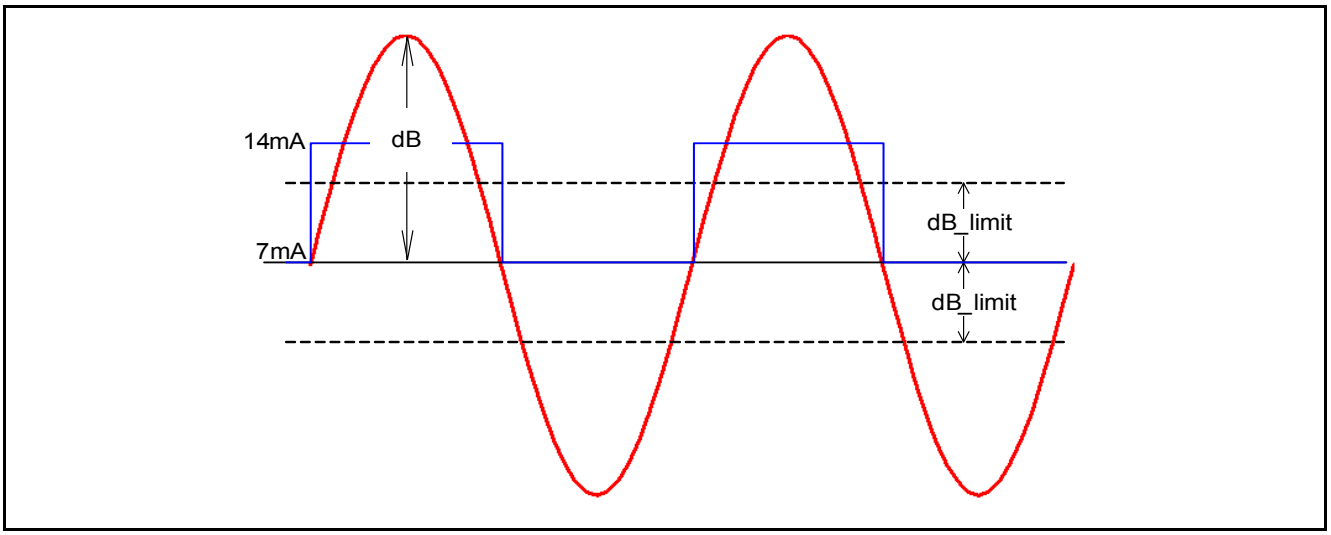
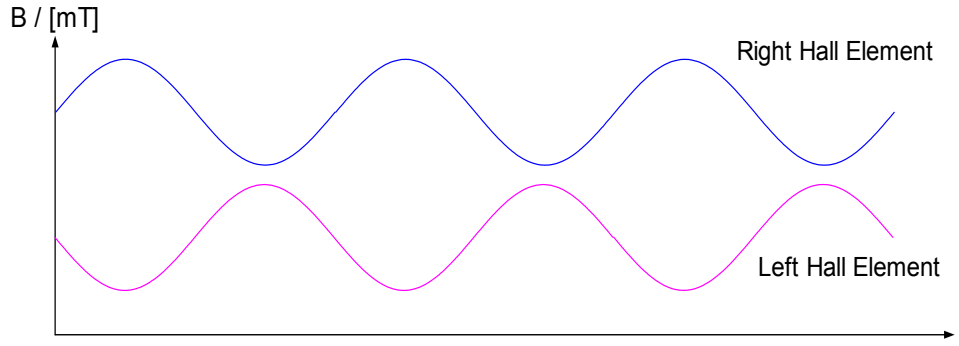
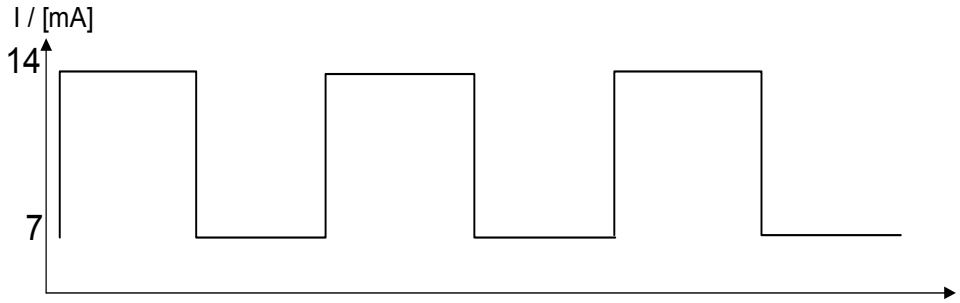
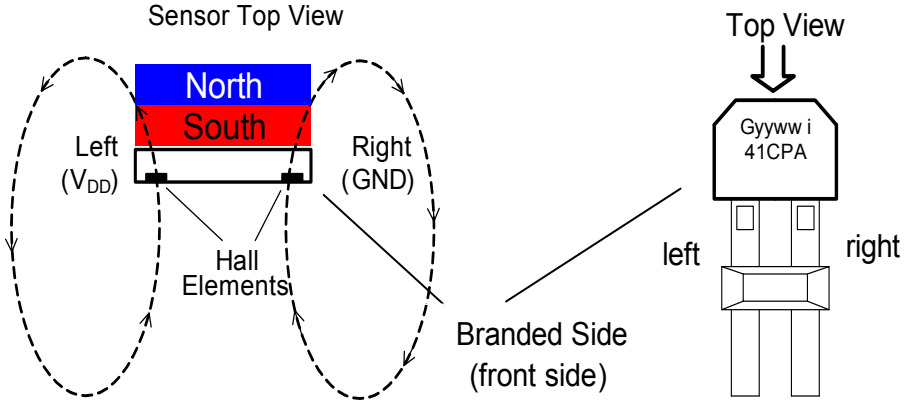


Figure 8 Description of differential field dB and switching threshold dB_{limit} (calibrated mode)

Note: dB is the resulting signal of difference between signal of right and left Hall element (right - left).
$dB = B_2$ (right) - B_1 (left)







Definition of magnetic field for this example

Positive	is considered when
South	pole shows to rear side of IC housing or when
North	pole shows to front side (=branded) of IC housing

(Gaussmeter: positive at north pole. Dot towards viewer)

Figure 9 Definition of field direction and sensor switching

Note: "If a positive field is applied to the right Hall probe (located over GND pin) and a negative field (or a weaker field) is applied to the left Hall probe, the resulting output current state is high

3.6 Test Circuit

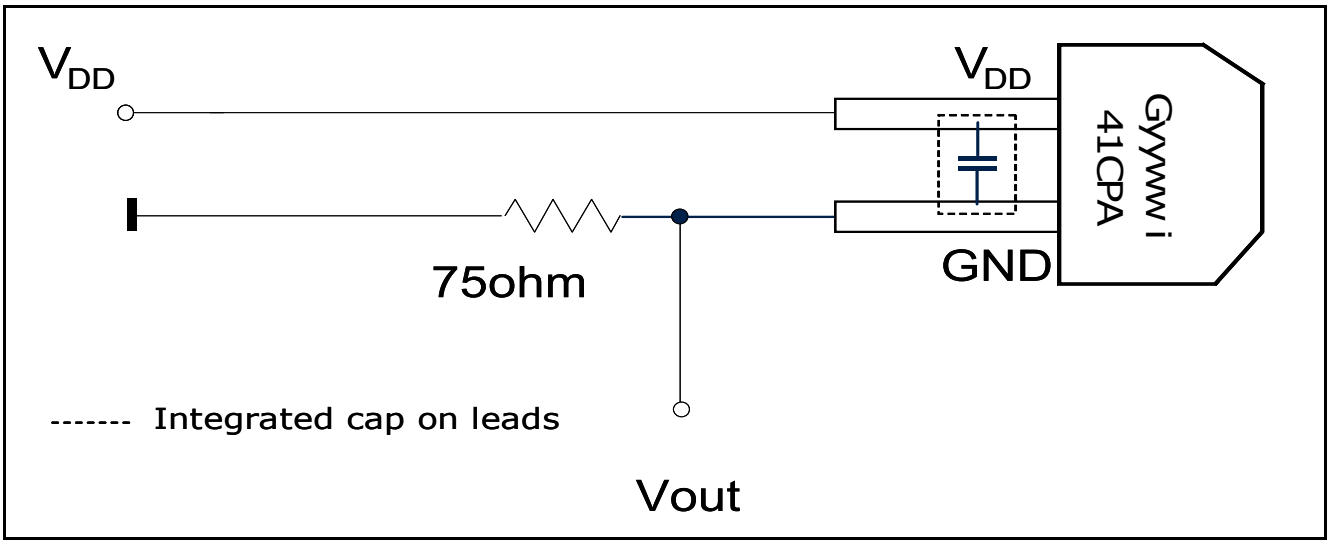


Figure 10 Test Circuit for TLE4941plusC

3.7 Application Circuit

Circuit below shows the recommended application circuit with reverse bias and overvoltage protection.

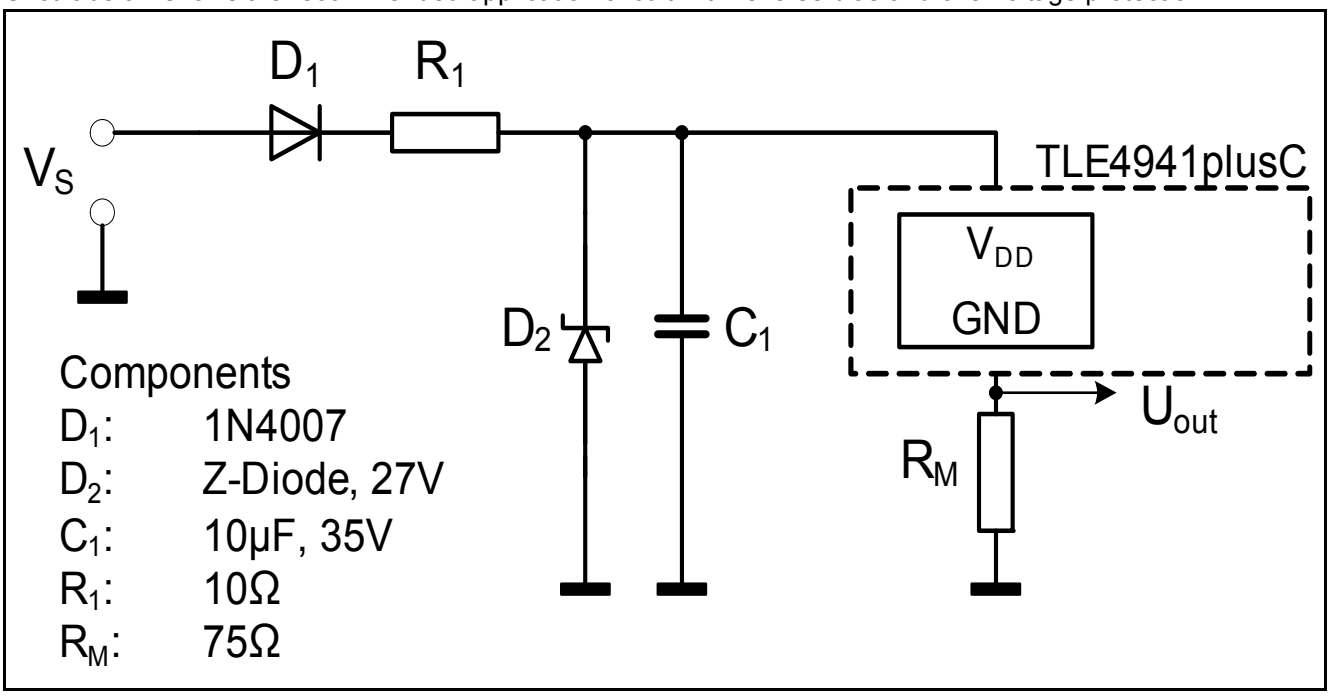


Figure 11 Application Circuit

An implementation of 10Ω in V_{DD} path reduces minimum power supply direct on leads of the sensor, but decreases max current at D_2 and makes PCB more robust. This PCB represents a compromise of minimum power supply and current flow on D_2. With higher values than 10Ω a higher minimum supply voltage and higher robustness is reached.

3.8 Typical Diagrams (measured performance)

Note: Temperatures above 170°C are not guaranteed by this data sheet even if shown below

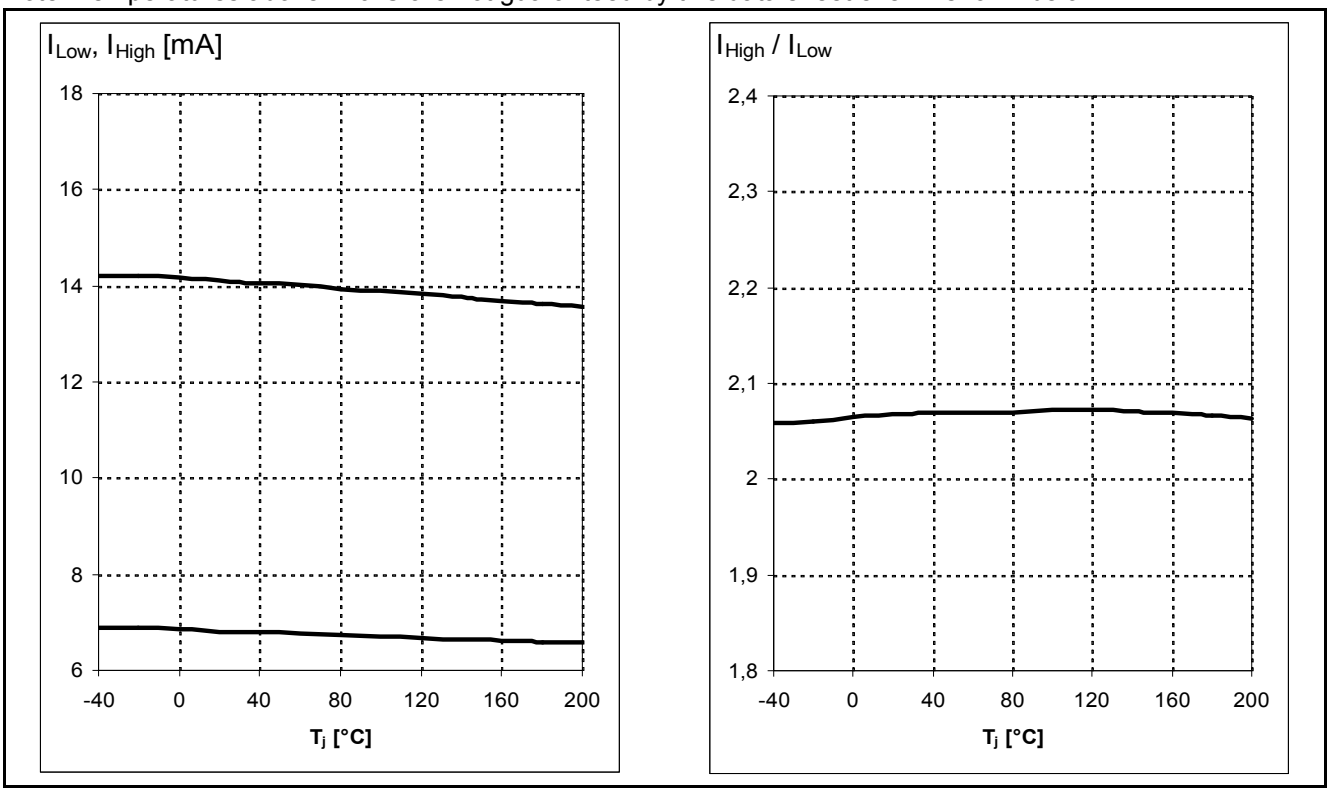


Figure 12 Supply Current = $f(T)$ (left), Supply Current Ratio $I_{high} / I_{Low} = f(T)$ (right)

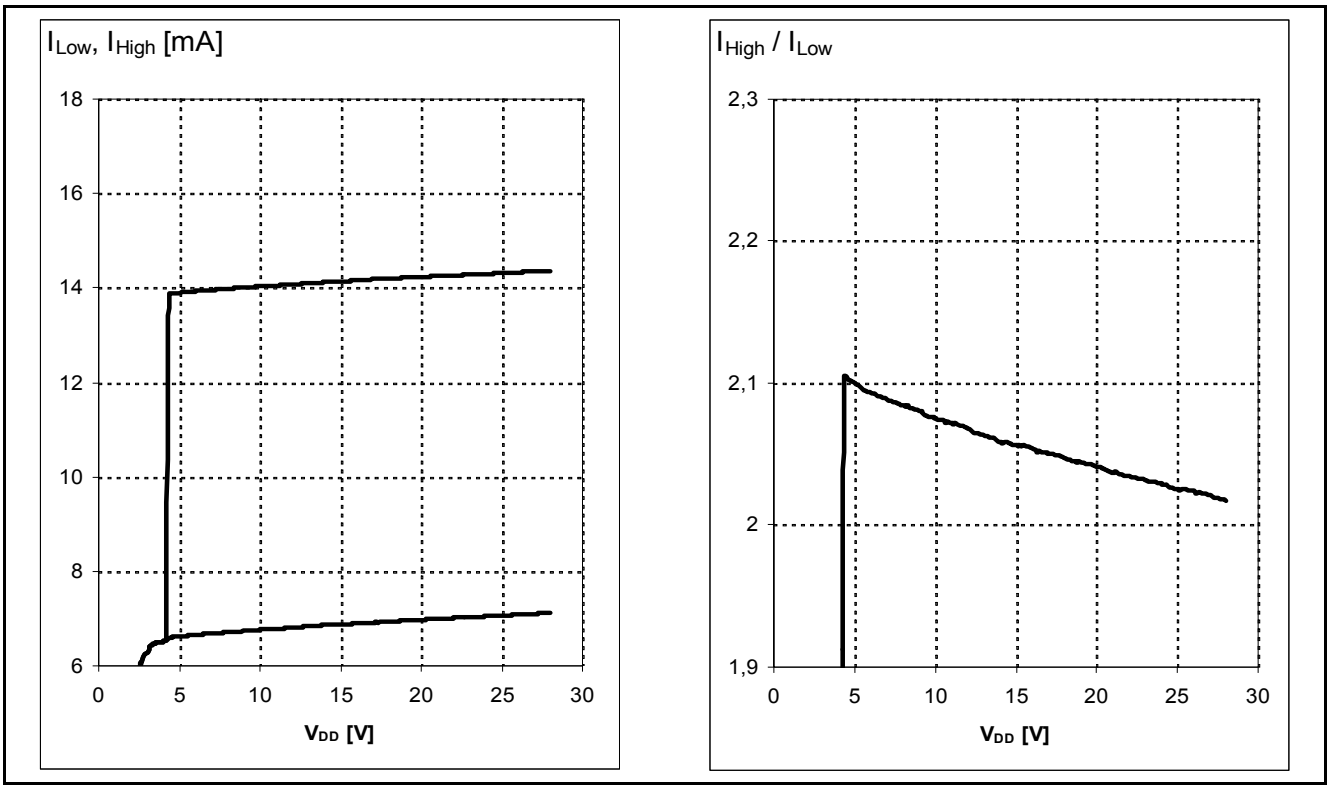


Figure 13 Supply Current =$f(V_{DD})$ (left), Supply Current Ratio $I_{high} / I_{Low} = f(V_{DD})$ (right)

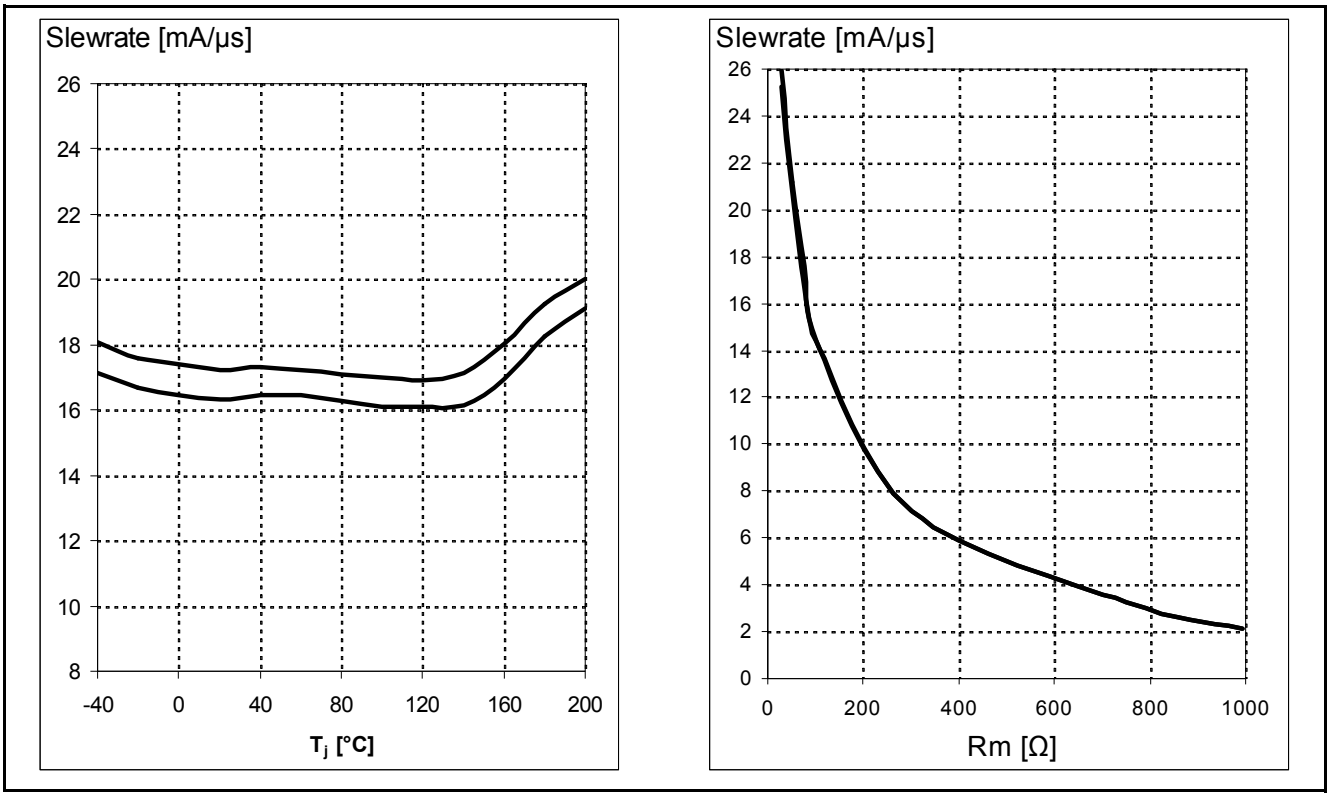


Figure 14 Slew Rate = $f(T)$, R_M = 75 Ω (left), Slew Rate = $f(R_M)$ (right)

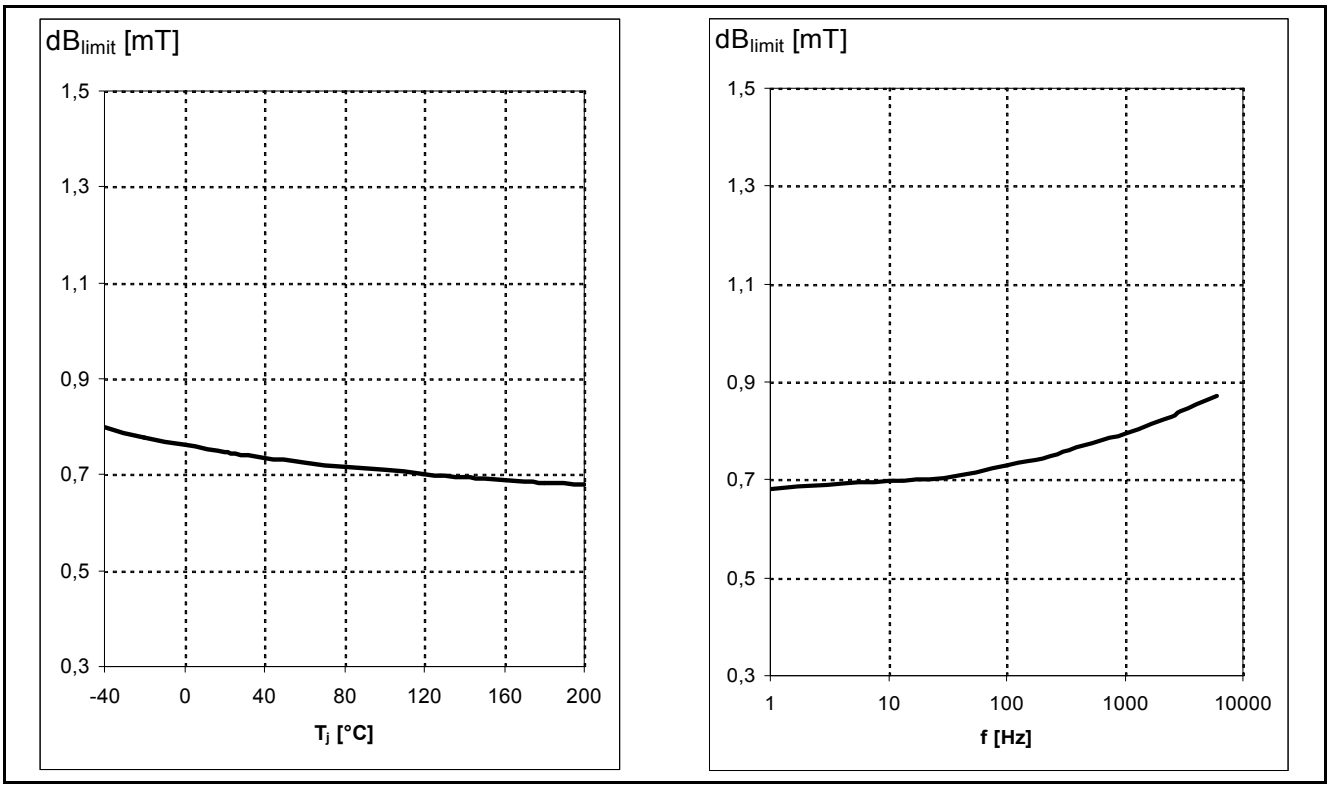


Figure 15 Magnetic Threshold ΔB_{Limit} = f(T) at f = 200Hz (left), Magnetic Threshold ΔB_{Limit} = f(f) (right)

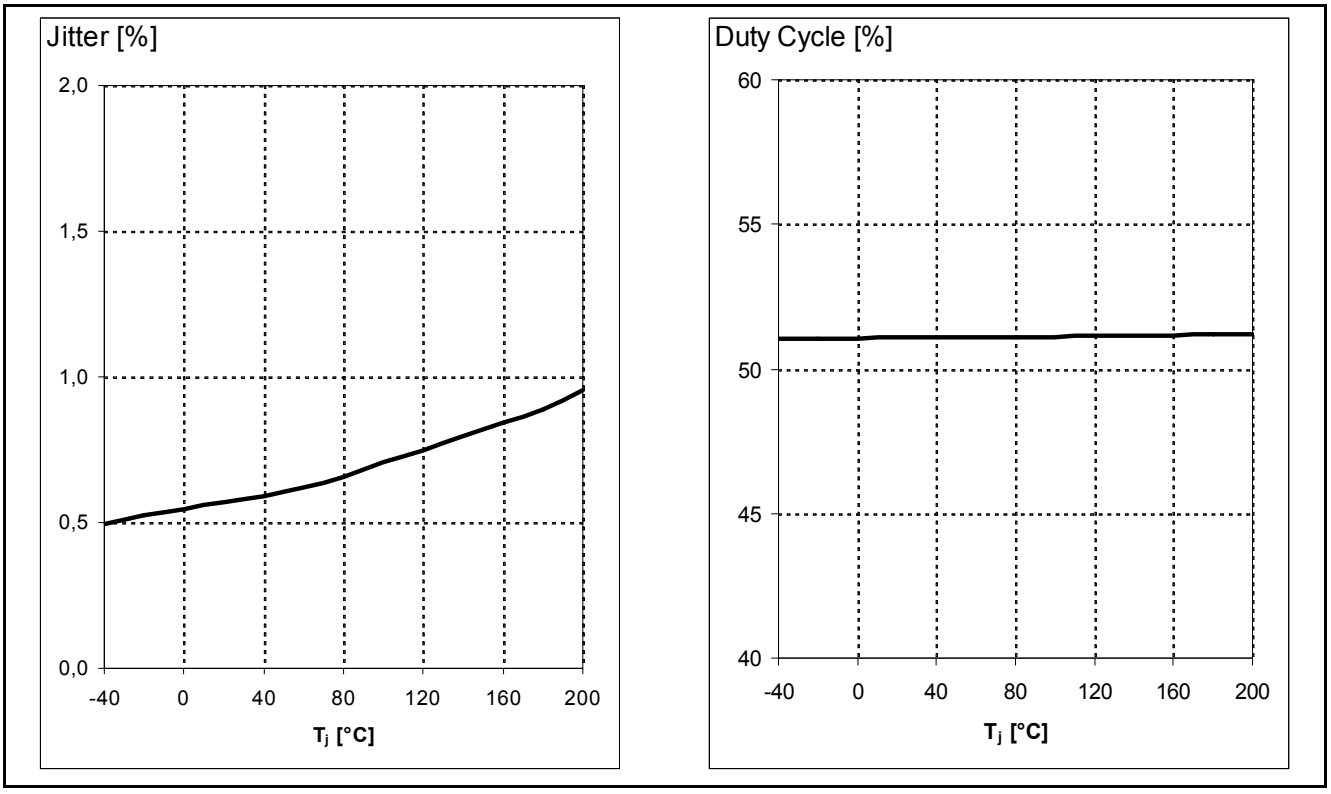


Figure 16 Jitter 1σ at ΔB = 2 mT at 1 kHz (left), Duty Cycle [%] ΔB = 2 mT at 1 kHz (right)

3.9 Electro Magnetic Compatibility (EMC)

Additional Information:

Characterization of Electro Magnetic Compatibility are carried out on sample base of one qualification lot. Not all specification parameters have been monitored during EMC exposure. Only key parameters e.g. switching current and duty cycle have been monitored.

Corresponds to Test Circuit of TLE4941/TLE4941C

Table 6 Electro Magnetic Compatibility (values depend on R_M!)

Ref. ISO 7637-1; 2000; EMC test circuit (figure 17)
ΔB = 2 mT (amplitude of sinus signal); V_{DD} = 13.5 V; f_B = 100 Hz; T = 25°C, $R_M \geq 75\ \Omega$

Parameter	Symbol	Level/Typ	Status
Testpulse 1	V_{EMC}	IV / -100 V	C
Testpulse 2[1)]		IV / 100 V	C
Testpulse 3a		IV / -150 V	A
Testpulse 3b		IV / 100 V	A
Testpulse 4		IV / -7 V	B
Testpulse 5		IV / 86.5 V	C

According to 7637-1 for test pulse 4 the test voltage shall be 12 V ± 0.2 V. Measured with R_M = 75 Ω only. Mainly the current consumption will decrease. Status C with test circuit 1.

Ref. ISO 7637-3 Release 1995 [2)]; EMC test circuit (figure 17)
ΔB = 2 mT (amplitude of sinus signal); V_{DD} = 13.5 V; f_B = 100 Hz; T = 25°C; $R_M \geq 75\ \Omega$

Parameter	Symbol	Level/Typ	Status
Testpulse 1	V_{EMC}	IV / -30 V	A
Testpulse 2		IV / 30 V	A
Testpulse 3a		IV / -60 V	A
Testpulse 3b		IV / 40 V	A

Ref. ISO 11452-3[3)]; EMC test circuit (figure 17), measured in TEM-cell
ΔB = 2 mT; V_{DD} = 13.5 V, f_B = 100 Hz; T = 25°C

Parameter	Symbol	Level/Typ	Remarks
EMC field strength	$E_{TEM-Cell}$	IV / 250 V/m	AM = 80%, f = 1 kHz

1) According to 7637-1 the supply switched “OFF” for t = 200 ms
2) Testpulse 1 and 2 are carried out with capacitive coupling even if ISO 7637-3 Testpulse 1 and 2 is not requesting for capacitive coupling clamp
3) Second edition 2001-03-01

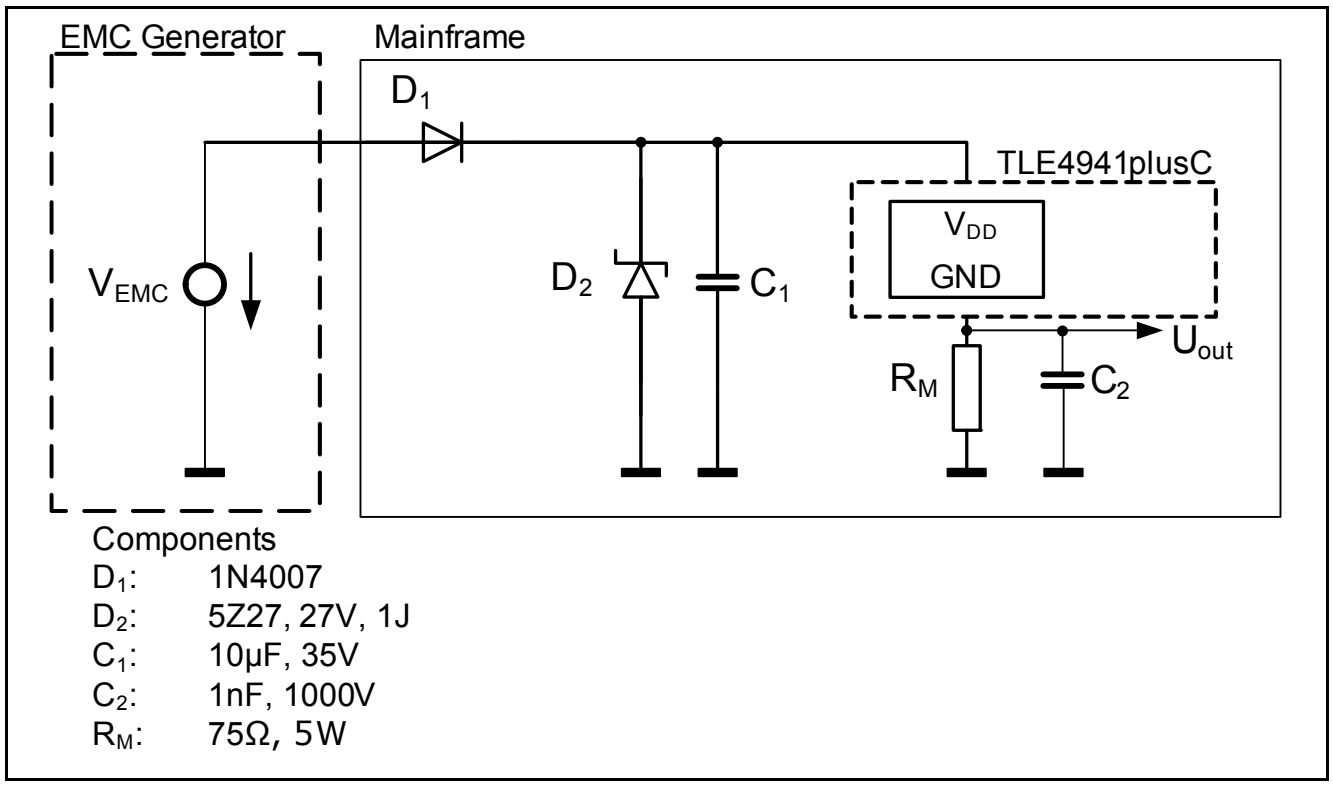


Figure 17 EMC Test Circuit

4 Package Information

Pure tin covering (green lead plating) is used. Lead frame material is K62 (UNS: C18090) and contains CuSn1CrNiTi. Product is RoHS (restriction of hazardous substances) compliant when marked with letter G in front or after the data code marking and contains a data matrix code on the back side of the package (see also information note 136/03). Please refer to your key account team or regional sales if you need further information.

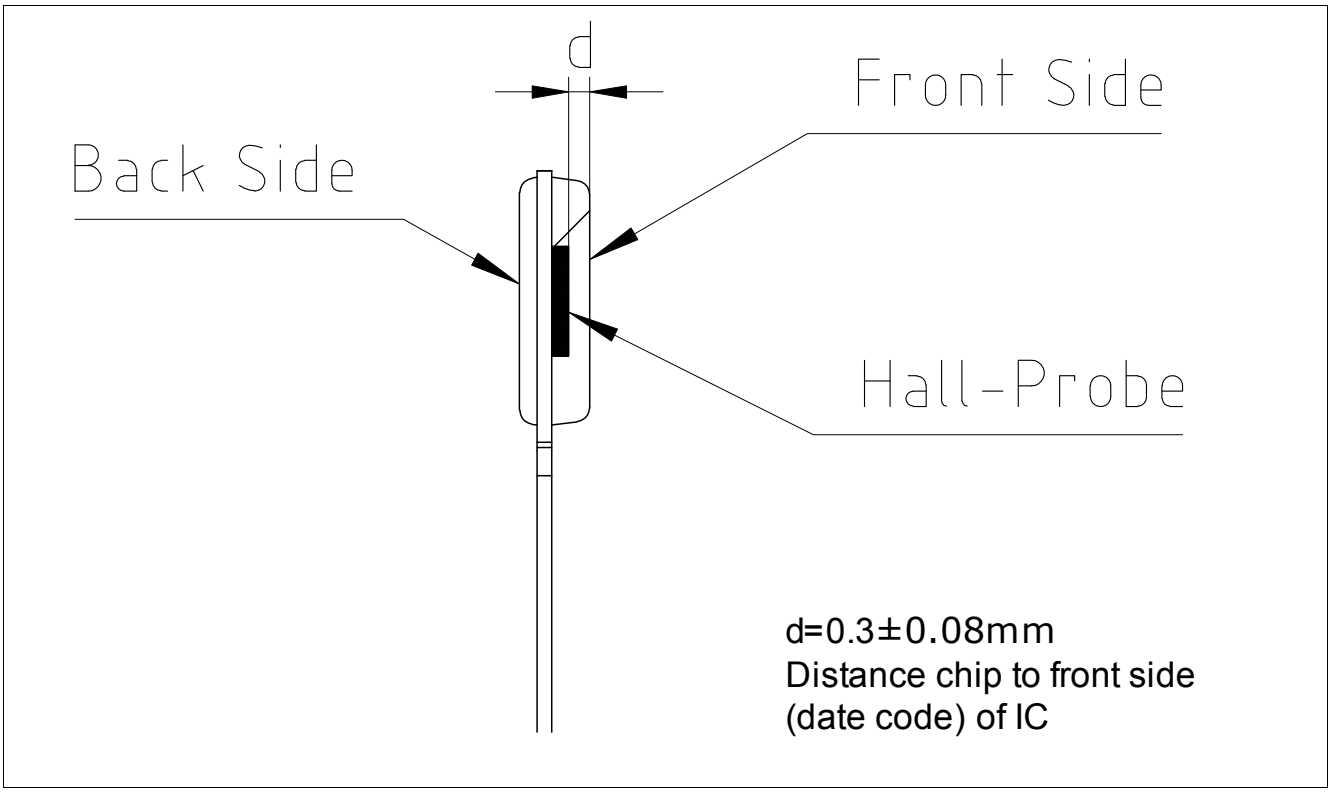


Figure 18 Distance Chip to Upper Side of IC

4.1 Lead Pull Out Force

The lead pull out force according IEC 60068-2-21 (fifth edition 1999-1) is 10N for each lead.

4.2 Packing and Package Dimensions of PG-SSO-2-53

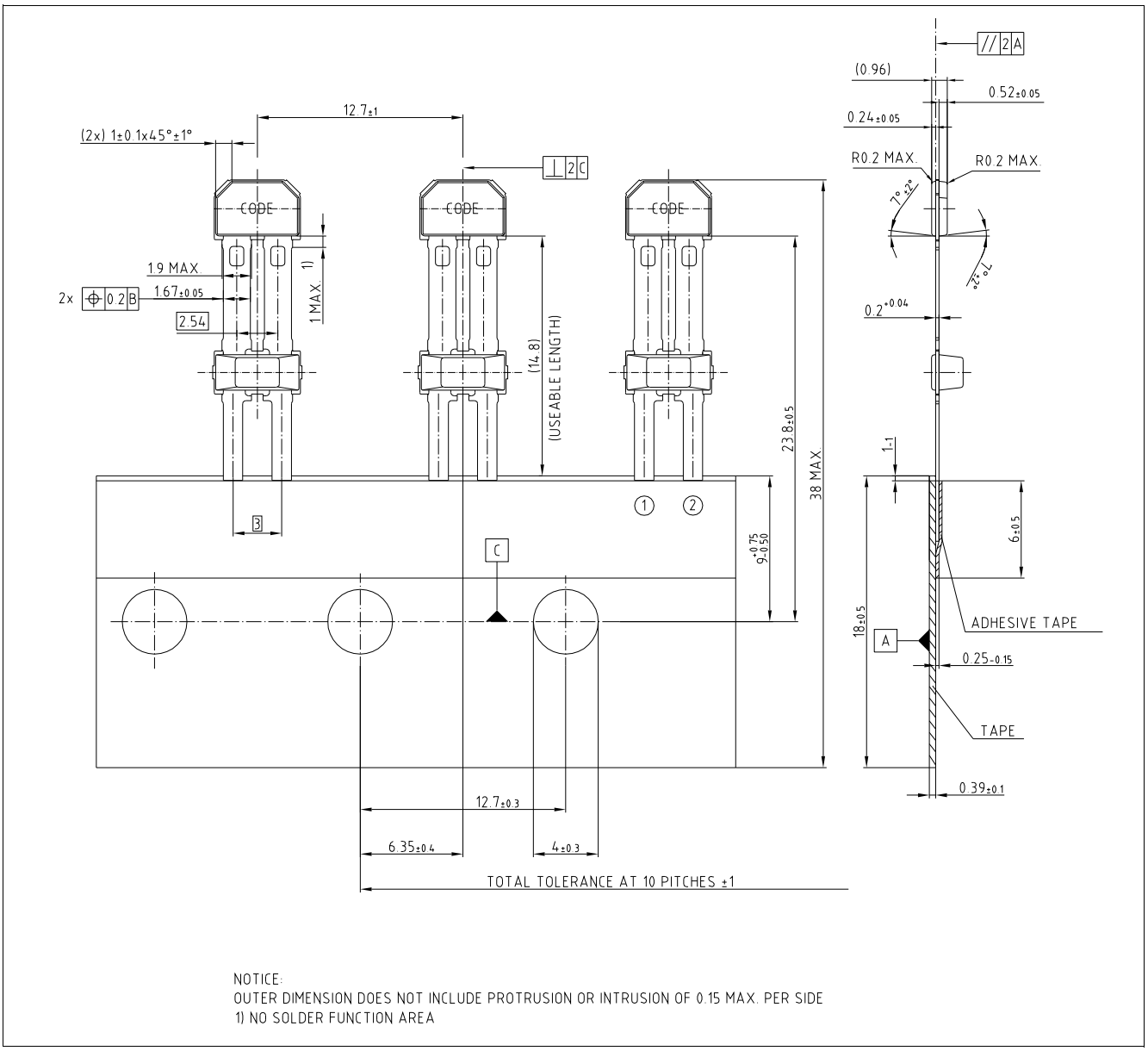


Figure 19 Packing Dimensions in mm of PG-SSO-2-53 (Plastic Single Small Outline Package)

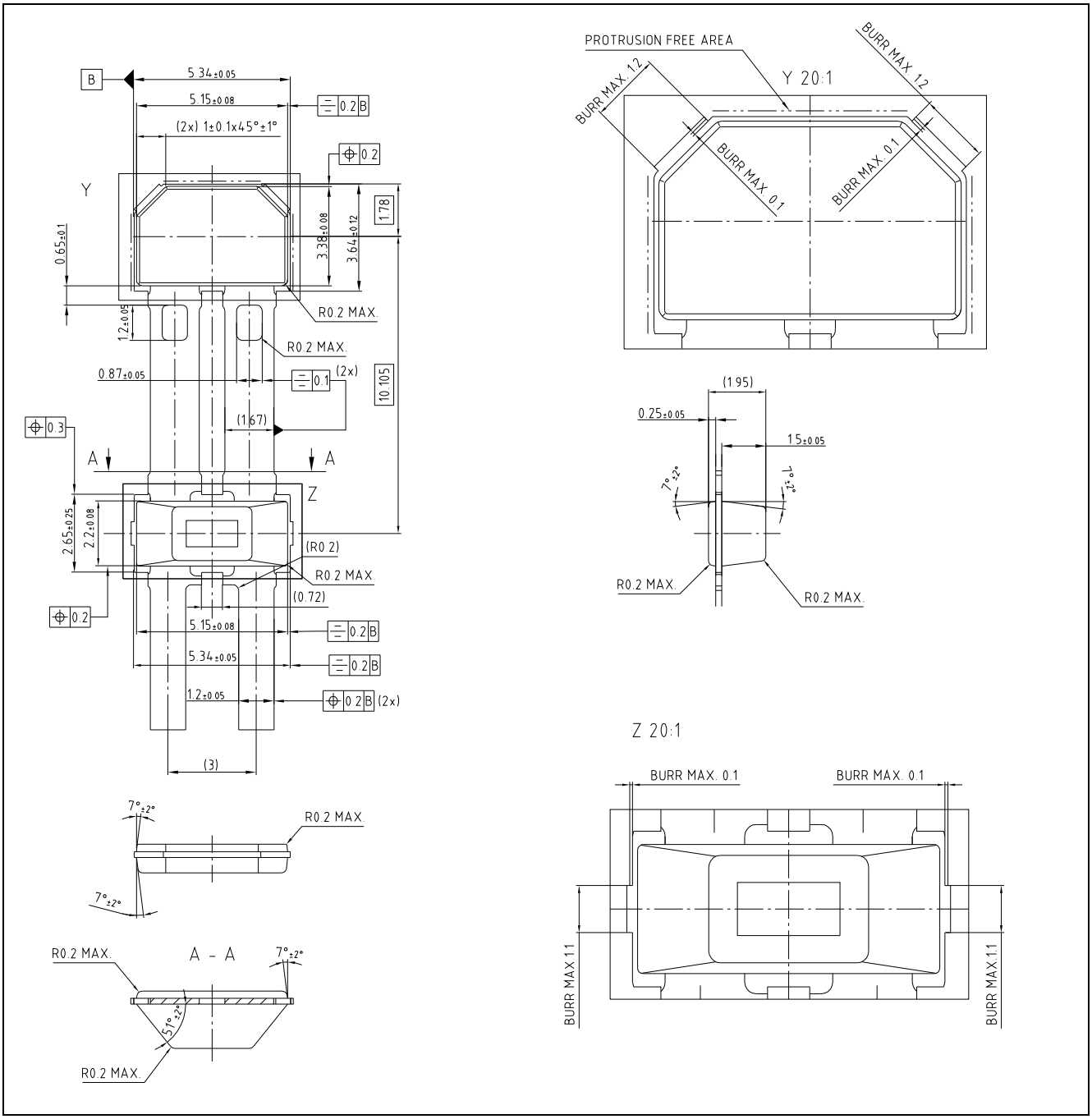


Figure 20 Package Dimensions in mm of PG-SSO-2-53 (Plastic Single Small Outline Package)

4.3 Packing

You can find all of our packages, type of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products

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