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LMZ14203HTZE/NOPB

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LMZ14203H SIMPLE SWITCHER® 6V to 42V, 3A High Output Voltage Power Module

1 Features

- Integrated Shielded Inductor
- Simple PCB Layout
- Flexible Start-Up Sequencing Using External Soft-Start and Precision Enable
- Protection Against Inrush Currents
- Input UVLO and Output Short-Circuit Protection
- –40°C to 125°C Junction Temperature Range
- Single Exposed Pad and Standard Pinout for Easy Mounting and Manufacturing
- Low Output Voltage Ripple
- Pin-to-Pin Compatible Family:
  - LMZ14203H/2H/1H (42 V Maximum, 3-A, 2-A, 1-A)
  - LMZ14203/2/1 (4 2V Maximum, 3-A, 2-A, 1-A)
  - LMZ12003/2/1 (20 V Maximum, 3-A, 2-A, 1-A)
- Fully Enabled for WEBENCH® Power Designer
- Electrical Specifications
  - Up to 3-A Output Current
  - Input Voltage Range 6 V to 42 V
  - Output Voltage as Low as 5 V
  - Efficiency up to 97%
- Performance Benefits
  - High Efficiency Reduces System Heat Generation
  - Low Radiated EMI (EN 55022 Class B Tested)
  - No Compensation Required
  - Low Package Thermal Resistance

NOTE: EN 55022:2006, +A1:2007, FCC Part 15 Subpart B: 2007

2 Applications

- Intermediate Bus Conversions to 12-V and 24-V Rail
- Time-Critical Projects
- Space Constrained and High Thermal Requirement Applications
- Negative Output Voltage Applications

3 Description

The LMZ14203H SIMPLE SWITCHER® power module is an easy-to-use step-down DC-DC solution that can drive up to 3-A load with exceptional power conversion efficiency, line and load regulation, and output accuracy. The LMZ14203H is available in an innovative package that enhances thermal performance and allows for hand or machine soldering.

The LMZ14203H can accept an input voltage rail between 6 V and 42 V and deliver an adjustable and highly accurate output voltage as low as 5 V. The LMZ14203H only requires three external resistors and four external capacitors to complete the power solution. The LMZ14203H is a reliable and robust design with the following protection features: thermal shutdown, input undervoltage lockout, output overvoltage protection, short-circuit protection, output current limit, and allows start-up into a prebiased output. A single resistor adjusts the switching frequency up to 1 MHz.

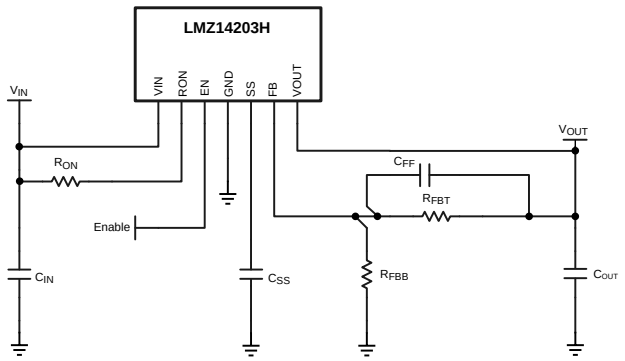
Device Information(1)(2)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMZ14203H	TO-PMOD (7)	10.16 mm × 9.85 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Peak reflow temperature equals 245°C. See SNAA214 for more details.

Simplified Application Schematic



Efficiency V_{OUT} = 12 V, T_A = 25°C

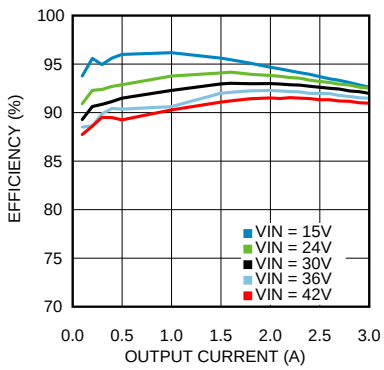


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (August 2015) to Revision G	Page
• Added this new bullet to the Power Module SMT Guidelines section	22

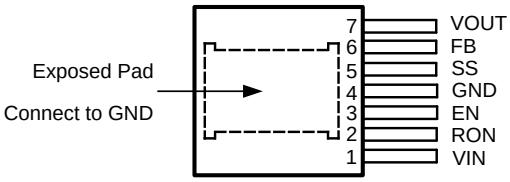
Changes from Revision E (June 2015) to Revision F	Page
• Changed the title of the document	1

Changes from Revision D (October 2013) to Revision E	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision C (June 2011) to Revision D	Page
• Added Peak Reflow Case Temp = 245°C	1
• Changed 10 mils	21
• Added Power Module SMT Guidelines	21

5 Pin Configuration and Functions

NDW Package
7-Pin TO-PMOD
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VIN	Power	Supply input — Additional external input capacitance is required between this pin and the exposed pad (EP).
2	RON	Analog	ON-time resistor — An external resistor from V_{IN} to this pin sets the ON-time and frequency of the application. Typical values range from 100k to 700k ohms.
3	EN	Analog	Enable — Input to the precision enable comparator. Rising threshold is 1.18 V.
4	GND	Ground	Ground — Reference point for all stated voltages. Must be externally connected to EP.
5	SS	Analog	Soft-Start — An internal 8-µA current source charges an external capacitor to produce the soft-start function.
6	FB	Analog	Feedback — Internally connected to the regulation, overvoltage, and short-circuit comparators. The regulation reference point is 0.8 V at this input pin. Connect the feedback resistor divider between the output and ground to set the output voltage.
7	VOUT	Power	Output Voltage — Output from the internal inductor. Connect the output capacitor between this pin and the EP.
—	EP	Ground	Exposed Pad — Internally connected to pin 4. Used to dissipate heat from the package during operation. Must be electrically connected to pin 4 external to the package.

6 Specifications

6.1 Absolute Maximum Ratings (1)(2)(3)

	MIN	MAX	UNIT
VIN, RON to GND	–0.3	43.5	V
EN, FB, SS to GND	–0.3	7	V
Junction Temperature		150	°C
Peak Reflow Case Temperature (30 s)		245	°C
Storage Temperature	–65	150	°C

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(2) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(3) For soldering specifications, see the application note *Absolute Maximum Ratings for Soldering* (SNOA549)

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
V_{IN}	6	42	V
EN	0	6.5	V
Operation Junction Temperature	−40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)			LMZ14203H NDW (TO-PMOD) 7 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	4 layer printed-circuit-board, 7.62 cm x 7.62 cm (3 in x 3 in) area, 1-oz copper, no air flow	16	°C/W
		4 layer printed-circuit-board, 6.35 cm x 6.35 cm (2.5 in x 2.5 in) area, 1-oz copper, no air flow	18.4	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		1.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Minimum and Maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 24 V, V_{OUT} = 12 V, R_{ON} = 249 kΩ

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
SYSTEM PARAMETERS						
ENABLE CONTROL						
V_{EN}	EN threshold trip point	V_{EN} rising, T_J = –40°C to 125°C	1.10	1.18	1.25	V
V_{EN-HYS}	EN threshold hysteresis			90		mV
SOFT-START						
I_{SS}	SS source current	V_{SS} = 0 V, T_J = –40°C to 125°C	8	10	15	µA
I_{SS-DIS}	SS discharge current			–200		µA
CURRENT LIMIT						
I_{CL}	Current limit threshold	DC average, T_J = –40°C to 125°C	3.2	4.7	5.5	A
VIN UVLO						
VIN_{UVLO}	Input UVLO	EN pin floating V_{IN} rising		3.75		V
$VIN_{UVLO-HYST}$	Hysteresis	EN pin floating V_{IN} falling		130		mV
ON/OFF TIMER						
t_{ON-MIN}	ON timer minimum pulse width			150		ns
t_{OFF}	OFF timer pulse width			260		ns

(1) Minimum and Maximum limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.

Electrical Characteristics (continued)

Minimum and Maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 24 V, V_{OUT} = 12 V, R_{ON} = 249 kΩ

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
REGULATION AND OVERVOLTAGE COMPARATOR						
V_{FB}	In-regulation feedback voltage	V_{IN} = 24 V, V_{OUT} = 12 V V_{SS} >+ 0.8 V T_J = –40°C to 125°C I_{OUT} = 10 mA to 3 A	0.782	0.803	0.822	V
		V_{IN} = 24 V, V_{OUT} = 12 V V_{SS} >+ 0.8 V T_J = 25°C I_{OUT} = 10 mA to 3 A	0.786	0.803	0.818	
V_{FB}	In-regulation feedback voltage	V_{IN} = 36 V, V_{OUT} = 24 V V_{SS} >+ 0.8 V T_J = –40°C to 125°C I_{OUT} = 10 mA to 3 A	0.780	0.803	0.826	V
		V_{IN} = 36 V, V_{OUT} = 24 V V_{SS} >+ 0.8 V T_J = 25°C I_{OUT} = 10 mA to 3 A	0.787	0.803	0.819	
V_{FB-OVP}	Feedback overvoltage protection threshold			0.92		V
I_{FB}	Feedback input bias current			5		nA
I_Q	Nonswitching Input Current	V_{FB}= 0.86 V		1		mA
I_{SD}	Shutdown quiescent current	V_{EN}= 0 V		25		µA
THERMAL CHARACTERISTICS						
T_{SD}	Thermal shutdown (rising)			165		°C
$T_{SD-HYST}$	Thermal shutdown hysteresis			15		°C
PERFORMANCE PARAMETERS						
ΔV_{OUT}	Output Voltage Ripple	V_{OUT} = 5 V, C_O = 100-µF 6.3-V X7R		8		mV_{PP}
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN} = 16 V to 42 V, I_{OUT}= 3 A		0.01%		
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	V_{IN} = 24 V, I_{OUT} = 0 A to 3 A		1.5		mV/A
η	Efficiency	V_{IN} = 24 V, V_{OUT} = 12 V, I_{OUT} = 1 A		94%		
η	Efficiency	V_{IN} = 24 V, V_O = 12 V, I_O = 3 A		93%		

6.6 Typical Characteristics

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; Cin = 10-uF X7R Ceramic; C_O = 47 uF; T_A = 25°C.

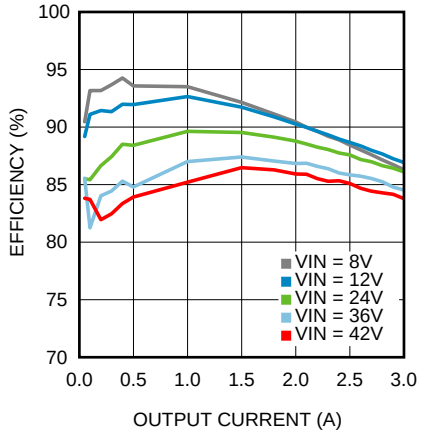


Figure 1. Efficiency V_{OUT} = 5 V, T_A = 25°C

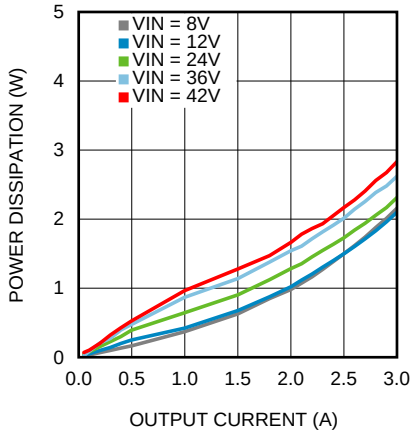


Figure 2. Power Dissipation V_{OUT} = 5 V, T_A = 25°C

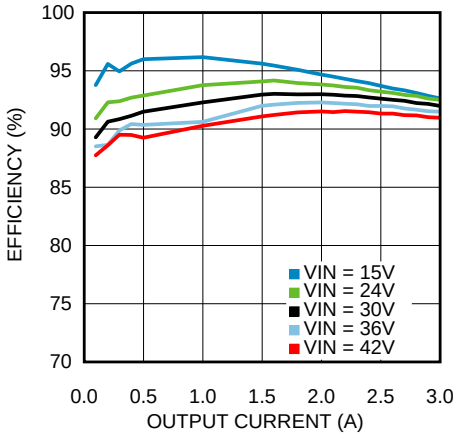


Figure 3. Efficiency V_{OUT} = 12 V, T_A = 25°C

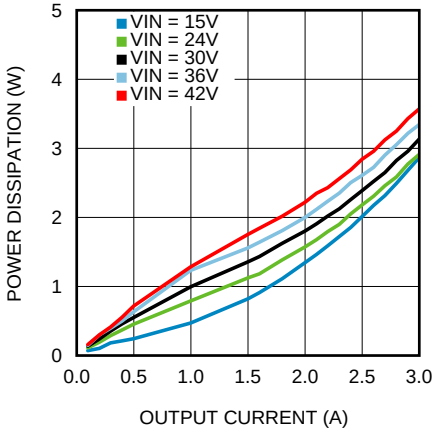


Figure 4. Power Dissipation V_{OUT} = 12 V, T_A = 25°C

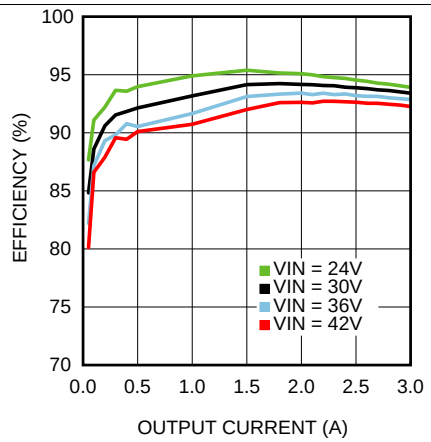


Figure 5. Efficiency V_{OUT} = 15 V, T_A = 25°C

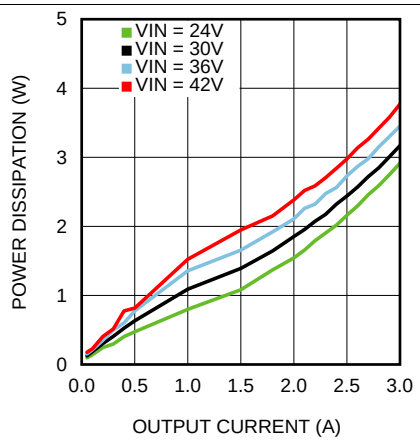


Figure 6. Power Dissipation V_{OUT} = 15 V, T_A = 25°C

Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; Cin = 10-uF X7R Ceramic; C_O = 47 uF; T_A = 25°C.

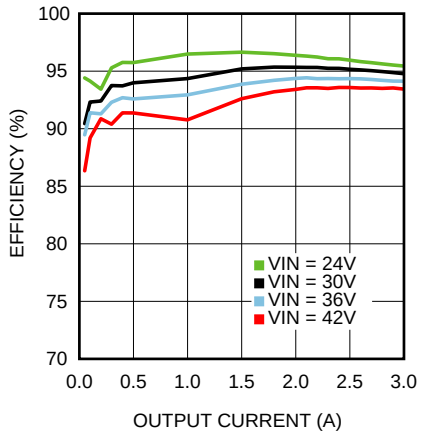


Figure 7. Efficiency V_{OUT} = 18 V, T_A = 25°C

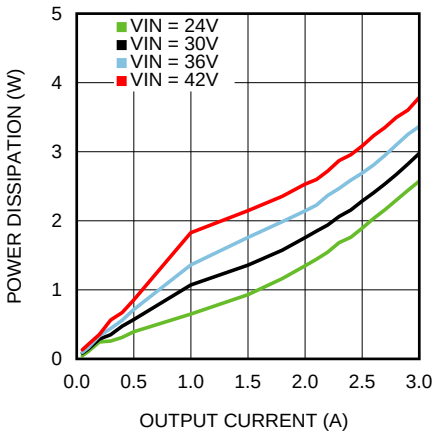


Figure 8. Power Dissipation V_{OUT} = 18 V, T_A = 25°C

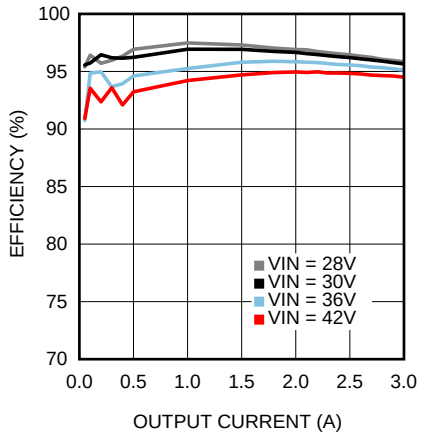


Figure 9. Efficiency V_{OUT} = 24 V, T_A = 25°C

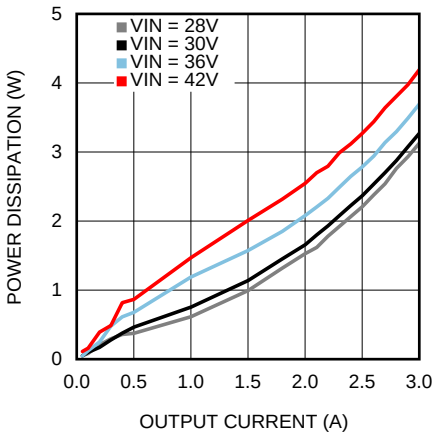


Figure 10. Power Dissipation V_{OUT} = 24 V, T_A = 25°C

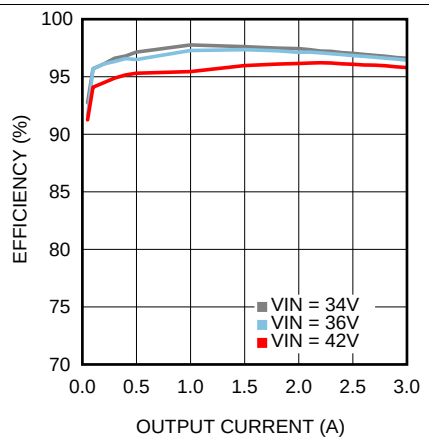


Figure 11. Efficiency V_{OUT} = 30 V, T_A = 25°C

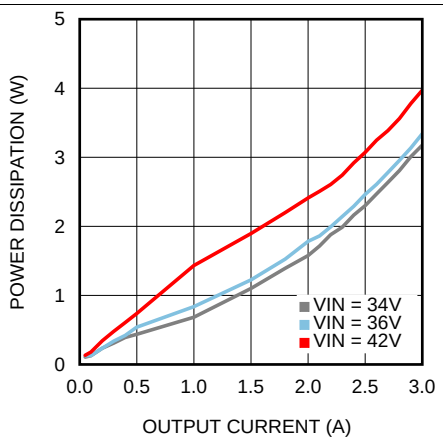


Figure 12. Power Dissipation V_{OUT} = 30 V, T_A = 25°C

Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; Cin = 10-uF X7R Ceramic; C_O = 47 uF; T_A = 25°C.

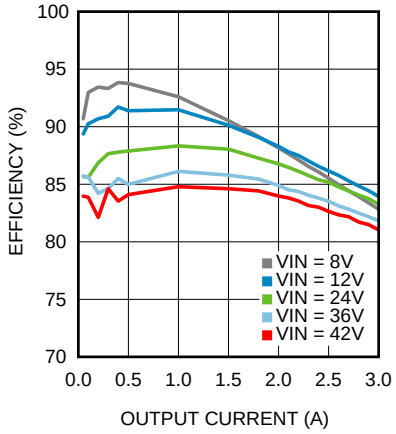


Figure 13. Efficiency V_{OUT} = 5 V, T_A = 85°C

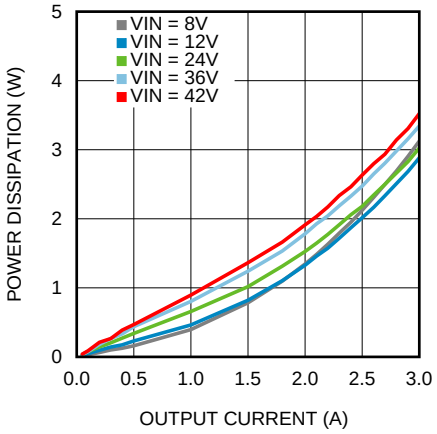


Figure 14. Power Dissipation V_{OUT} = 5 V, T_A = 85°C

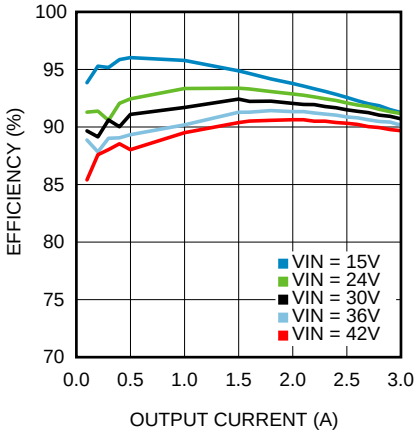


Figure 15. Efficiency V_{OUT} = 12 V, T_A = 85°C

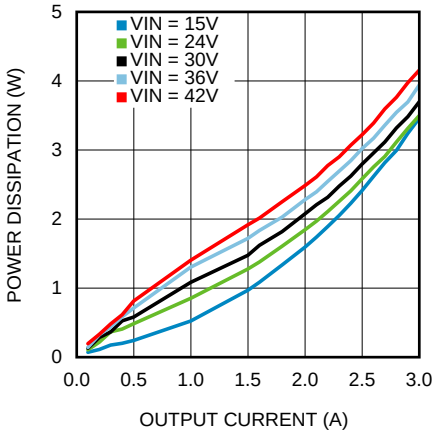


Figure 16. Power Dissipation V_{OUT} = 12 V, T_A = 85°C

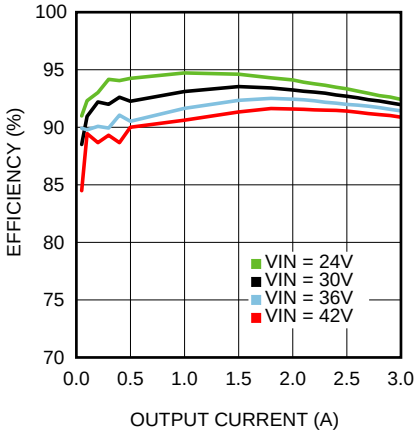


Figure 17. Efficiency V_{OUT} = 15 V, T_A = 85°C

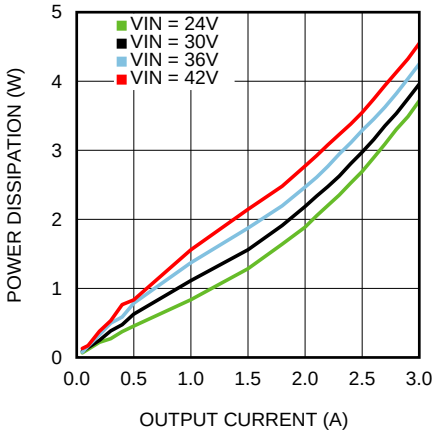


Figure 18. Power Dissipation V_{OUT} = 15 V, T_A = 85°C

Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; Cin = 10-uF X7R Ceramic; C_O = 47 uF; T_A = 25°C.

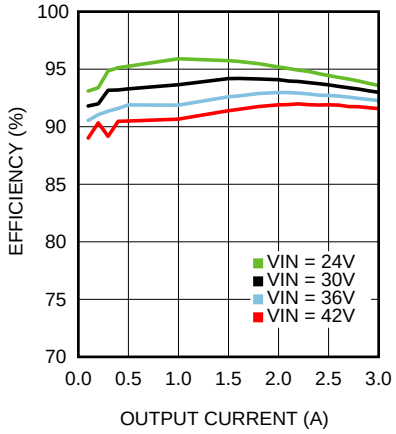


Figure 19. Efficiency V_{OUT} = 18 V, T_A = 85°C

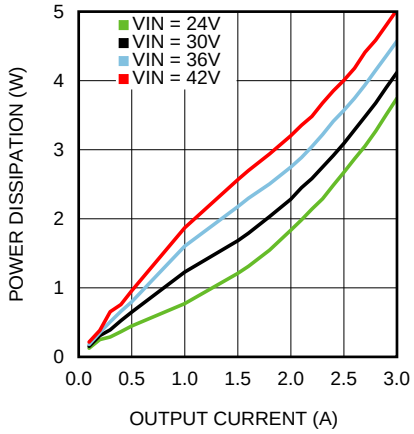


Figure 20. Power Dissipation V_{OUT} = 18 V, T_A = 85°C

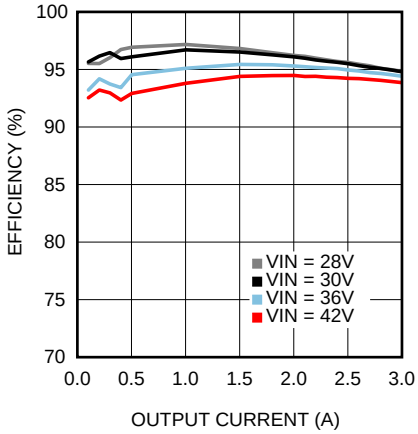


Figure 21. Efficiency V_{OUT} = 24 V, T_A = 85°C

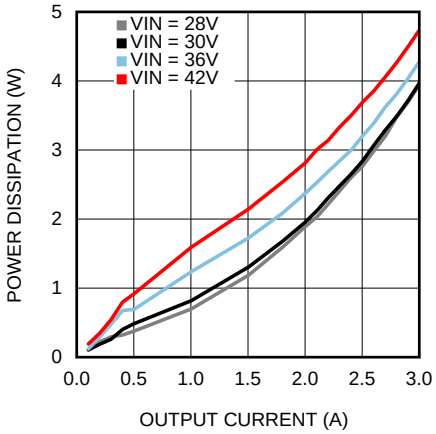


Figure 22. Power Dissipation V_{OUT} = 24 V, T_A = 85°C

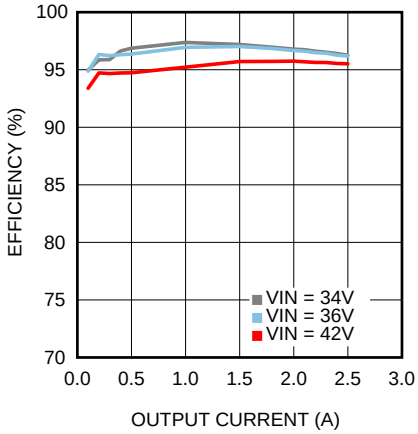


Figure 23. Efficiency V_{OUT} = 30 V, T_A = 85°C

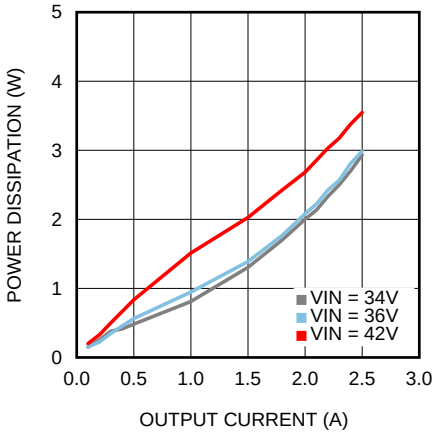


Figure 24. Power Dissipation V_{OUT} = 30 V, T_A = 85°C

Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; Cin = 10-uF X7R Ceramic; C_O = 47 uF; T_A = 25°C.

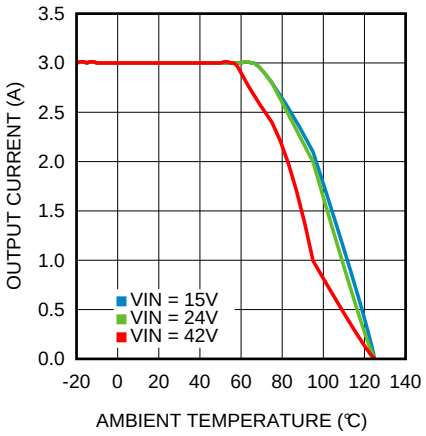


Figure 25. Thermal Derating V_{OUT} = 12 V, $R_{\theta JA}$ = 16°C/W

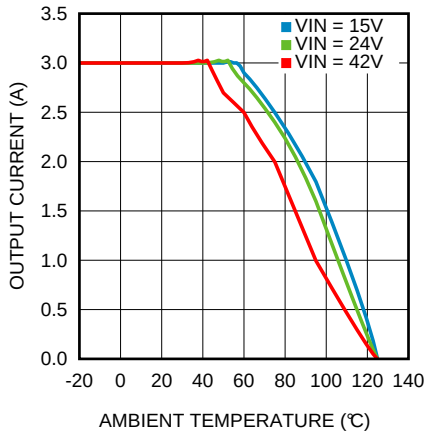


Figure 26. Thermal Derating V_{OUT} = 12 V, $R_{\theta JA}$ = 20°C/W

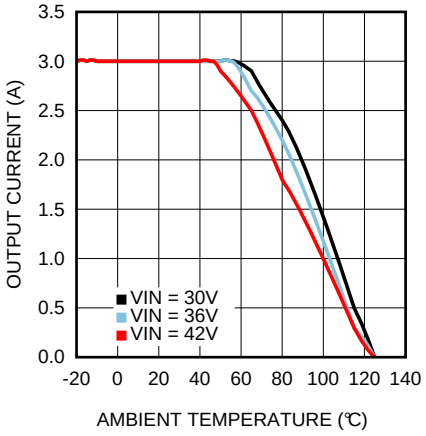


Figure 27. Thermal Derating V_{OUT} = 24 V, $R_{\theta JA}$ = 16°C/W

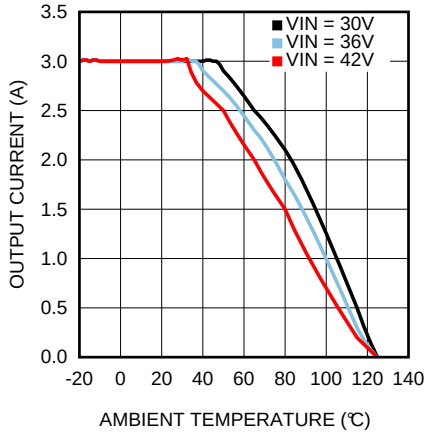


Figure 28. Thermal Derating V_{OUT} = 24 V, $R_{\theta JA}$ = 20°C/W

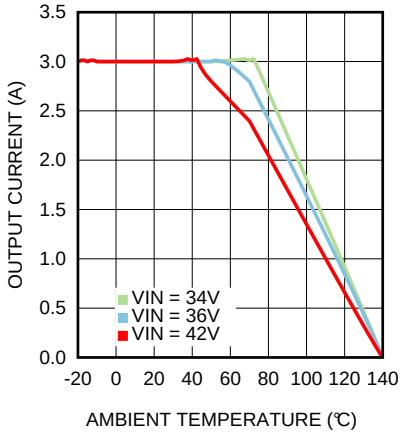


Figure 29. Thermal Derating V_{OUT} = 30 V, $R_{\theta JA}$ = 16°C/W

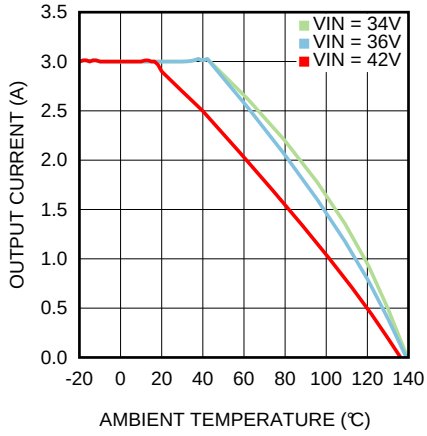


Figure 30. Thermal Derating V_{OUT} = 30 V, $R_{\theta JA}$ = 20°C/W

Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; Cin = 10-uF X7R Ceramic; C_O = 47 uF; T_A = 25°C.

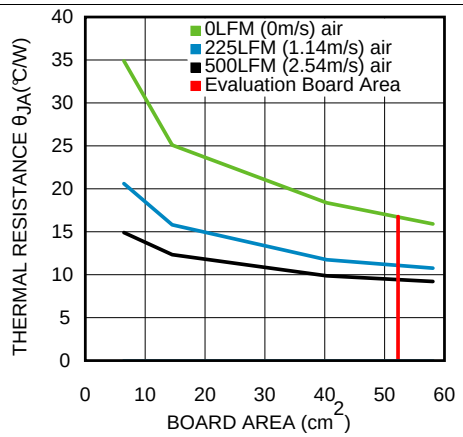


Figure 31. Package Thermal Resistance $R_{\theta JA}$ 4-Layer Printed-Circuit-Board With 1-oz Copper

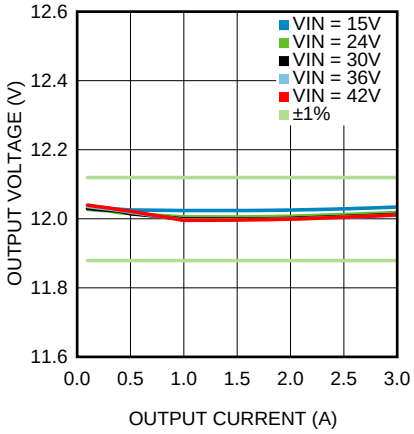


Figure 32. Line and Load Regulation T_A = 25°C

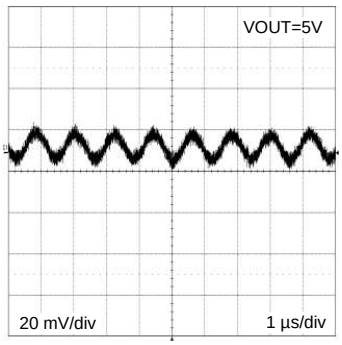


Figure 33. Output Ripple V_{IN} = 12 V, I_{OUT} = 3 A, Ceramic C_{OUT}, BW = 200 MHz

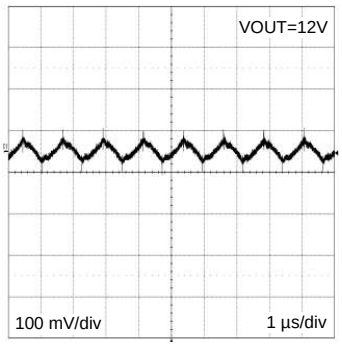


Figure 34. Output Ripple V_{IN} = 24 V, I_{OUT} = 3 A, Polymer Electrolytic C_{OUT}, BW = 200 MHz

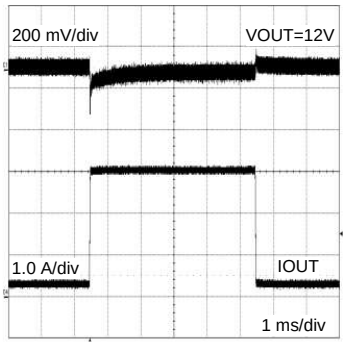


Figure 35. Load Transient Response V_{IN} = 24 V, V_{OUT} = 12 V Load Step From 10% to 100%

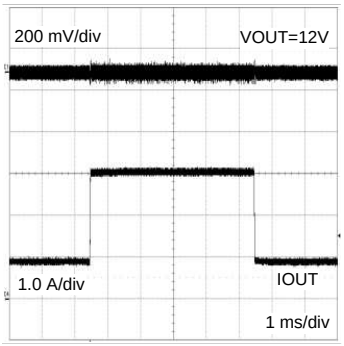


Figure 36. Load Transient Response V_{IN} = 24 V, V_{OUT} = 12 V Load Step From 30% to 100%

Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; Cin = 10-uF X7R Ceramic; C_O = 47 uF; T_A = 25°C.

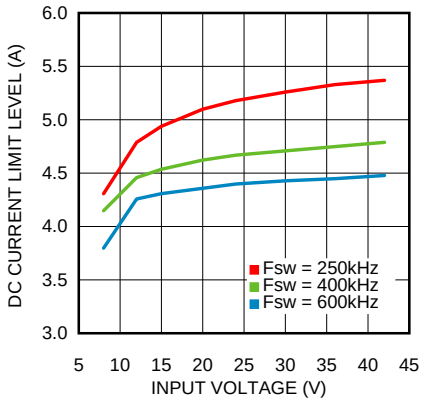


Figure 37. Current Limit vs Input Voltage
V_{OUT} = 5 V

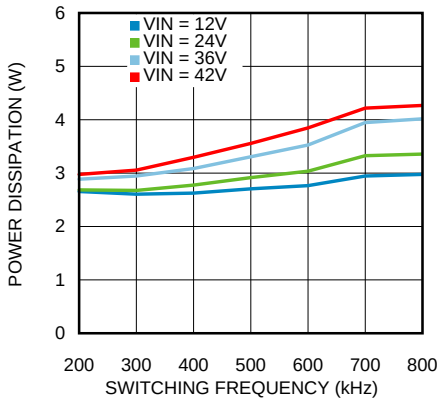


Figure 38. Switching Frequency vs Power Dissipation
V_{OUT} = 5 V

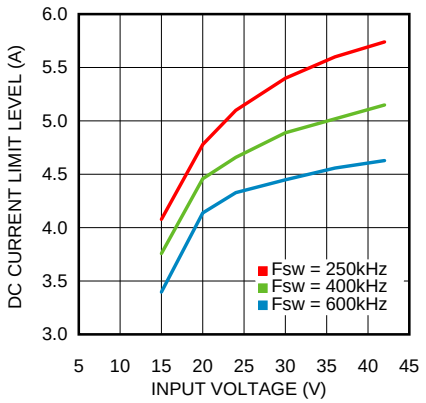


Figure 39. Current Limit vs Input Voltage
V_{OUT} = 12 V

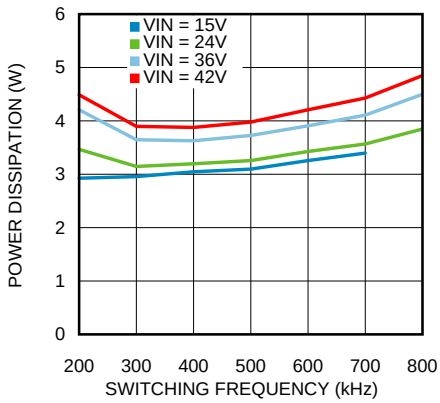


Figure 40. Switching Frequency vs Power Dissipation
V_{OUT} = 12 V

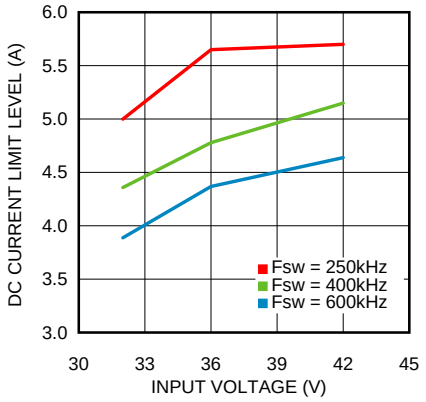


Figure 41. Current Limit vs Input Voltage
V_{OUT} = 24 V

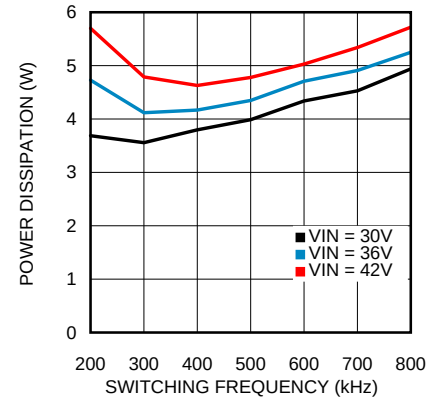


Figure 42. Switching Frequency vs Power Dissipation
V_{OUT} = 24 V

Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; Cin = 10-uF X7R Ceramic; C_O = 47 uF; T_A = 25°C.

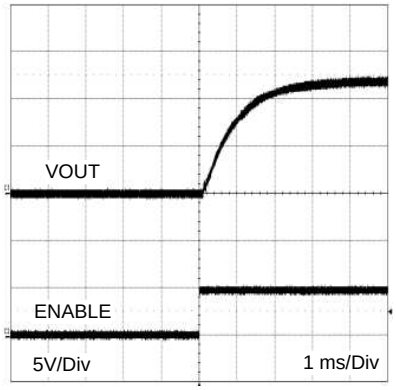


Figure 43. Startup
V_{IN} = 24 V, I_{OUT} = 3 A

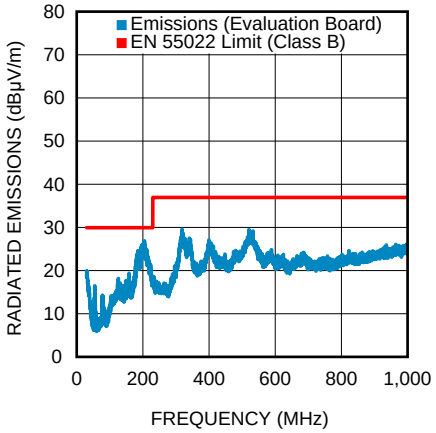


Figure 44. Radiated EMI of Evaluation Board, V_{OUT} = 12 V

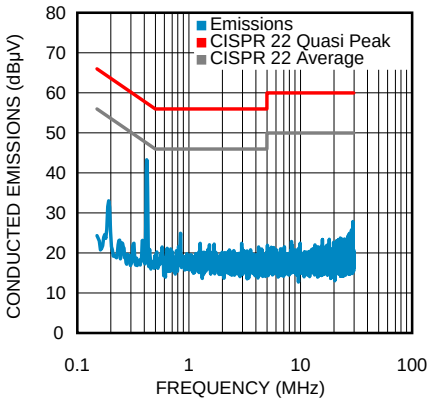


Figure 45. Conducted EMI, V_{OUT} = 12 V
Evaluation Board BOM and 3.3 µH 2x10 µF LC Line Filter

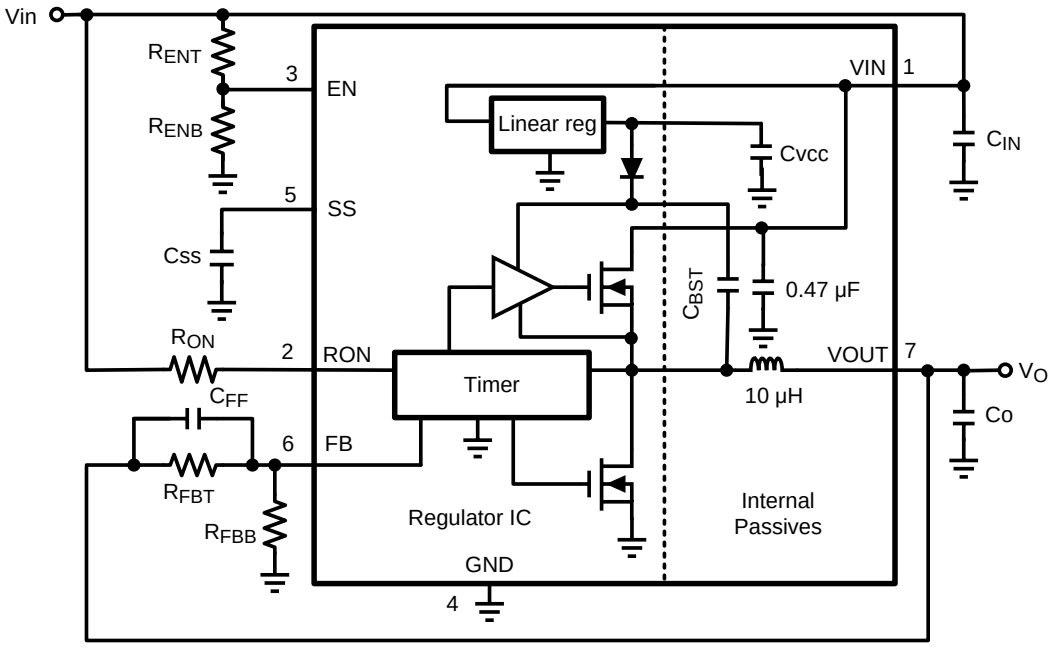
7 Detailed Description

7.1 Overview

7.1.1 COT Control Circuit Overview

Constant ON-time control is based on a comparator and an ON-time one-shot, with the output voltage feedback compared to an internal 0.8-V reference. If the feedback voltage is below the reference, the high-side MOSFET is turned on for a fixed ON-time determined by a programming resistor R_{ON}. R_{ON} is connected to V_{IN} such that ON-time is reduced with increasing input supply voltage. Following this ON-time, the high-side MOSFET remains off for a minimum of 260 ns. If the voltage on the feedback pin falls below the reference level again the ON-time cycle is repeated. Regulation is achieved in this manner.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Overvoltage Comparator

The voltage at FB is compared to a 0.92-V internal reference. If FB rises above 0.92 V the ON-time is immediately terminated. This condition is known as overvoltage protection (OVP). It can occur if the input voltage is increased very suddenly or if the output load is decreased very suddenly. Once OVP is activated, the top MOSFET ON-times will be inhibited until the condition clears. Additionally, the synchronous MOSFET will remain on until inductor current falls to zero.

7.3.2 Current Limit

Current limit detection is carried out during the OFF-time by monitoring the current in the synchronous MOSFET. Referring to the *Functional Block Diagram*, when the top MOSFET is turned off, the inductor current flows through the load, the PGND pin and the internal synchronous MOSFET. If this current exceeds 4.2 A (typical) the current limit comparator disables the start of the next ON-time period. The next switching cycle will occur only if the FB input is less than 0.8 V and the inductor current has decreased below 4.2 A. Inductor current is monitored during the period of time the synchronous MOSFET is conducting. So long as inductor current exceeds 4.2 A, further ON-time intervals for the top MOSFET will not occur. Switching frequency is lower during current limit due to the longer OFF-time.

Feature Description (continued)

NOTE

The DC current limit varies with duty cycle, switching frequency, and temperature.

7.3.3 Thermal Protection

The junction temperature of the LMZ14203H should not be allowed to exceed its maximum ratings. Thermal protection is implemented by an internal Thermal Shutdown circuit which activates at 165 °C (typical) causing the device to enter a low power standby state. In this state the main MOSFET remains off causing V_O to fall, and additionally the CSS capacitor is discharged to ground. Thermal protection helps prevent catastrophic failures for accidental device overheating. When the junction temperature falls back below 145 °C (typical Hyst = 20 °C) the SS pin is released, V_O rises smoothly, and normal operation resumes.

7.3.4 Zero Coil Current Detection

The current of the lower (synchronous) MOSFET is monitored by a zero coil current detection circuit which inhibits the synchronous MOSFET when its current reaches zero until the next ON-time. This circuit enables the DCM operating mode, which improves efficiency at light loads.

7.3.5 Prebiased Startup

The LMZ14203H will properly start up into a prebiased output. This startup situation is common in multiple rail logic applications where current paths may exist between different power rails during the startup sequence. The prebias level of the output voltage must be less than the input UVLO set point. This will prevent the output pre-bias from enabling the regulator through the high-side MOSFET body diode.

7.4 Device Functional Modes

7.4.1 Discontinuous Conduction and Continuous Conduction Modes

At light-load, the regulator will operate in discontinuous conduction mode (DCM). With load currents above the critical conduction point, it will operate in continuous conduction mode (CCM). When operating in DCM the switching cycle begins at zero amps inductor current; increases up to a peak value, and then recedes back to zero before the end of the OFF-time. During the period of time that inductor current is zero, all load current is supplied by the output capacitor. The next ON-time period starts when the voltage on the FB pin falls below the internal reference. The switching frequency is lower in DCM and varies more with load current as compared to CCM. Conversion efficiency in DCM is maintained since conduction and switching losses are reduced with the smaller load and lower switching frequency.

8 Application and Implementation

NOTE

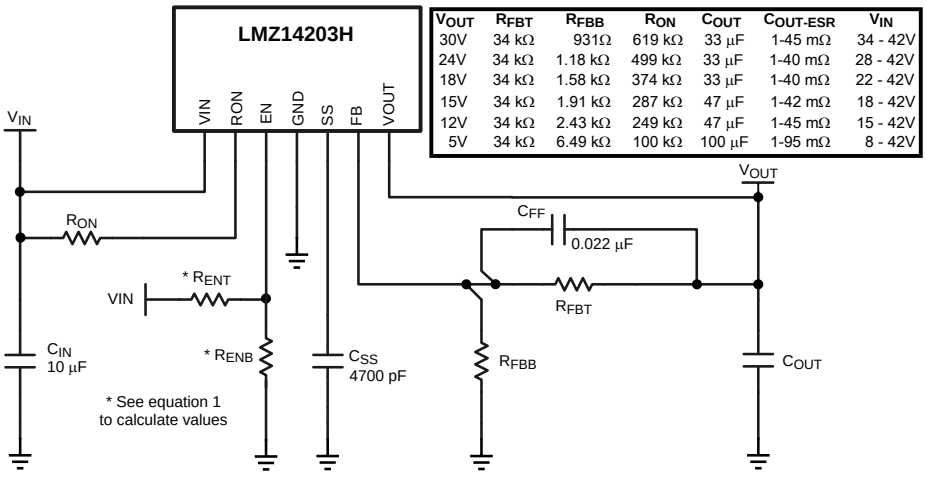
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMZ14203H is a step down DC-to-DC power module. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 3 A. The following design procedure can be used to select components for the LMZ14203H. Alternately, the WEBENCH software may be used to generate complete designs.

When generating a design, the WEBENCH software uses iterative design procedure and accesses comprehensive databases of components. For more details, go to www.ti.com.

8.2 Typical Application



VOUT	RFBT	RFBB	RON	COUT	COUT-ESR	VIN
30V	34 kΩ	931Ω	619 kΩ	33 µF	1-45 mΩ	34 - 42V
24V	34 kΩ	1.18 kΩ	499 kΩ	33 µF	1-40 mΩ	28 - 42V
18V	34 kΩ	1.58 kΩ	374 kΩ	33 µF	1-40 mΩ	22 - 42V
15V	34 kΩ	1.91 kΩ	287 kΩ	47 µF	1-42 mΩ	18 - 42V
12V	34 kΩ	2.43 kΩ	249 kΩ	47 µF	1-45 mΩ	15 - 42V
5V	34 kΩ	6.49 kΩ	100 kΩ	100 µF	1-95 mΩ	8 - 42V

Figure 46. Simplified Application Schematic

8.2.1 Design Requirements

For this example the following application parameters exist.

- V_{IN} Range = Up to 42 V
- V_{OUT} = 5 V to 30 V
- I_{OUT} = 3 A

Refer to the table in Figure 46 for more information.

8.2.2 Detailed Design Procedure

8.2.2.1 Design Steps for the LMZ14203H Application

The LMZ14203H is fully supported by WEBENCH which offers the following: component selection, electrical simulation, thermal simulation, as well as a build-it prototype board for a reduction in design time. The following list of steps can be used to manually design the LMZ14203H application.

1. Select minimum operating V_{IN} with enable divider resistors.
2. Program V_O with divider resistor selection.
3. Program turnon time with soft-start capacitor selection.
4. Select C_O.

Typical Application (continued)

5. Select C_{IN}.
6. Set operating frequency with R_{ON}.
7. Determine module dissipation.
8. Lay out PCB for required thermal performance.

8.2.2.1.1 Enable Divider, R_{ENT} and R_{ENB} Selection

The enable input provides a precise 1.18-V reference threshold to allow direct logic drive or connection to a voltage divider from a higher enable voltage such as V_{IN}. The enable input also incorporates 90 mV (typical) of hysteresis resulting in a falling threshold of 1.09 V. The maximum recommended voltage into the EN pin is 6.5 V. For applications where the midpoint of the enable divider exceeds 6.5 V, a small Zener diode can be added to limit this voltage.

The function of the R_{ENT} and R_{ENB} divider is to allow the designer to choose an input voltage below which the circuit will be disabled. This implements the feature of programmable under voltage lockout. This is often used in battery-powered systems to prevent deep discharge of the system battery. It is also useful in system designs for sequencing of output rails or to prevent early turnon of the supply as the main input voltage rail rises at power up. Applying the enable divider to the main input rail is often done in the case of higher input voltage systems such as 24-V AC/DC systems where a lower boundary of operation should be established. In the case of sequencing supplies, the divider is connected to a rail that becomes active earlier in the power-up cycle than the LMZ14203H output rail. The two resistors should be chosen based on the following ratio:

$$R_{ENT} / R_{ENB} = (V_{IN\text{-}ENABLE} / 1.18\ V) - 1 \quad (1)$$

The EN pin is internally pulled up to VIN and can be left floating for always-on operation. However, it is good practice to use the enable divider and turn on the regulator when V_{IN} is close to reaching its nominal value. This will ensure smooth start-up and will prevent overloading the input supply.

8.2.2.1.2 Output Voltage Selection

Output voltage is determined by a divider of two resistors connected between V_O and ground. The midpoint of the divider is connected to the FB input. The voltage at FB is compared to a 0.8-V internal reference. In normal operation an ON-time cycle is initiated when the voltage on the FB pin falls below 0.8 V. The high-side MOSFET ON-time cycle causes the output voltage to rise and the voltage at the FB to exceed 0.8 V. As long as the voltage at FB is above 0.8 V, ON-time cycles will not occur.

The regulated output voltage determined by the external divider resistors R_{FBT} and R_{FBB} is:

$$V_O = 0.8\ V \times (1 + R_{FBT} / R_{FBB}) \quad (2)$$

Rearranging terms; the ratio of the feedback resistors for a desired output voltage is:

$$R_{FBT} / R_{FBB} = (V_O / 0.8\ V) - 1 \quad (3)$$

These resistors should be chosen from values in the range of 1 kΩ to 50 kΩ.

A feed-forward capacitor is placed in parallel with R_{FBT} to improve load step transient response. Its value is usually determined experimentally by load stepping between DCM and CCM conduction modes and adjusting for best transient response and minimum output ripple.

A table of values for R_{FBT} , R_{FBB} , and R_{ON} is included in the simplified applications schematic (see Figure 46).

8.2.2.1.3 Soft-Start Capacitor, C_{SS}, Selection

Programmable soft-start permits the regulator to slowly ramp to its steady-state operating point after being enabled, thereby reducing current inrush from the input supply and slowing the output voltage rise-time to prevent overshoot.

Upon turnon, after all UVLO conditions have been passed, an internal 8-uA current source begins charging the external soft-start capacitor. The soft-start time duration to reach steady-state operation is given by the formula:

$$t_{SS} = V_{REF} \times C_{SS} / Iss = 0.8\ V \times C_{SS} / 8\ \mu A \quad (4)$$

Equation 4 can be rearranged as follows:

$$C_{SS} = t_{SS} \times 8\ \mu A / 0.8\ V \quad (5)$$

Typical Application (continued)

Use of a 4700-pF capacitor results in 0.5-ms soft-start duration. This is a recommended value. Note high values of C_{SS} capacitance will cause more output voltage droop when a load transient goes across the DCM-CCM boundary. Use Equation 22 to find the DCM-CCM boundary load current for the specific operating condition. If a fast load transient response is desired for steps between DCM and CCM mode the soft-start capacitor value should be less than 0.018 µF.

Note the following conditions will reset the soft-start capacitor by discharging the SS input to ground with an internal 200-µA current sink:

- The enable input being pulled low
- Thermal shutdown condition
- Overcurrent fault
- Internal VIN_{UVLO}

8.2.2.1.4 Output Capacitor, C_O, Selection

None of the required output capacitance is contained within the module. At a minimum, the output capacitor must meet the worst-case RMS current rating of 0.5 × $I_{LR\ P-P}$, as calculated in Equation 23. Beyond that, additional capacitance will reduce output ripple so long as the ESR is low enough to permit it. A minimum value of 10 µF is generally required. Experimentation will be required if attempting to operate with a minimum value. Low-ESR capacitors, such as ceramic and polymer electrolytic capacitors are recommended.

8.2.2.1.4.1 Capacitance

Equation 6 provides a good first pass approximation of C_O for load transient requirements:

$$C_O \geq I_{STEP} \times V_{FB} \times L \times V_{IN} / (4 \times V_O \times (V_{IN} - V_O) \times V_{OUT\text{-}TRAN}) \quad (6)$$

As an example, for 3-A load step, V_{IN} = 24 V, V_{OUT} = 12 V, $V_{OUT\text{-}TRAN}$ = 50 mV:

$$C_O \geq 3\ A \times 0.8\ V \times 10\ \mu H \times 24\ V / (4 \times 12V\ (\ 24\ V - 12\ V) \times 50\ mV) \quad (7)$$

$$C_O \geq 20 \mu F \quad (8)$$

8.2.2.1.4.2 ESR

The ESR of the output capacitor affects the output voltage ripple. High ESR will result in larger V_{OUT} peak-to-peak ripple voltage. Furthermore, high output voltage ripple caused by excessive ESR can trigger the overvoltage protection monitored at the FB pin. The ESR should be chosen to satisfy the maximum desired V_{OUT} peak-to-peak ripple voltage and to avoid overvoltage protection during normal operation. The following equations can be used:

$$ESR_{MAX\text{-}RIPPLE} \leq V_{OUT\text{-}RIPPLE} / I_{LR\ P-P}$$

where

- $I_{LR\ P-P}$ is calculated using Equation 23. (9)

$$ESR_{MAX\text{-}OVP} < (V_{FB\text{-}OVP} - V_{FB}) / (I_{LR\ P-P} \times A_{FB})$$

where

- A_{FB} is the gain of the feedback network from V_{OUT} to V_{FB} at the switching frequency. (10)

As worst-case, assume the gain of A_{FB} with the C_{FF} capacitor at the switching frequency is 1.

The selected capacitor should have sufficient voltage and RMS current rating. The RMS current through the output capacitor is:

$$I(C_{OUT(RMS)}) = I_{LR\ P-P} / \sqrt{12} \quad (11)$$

8.2.2.1.5 Input Capacitor, C_{IN}, Selection

The LMZ14203H module contains an internal 0.47-µF input ceramic capacitor. Additional input capacitance is required external to the module to handle the input ripple current of the application. This input capacitance should be as close as possible to the module. Input capacitor selection is generally directed to satisfy the input ripple current requirements rather than by capacitance value.

Typical Application (continued)

Worst-case input ripple current rating is dictated by Equation 12.

$$I(C_{IN(RMS)}) \cong 1 / 2 \times I_O \times \sqrt{} (D / 1\text{-}D)$$

where

- $D \cong V_O / V_{IN}$ (12)

(As a point of reference, the worst-case ripple current will occur when the module is presented with full load current and when $V_{IN} = 2 \times V_O$).

Recommended minimum input capacitance is 10-uF X7R ceramic with a voltage rating at least 25% higher than the maximum applied input voltage for the application. TI also recommends to pay attention to the voltage and temperature deratings of the capacitor selected. It should be noted that ripple current rating of ceramic capacitors may be missing from the capacitor data sheet and you may have to contact the capacitor manufacturer for this rating.

If the system design requires a certain maximum value of input ripple voltage ΔV_{IN} to be maintained then Equation 13 may be used.

$$C_{IN} \geq I_O \times D \times (1\text{–}D) / f_{SW\text{-}CCM} \times \Delta V_{IN} \quad (13)$$

If ΔV_{IN} is 1% of V_{IN} for a 24-V input to 12V output application this equals 240 mV and f_{SW} = 400 kHz.

$$C_{IN} \geq 3\ A \times 12\ V/24\ V \times (1\text{–}\ 12\ V/24\ V) / (400000 \times 0.240\ V) \quad (14)$$

$$C_{IN} \geq 7.8\ \mu F \quad (15)$$

Additional bulk capacitance with higher ESR may be required to damp any resonant effects of the input capacitance and parasitic inductance of the incoming supply lines.

8.2.2.1.6 ON-Time, R_{ON}, Resistor Selection

Many designs will begin with a desired switching frequency in mind. As seen in the *Typical Characteristics* section, the best efficiency is achieved in the 300kHz-400kHz switching frequency range. Equation 16 can be used to calculate the R_{ON} value.

$$f_{SW(CCM)} \cong V_O / (1.3 \times 10^{-10} \times R_{ON}) \quad (16)$$

This can be rearranged as

$$R_{ON} \cong V_O / (1.3 \times 10^{-10} \times f_{SW(CCM)}) \quad (17)$$

The selection of R_{ON} and $f_{SW(CCM)}$ must be confined by limitations in the ON-time and OFF-time for the *COT Control Circuit Overview* section.

The ON-time of the LMZ14203H timer is determined by the resistor R_{ON} and the input voltage V_{IN}. It is calculated as follows:

$$t_{ON} = (1.3 \times 10^{-10} \times R_{ON}) / V_{IN} \quad (18)$$

The inverse relationship of t_{ON} and V_{IN} gives a nearly constant switching frequency as V_{IN} is varied. R_{ON} should be selected such that the ON-time at maximum V_{IN} is greater than 150 ns. The ON-timer has a limiter to ensure a minimum of 150 ns for t_{ON}. This limits the maximum operating frequency, which is governed by Equation 19.

$$f_{SW(MAX)} = V_O / (V_{IN(MAX)} \times 150\ ns) \quad (19)$$

This equation can be used to select R_{ON} if a certain operating frequency is desired so long as the minimum ON-time of 150 ns is observed. The limit for R_{ON} can be calculated as follows:

$$R_{ON} \geq V_{IN(MAX)} \times 150\ nsec / (1.3 \times 10^{-10}) \quad (20)$$

If R_{ON} calculated in Equation 17 is less than the minimum value determined in Equation 20, a lower frequency should be selected. Alternatively, $V_{IN(MAX)}$ can also be limited in order to keep the frequency unchanged.

Additionally, the minimum OFF-time of 260 ns (typical) limits the maximum duty ratio. Larger R_{ON} (lower F_{SW}) should be selected in any application requiring large duty ratio.

8.2.2.1.6.1 Discontinuous Conduction and Continuous Conduction Mode Selection

Operating frequency in DCM can be calculated as follows:

$$f_{SW(DCM)} \cong V_O \times (V_{IN}\text{-}1) \times 10\ \mu H \times 1.18 \times 10^{20} \times I_O / (V_{IN}\text{–}V_O) \times R_{ON}^2 \quad (21)$$

Typical Application (continued)

In CCM, current flows through the inductor through the entire switching cycle and never falls to zero during the OFF-time. The switching frequency remains relatively constant with load current and line voltage variations. The CCM operating frequency can be calculated using Equation 16.

The approximate formula for determining the DCM/CCM boundary is as follows:

$$I_{DCB} \cong V_O \times (V_{IN} - V_O) / (2 \times 10\ \mu H \times f_{SW(CCM)} \times V_{IN}) \quad (22)$$

The inductor internal to the module is 10 µH. This value was chosen as a good balance between low and high input voltage applications. The main parameter affected by the inductor is the amplitude of the inductor ripple current (I_{LR}). I_{LR} can be calculated with:

$$I_{LR\ P\text{-}P} = V_O \times (V_{IN} - V_O) / (10\ \mu H \times f_{SW} \times V_{IN})$$

where

- V_{IN} is the maximum input voltage and f_{SW} is determined from Equation 16. (23)

If the output current I_O is determined by assuming that $I_O = I_L$, the higher and lower peak of I_{LR} can be determined. Be aware that the lower peak of I_{LR} must be positive if CCM operation is required.

8.2.3 Application Curve

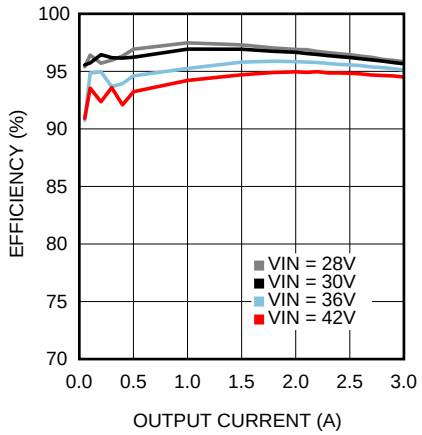


Figure 47. Efficiency V_{OUT} = 24 V, T_A = 25°C

9 Power Supply Recommendations

The LMZ14203H device is designed to operate from an input voltage supply range between 4.5 V and 42 V. This input supply should be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail should be low enough that an input current transient does not cause a high enough drop at the LMZ14203H supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is more than a few inches from the LMZ14203H, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 47-µF or 100-µF electrolytic capacitor is a typical choice.

10 Layout

10.1 Layout Guidelines

PCB layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce and resistive voltage drop in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

1. **Minimize area of switched current loops.**

   From an EMI reduction standpoint, it is imperative to minimize the high di/dt paths during PCB layout. The high current loops that do not overlap have high di/dt content that will cause observable high frequency noise on the output pin if the input capacitor (Cin1) is placed at a distance away from the LMZ14203. Therefore place C_{IN1} as close as possible to the LMZ14203 VIN and GND exposed pad. This will minimize the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor should consist of a localized top side plane that connects to the GND exposed pad (EP).

2. **Have a single point ground.**

   The ground connections for the feedback, soft-start, and enable components should be routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior. Provide the single point ground connection from pin 4 to EP.

3. **Minimize trace length to the FB pin.**

   Both feedback resistors, R_{FBT} and R_{FBB}, and the feed forward capacitor C_{FF}, should be close to the FB pin. Since the FB node is high impedance, maintain the copper area as small as possible. The trace are from R_{FBT}, R_{FBB}, and C_{FF} should be routed away from the body of the LMZ14203 to minimize noise.

4. **Make input and output bus connections as wide as possible.**

   This reduces any voltage drops on the input or output of the converter and maximizes efficiency. To optimize voltage accuracy at the load, ensure that a separate feedback voltage sense trace is made to the load. Doing so will correct for voltage drops and provide optimum output accuracy.

5. **Provide adequate device heat-sinking.**

   Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has a plurality of copper layers, these thermal vias can also be employed to make connection to inner layer heat-spreading ground planes. For best results use a 6 × 6 via array with minimum via diameter of 8 mils thermal vias spaced 59 mils (1.5 mm). Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

10.1.1 Power Module SMT Guidelines

The recommendations below are for a standard module surface mount assembly

- Land Pattern – Follow the PCB land pattern with either soldermask defined or non-soldermask defined pads
- Stencil Aperture
  - For the exposed die attach pad (DAP), adjust the stencil for approximately 80% coverage of the PCB land pattern
  - For all other I/O pads use a 1:1 ratio between the aperture and the land pattern recommendation
- Solder Paste – Use a standard SAC Alloy such as SAC 305, type 3 or higher

Layout Guidelines (continued)

- Stencil Thickness – 0.125 mm to 0.15 mm
- Reflow - Refer to solder paste supplier recommendation and optimized per board size and density
- Refer to AN *Design Summary LMZ1xxx and LMZ2xxx Power Modules Family* (SNAA214) for Reflow information.
- Maximum number of reflows allowed is one

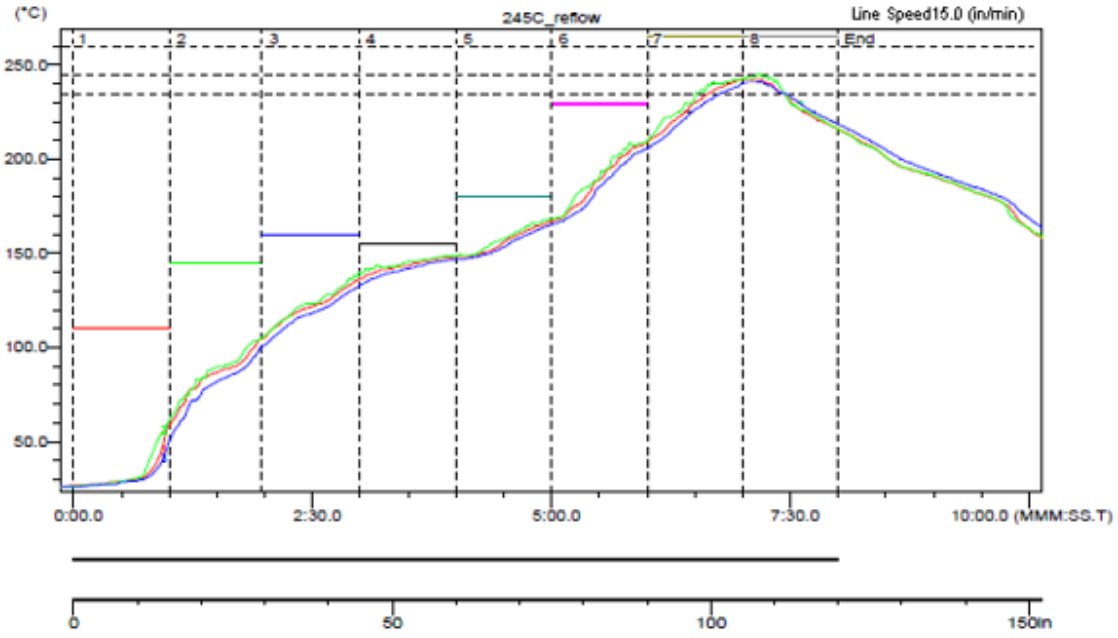


Figure 48. Sample Reflow Profile

Table 1. Sample Reflow Profile Table

PROBE	MAX TEMP (°C)	REACHED MAX TEMP	TIME ABOVE 235°C	REACHED 235°C	TIME ABOVE 245°C	REACHED 245°C	TIME ABOVE 260°C	REACHED 260°C
1	242.5	6.58	0.49	6.39	0	–	0	–
2	242.5	7.1	0.55	6.31	0	7.1	0	–
3	241	7.09	0.42	6.44	0	–	0	–

10.2 Layout Example

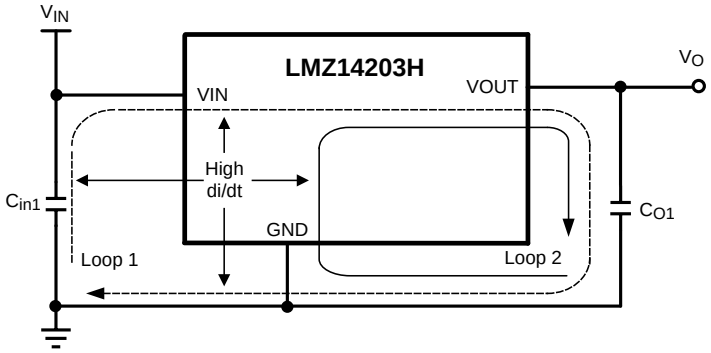


Figure 49. Minimize Area of Current Loops in Buck Module

Layout Example (continued)

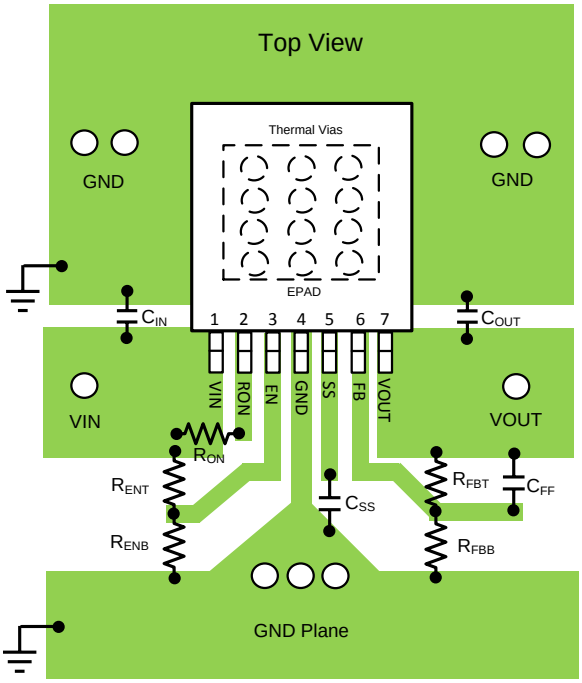


Figure 50. PCB Layout Guide

10.3 Power Dissipation and Board Thermal Requirements

For a design case of V_{IN} = 24 V, V_{OUT} = 12 V, I_{OUT} = 3 A, T_A (MAX) = 65°C , and $T_{JUNCTION}$ = 125°C, the device must see a maximum junction-to-ambient thermal resistance of:

$$R_{\theta JA\text{-}MAX} < (T_{J\text{-}MAX} - T_{A(MAX)}) / P_D \quad (24)$$

This $R_{\theta JA\text{-}MAX}$ will ensure that the junction temperature of the regulator does not exceed $T_{J\text{-}MAX}$ in the particular application ambient temperature.

To calculate the required $R_{\theta JA\text{-}MAX}$ we need to get an estimate for the power losses in the IC. The following graph is taken form the *Typical Characteristics* section (Figure 16) and shows the power dissipation of the LMZ14203H for V_{OUT} = 12 V at 85°C T_A.

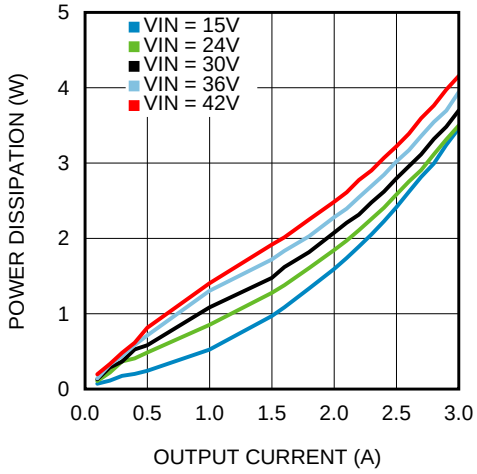


Figure 51. Power Dissipation V_{OUT} = 12V T_A = 85°C

Power Dissipation and Board Thermal Requirements (continued)

Using the 85°C T_A power dissipation data as a conservative starting point, the power dissipation P_D for V_{IN} = 24 V and V_{OUT} = 12V is estimated to be 3.5W. The necessary $R_{\theta JA-MAX}$ can now be calculated.

$$R_{\theta JA-MAX} < (125°C - 65°C) / 3.5W \quad (25)$$

$$R_{\theta JA-MAX} < 17.1°C/W \quad (26)$$

To achieve this thermal resistance the PCB is required to dissipate the heat effectively. The area of the PCB will have a direct effect on the overall junction-to-ambient thermal resistance. In order to estimate the necessary copper area we can refer to Figure 52. This graph is taken from the *Typical Characteristics* section (Figure 31) and shows how the $R_{\theta JA}$ varies with the PCB area.

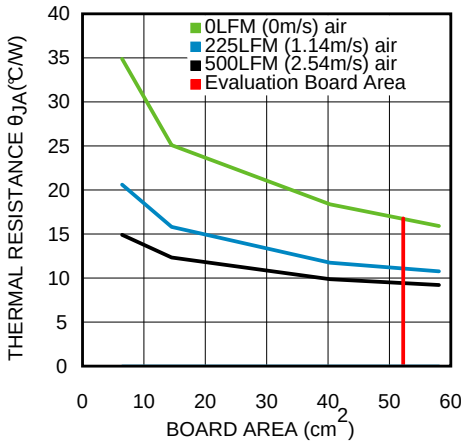


Figure 52. Package Thermal Resistance $R_{\theta JA}$ 4-Layer PCB With 1-oz Copper

For $R_{\theta JA-MAX}$< 17.1°C/W and only natural convection (that is., no air flow), the PCB area will have to be at least 52 cm^2. This corresponds to a square board with 7.25 cm x 7.25 cm (2.85 in x 2.85 in) copper area, 4 layers, and 1oz copper thickness. Higher copper thickness will further improve the overall thermal performance. As a reference, the evaluation board has 2-oz copper on the top and bottom layers, achieving $R_{\theta JA}$ of 14.9°C/W for the same board area. Note thermal vias should be placed under the IC package to easily transfer heat from the top layer of the PCB to the inner layers and the bottom layer.

For more guidelines and insight on PCB copper area, thermal vias placement, and general thermal design practices see the application note, *AN-2020 Thermal Design By Insight, Not Hindsight* (SNVA419).

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

11.1.1.1 Related Documentation

- *AN-2027 Inverting Application for the LMZ14203 SIMPLE SWITCHER Power Module*, SNVA425
- *Evaluation Board Application Note AN-2024*, SNVA422
- *AN-2026 Effect of PCB Design on Thermal Performance of SIMPLE SWITCHER Power Modules*, SNVA424
- *AN-2020 Thermal Design By Insight, Not Hindsight*, SNVA419
- *AN Design Summary LMZ1xxx and LMZ2xxx Power Modules Family*, SNAA214

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMZ14203HTZ/NOPB	ACTIVE	TO-PMOD	NDW	7	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	LMZ14203 HTZ	Samples
LMZ14203HTZE/NOPB	ACTIVE	TO-PMOD	NDW	7	45	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	LMZ14203 HTZ	Samples
LMZ14203HTZX/NOPB	ACTIVE	TO-PMOD	NDW	7	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	LMZ14203 HTZ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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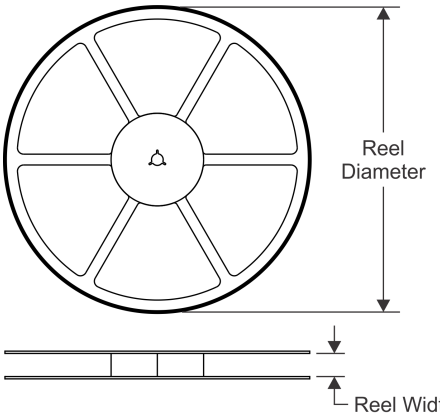
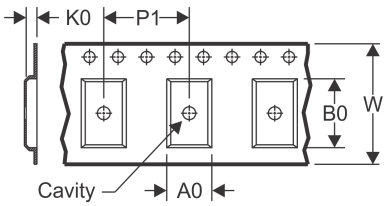
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

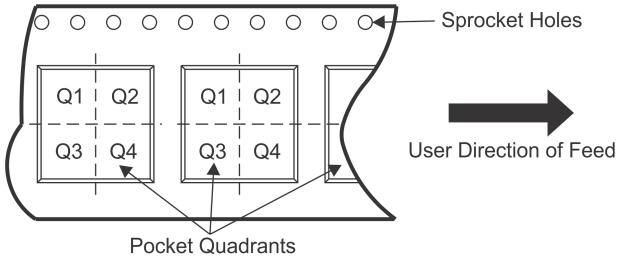


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

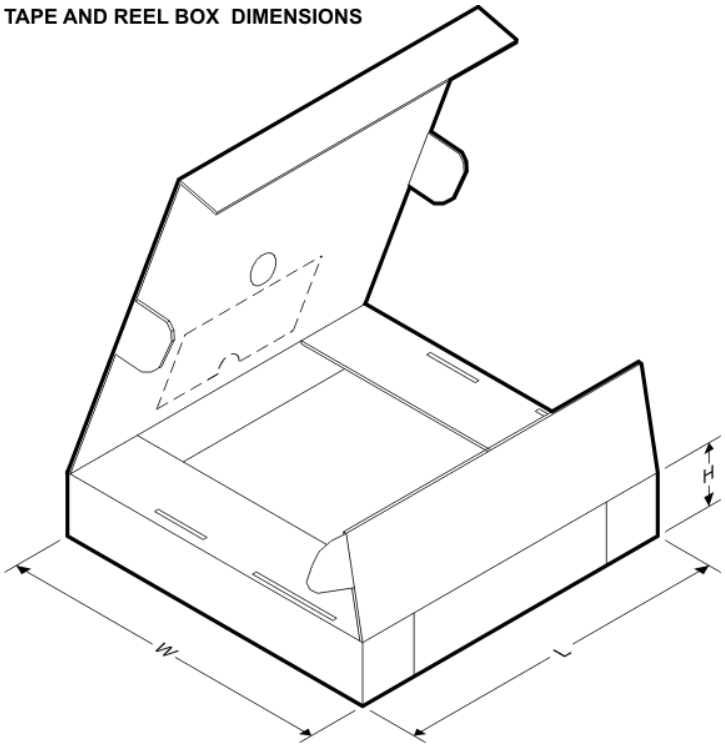


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMZ14203HTZ/NOPB	TO-PMOD	NDW	7	250	330.0	24.4	10.6	14.22	5.0	16.0	24.0	Q2
LMZ14203HTZX/NOPB	TO-PMOD	NDW	7	500	330.0	24.4	10.6	14.22	5.0	16.0	24.0	Q2

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

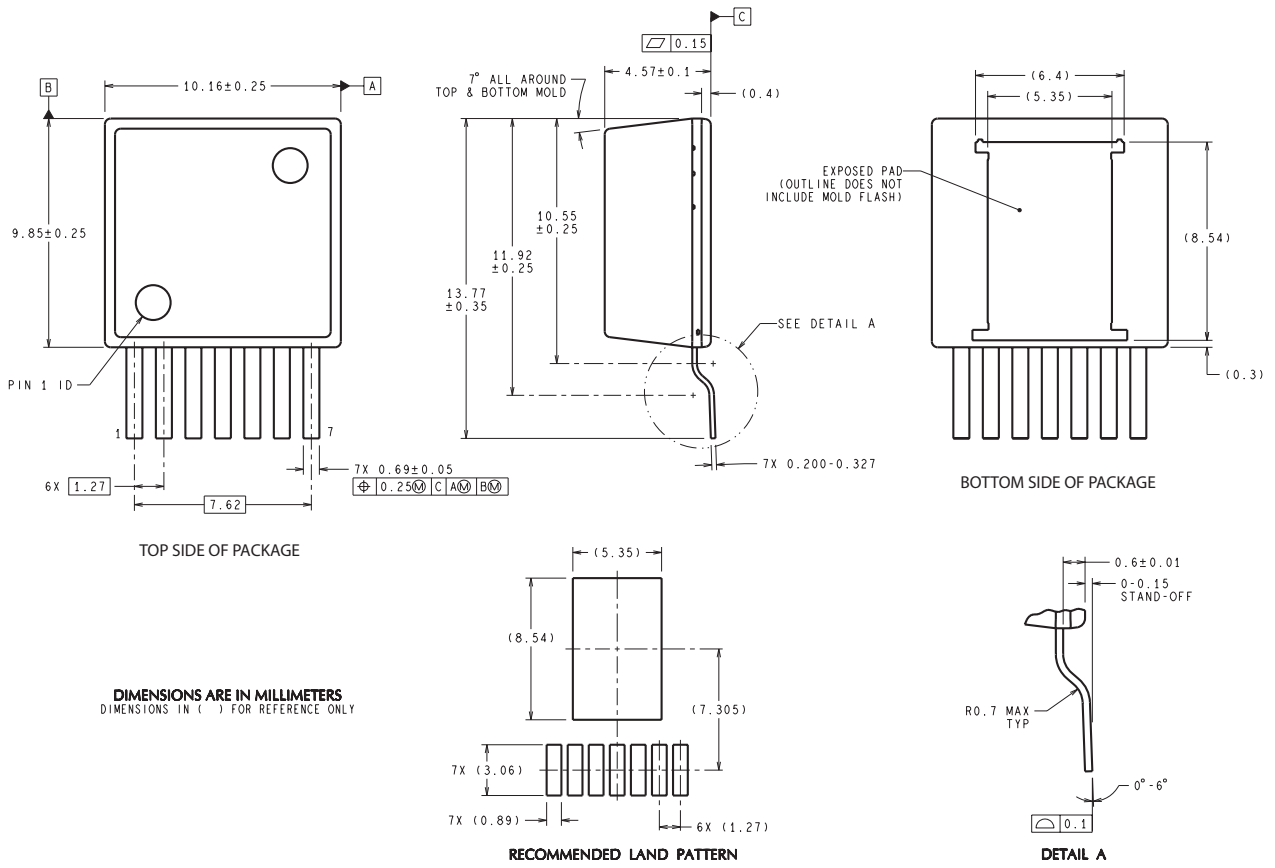


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMZ14203HTZ/NOPB	TO-PMOD	NDW	7	250	367.0	367.0	45.0
LMZ14203HTZX/NOPB	TO-PMOD	NDW	7	500	367.0	367.0	45.0

MECHANICAL DATA

NDW0007A



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