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LPC1111/12/13/14

32-bit ARM Cortex-M0 microcontroller; up to 32 kB flash and 8 kB SRAM

Rev. 00.11 — 13 November 2009 **Objective data sheet**

1. General description

The LPC1111/12/13/14 are a ARM Cortex-M0 based, low-cost 32-bit MCU family, designed for 8/16-bit microcontroller applications, offering performance, low power, simple instruction set and memory addressing together with reduced code size compared to existing 8/16-bit architectures.

The LPC1111/12/13/14 operate at CPU frequencies of up to 50 MHz.

The peripheral complement of the LPC1111/12/13/14 includes up to 32 kB of flash memory, up to 8 kB of data memory, one Fast-mode Plus I²C-bus interface, one RS-485/EIA-485 UART, up to two SPI interfaces with SSP features, four general purpose timers, a 10-bit ADC, and up to 42 general purpose I/O pins.

2. Features

- ARM Cortex-M0 processor, running at frequencies of up to 50 MHz.
- ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).
- 32 kB (LPC1114), 24 kB (LPC1113), 16 kB (LPC1112), or 8 kB (LPC1111) on-chip flash programming memory.
- 8 kB, 4 kB, or 2 kB SRAM.
- In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software.
- Serial interfaces:
  - UART with fractional baud rate generation, internal FIFO, and RS-485 support.
  - Two SPI controllers with SSP features and with FIFO and multi-protocol capabilities (second SPI on LQFP48 and PLCC44 packages only).
  - I²C-bus interface supporting full I²C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.
- Other peripherals:
  - Up to 42 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors.
  - Four general purpose timers/counters with a total of four capture inputs and 13 match outputs.
  - Programmable WatchDog Timer (WDT).
  - System tick timer.
- Serial Wire Debug.
- High-current output driver (20 mA) on one pin.
- High-current sink drivers (20 mA) on two I²C-bus pins in Fast-mode Plus.

- Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, and Deep power-down modes.
- Three reduced power modes: Sleep, Deep-sleep, and Deep power-down.
- Single 3.3 V power supply (1.8 V to 3.6 V).
- 10-bit ADC with input multiplexing among 8 pins.
- GPIO pins can be used as edge and level sensitive interrupt sources.
- Clock output function with divider that can reflect the system oscillator clock, IRC clock, CPU clock, and the Watchdog clock.
- Processor wake-up from Deep-sleep mode via a dedicated start logic using up to 13 of the functional pins.
- Brownout detect with four separate thresholds for interrupt and one threshold for forced reset.
- Power-On Reset (POR).
- Crystal oscillator with an operating range of 1 MHz to 25 MHz.
- 12 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.
- PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the main oscillator, the internal RC oscillator, or the watchdog oscillator.
- Available as 48-pin LQFP package, 33-pin HVQFN package, and 44-pin PLCC package.

3. Applications

- eMetering
- Lighting
- Industrial networking
- Alarm systems
- White goods

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1111FHN33/101	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 x 7 x 0.85 mm	n/a
LPC1111FHN33/201	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 x 7 x 0.85 mm	n/a
LPC1112FHN33/101	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 x 7 x 0.85 mm	n/a
LPC1112FHN33/201	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 x 7 x 0.85 mm	n/a
LPC1113FHN33/201	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 x 7 x 0.85 mm	n/a
LPC1113FHN33/301	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 x 7 x 0.85 mm	n/a

Table 1. Ordering information *...continued*

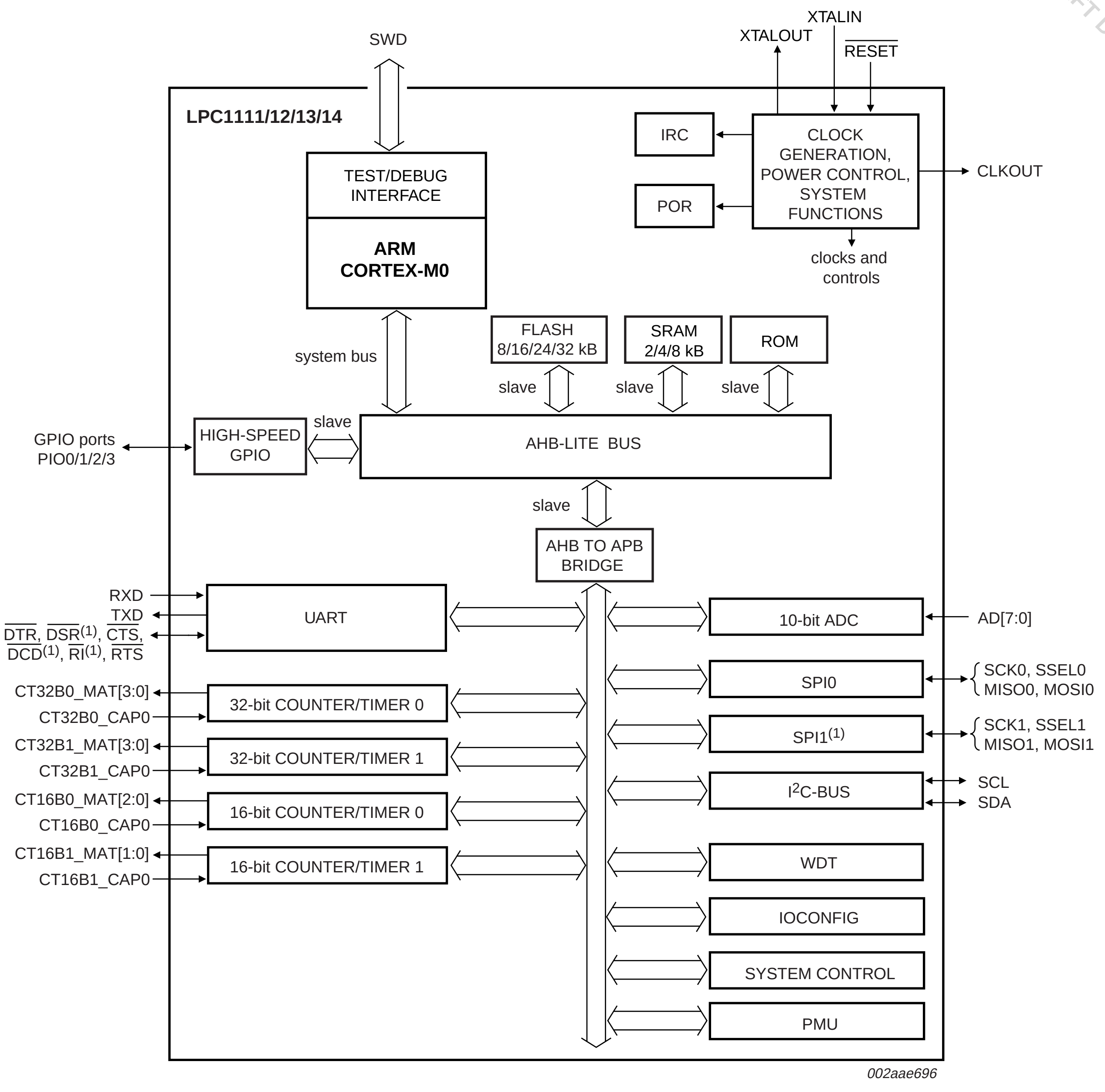
Type number	Package		
	Name	Description	Version
LPC1114FHN33/201	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 x 7 x 0.85 mm	n/a
LPC1114FHN33/301	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 x 7 x 0.85 mm	n/a
LPC1113FBD48/301	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm	sot313-2
LPC1114FBD48/301	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm	sot313-2
LPC1114FA44/301	PLCC44	PLCC44; plastic leaded chip carrier; 44 leads	sot187-2

4.1 Ordering options

Table 2. Ordering options

Type number	Flash	Total SRAM	UART RS-485	I^2C/ Fast+	SPI	ADC channels	Package
LPC1111							
LPC1111FHN33/101	8 kB	2 kB	1	1	1	8	HVQFN33
LPC1111FHN33/201	8 kB	4 kB	1	1	1	8	HVQFN33
LPC1112							
LPC1112FHN33/101	16 kB	2 kB	1	1	1	8	HVQFN33
LPC1112FHN33/201	16 kB	4 kB	1	1	1	8	HVQFN33
LPC1113							
LPC1113FHN33/201	24 kB	4 kB	1	1	1	8	HVQFN33
LPC1113FHN33/301	24 kB	8 kB	1	1	1	8	HVQFN33
LPC1113FBD48/301	24 kB	8 kB	1	1	2	8	LQFP48
LPC1114							
LPC1114FHN33/201	32 kB	4 kB	1	1	1	8	HVQFN33
LPC1114FHN33/301	32 kB	8 kB	1	1	1	8	HVQFN33
LPC1114FBD48/301	32 kB	8 kB	1	1	2	8	LQFP48
LPC1114FA44/301	32 kB	8 kB	1	1	2	8	PLCC44

5. Block diagram



(1) LQFP48 and PLCC44 packages only.

Fig 1. LPC1111/12/13/14 block diagram

6. Pinning information

6.1 Pinning

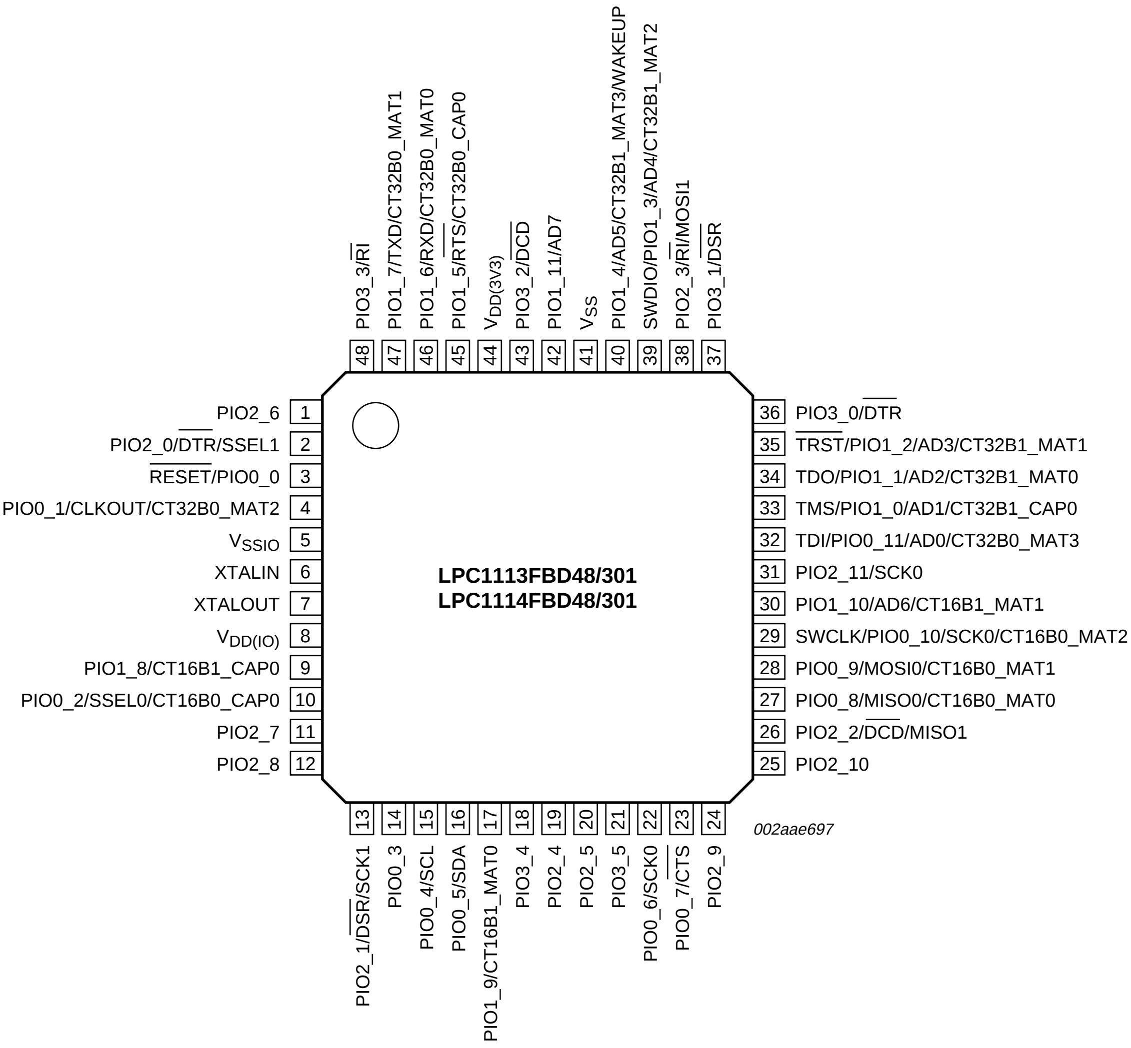


Fig 2. Pin configuration LQFP48 package

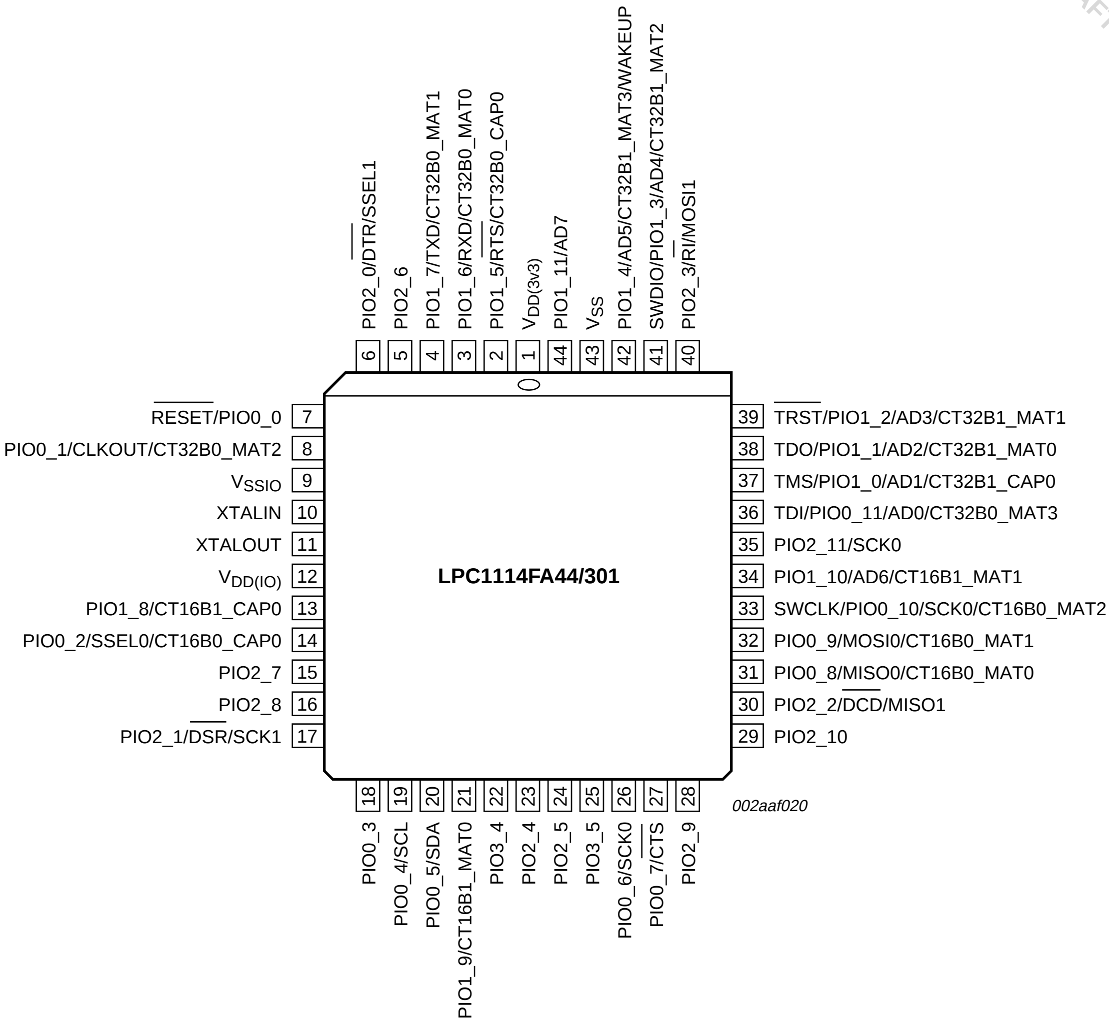


Fig 3. Pin configuration PLCC44 package

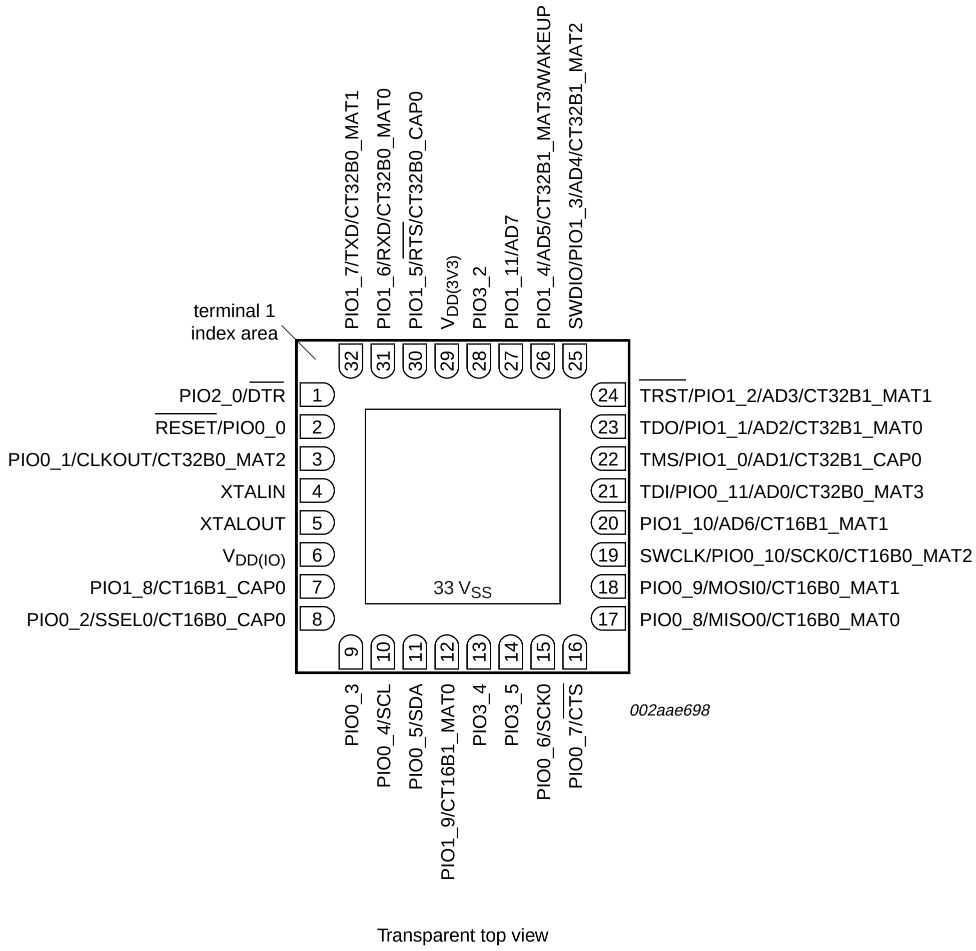


Fig 4. Pin configuration HVQFN 33 package

6.2 Pin description

Table 3. LPC1113/14 pin description table (LQFP48 package)

Symbol	Pin	Type	Description
PIO0_0 to PIO0_11		I/O	**Port 0 —** Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
$\overline{\text{RESET}}$/PIO0_0	3	I	**$\overline{\text{RESET}}$ —** External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.
		I/O	**PIO0_0 —** General purpose digital input/output pin.
PIO0_1/CLKOUT/ CT32B0_MAT2	4[1]	I/O	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
		O	**CLKOUT —** Clockout pin.
		O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	10[1]	I/O	**PIO0_2 —** General purpose digital input/output pin.
		O	**SSEL0 —** Slave Select for SPI0.
		I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO0_3	14[1]	I/O	**PIO0_3 —** General purpose digital input/output pin.
PIO0_4/SCL	15[2]	I/O	**PIO0_4 —** General purpose digital input/output pin.
		I/O	**SCL —** I^{2}C-bus clock input/output. High-current sink only if I^{2}C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	16[2]	I/O	**PIO0_5 —** General purpose digital input/output pin.
		I/O	**SDA —** I^{2}C-bus data input/output. High-current sink only if I^{2}C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	22[1]	I/O	**PIO0_6 —** General purpose digital input/output pin.
		I/O	**SCK0 —** Serial clock for SPI0.
PIO0_7/$\overline{\text{CTS}}$	23[1]	I/O	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
		I	**$\overline{\text{CTS}}$ —** Clear To Send input for UART.
PIO0_8/MISO0/ CT16B0_MAT0	27[1]	I/O	**PIO0_8 —** General purpose digital input/output pin.
		I/O	**MISO0 —** Master In Slave Out for SPI0.
		O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	28[1]	I/O	**PIO0_9 —** General purpose digital input/output pin.
		I/O	**MOSI0 —** Master Out Slave In for SPI0.
		O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
SWCLK/PIO0_10/ SCK0/CT16B0_MAT2	29[1]	I	**SWCLK —** Serial wire clock and test clock TCK for JTAG interface.
		I/O	**PIO0_10 —** General purpose digital input/output pin.
		I/O	**SCK0 —** Serial clock for SPI0.
		O	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
TDI/PIO0_11/ AD0/CT32B0_MAT3	32[3]	I	**TDI —** Test Data In for JTAG interface.
		I/O	**PIO0_11 —** General purpose digital input/output pin.
		I	**AD0 —** A/D converter, input 0.
		O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.

Table 3. LPC1113/14 pin description table (LQFP48 package) *...continued*

Symbol	Pin	Type	Description
PIO1_0 to PIO1_11		I/O	**Port 1** — Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.
TMS/PIO1_0/ AD1/CT32B1_CAP0	33[3]	I	**TMS** — Test Mode Select for JTAG interface.
		I/O	**PIO1_0** — General purpose digital input/output pin.
		I	**AD1** — A/D converter, input 1.
		I	**CT32B1_CAP0** — Capture input 0 for 32-bit timer 1.
TDO/PIO1_1/ AD2/CT32B1_MAT0	34[3]	O	**TDO** — Test Data Out for JTAG interface.
		I/O	**PIO1_1** — General purpose digital input/output pin.
		I	**AD2** — A/D converter, input 2.
		O	**CT32B1_MAT0** — Match output 0 for 32-bit timer 1.
$\overline{\text{TRST}}$/PIO1_2/ AD3/CT32B1_MAT1	35[3]	I	**$\overline{\text{TRST}}$** — Test Reset for JTAG interface.
		I/O	**PIO1_2** — General purpose digital input/output pin.
		I	**AD3** — A/D converter, input 3.
		O	**CT32B1_MAT1** — Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/AD4/ CT32B1_MAT2	39[3]	I/O	**SWDIO** — Serial wire debug input/output.
		I/O	**PIO1_3** — General purpose digital input/output pin.
		I	**AD4** — A/D converter, input 4.
		O	**CT32B1_MAT2** — Match output 2 for 32-bit timer 1.
PIO1_4/AD5/ CT32B1_MAT3/WAKEUP	40[3]	I/O	**PIO1_4** — General purpose digital input/output pin.
		I	**AD5** — A/D converter, input 5.
		O	**CT32B1_MAT3** — Match output 3 for 32-bit timer 1.
		I	**WAKEUP** — Deep power-down mode wake-up pin.
PIO1_5/$\overline{\text{RTS}}$/ CT32B0_CAP0	45[1]	I/O	**PIO1_5** — General purpose digital input/output pin.
		O	**$\overline{\text{RTS}}$** — Request To Send output for UART.
		I	**CT32B0_CAP0** — Capture input 0 for 32-bit timer 0.
PIO1_6/RXD/ CT32B0_MAT0	46[1]	I/O	**PIO1_6** — General purpose digital input/output pin.
		I	**RXD** — Receiver input for UART.
		O	**CT32B0_MAT0** — Match output 0 for 32-bit timer 0.
PIO1_7/TXD/ CT32B0_MAT1	47[1]	I/O	**PIO1_7** — General purpose digital input/output pin.
		O	**TXD** — Transmitter output for UART.
		O	**CT32B0_MAT1** — Match output 1 for 32-bit timer 0.
PIO1_8/CT16B1_CAP0	9[1]	I/O	**PIO1_8** — General purpose digital input/output pin.
		I	**CT16B1_CAP0** — Capture input 0 for 16-bit timer 1.
PIO1_9/CT16B1_MAT0	17[1]	I/O	**PIO1_9** — General purpose digital input/output pin.
		O	**CT16B1_MAT0** — Match output 0 for 16-bit timer 1.
PIO1_10/AD6/ CT16B1_MAT1	30[3]	I/O	**PIO1_10** — General purpose digital input/output pin.
		I	**AD6** — A/D converter, input 6.
		O	**CT16B1_MAT1** — Match output 1 for 16-bit timer 1.
PIO1_11/AD7	42[3]	I/O	**PIO1_11** — General purpose digital input/output pin.
		I	**AD7** — A/D converter, input 7.

Table 3. LPC1113/14 pin description table (LQFP48 package) *…continued*

Symbol	Pin	Type	Description
PIO2_0 to PIO2_11		I/O	**Port 2** — Port 2 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 2 pins depends on the function selected through the IOCONFIG register block.
PIO2_0/$\overline{\text{DTR}}$/SSEL1	2[1]	I/O	**PIO2_0** — General purpose digital input/output pin.
		O	**$\overline{\text{DTR}}$** — Data Terminal Ready output for UART.
		O	**SSEL1** — Slave Select for SPI1.
PIO2_1/$\overline{\text{DSR}}$/SCK1	13[1]	I/O	**PIO2_1** — General purpose digital input/output pin.
		I	**$\overline{\text{DSR}}$** — Data Set Ready input for UART.
		I/O	**SCK1** — Serial clock for SPI1.
PIO2_2/$\overline{\text{DCD}}$/MISO1	26[1]	I/O	**PIO2_2** — General purpose digital input/output pin.
		I	**$\overline{\text{DCD}}$** — Data Carrier Detect input for UART.
		I/O	**MISO1** — Master In Slave Out for SPI1.
PIO2_3/$\overline{\text{RI}}$/MOSI1	38[1]	I/O	**PIO2_3** — General purpose digital input/output pin.
		I	**$\overline{\text{RI}}$** — Ring Indicator input for UART.
		I/O	**MOSI1** — Master Out Slave In for SPI1.
PIO2_4	19[1]	I/O	**PIO2_4** — General purpose digital input/output pin.
PIO2_5	20[1]	I/O	**PIO2_5** — General purpose digital input/output pin.
PIO2_6	1[1]	I/O	**PIO2_6** — General purpose digital input/output pin.
PIO2_7	11[1]	I/O	**PIO2_7** — General purpose digital input/output pin.
PIO2_8	12[1]	I/O	**PIO2_8** — General purpose digital input/output pin.
PIO2_9	24[1]	I/O	**PIO2_9** — General purpose digital input/output pin.
PIO2_10	25[1]	I/O	**PIO2_10** — General purpose digital input/output pin.
PIO2_11/SCK0	31[1]	I/O	**PIO2_11** — General purpose digital input/output pin.
		I/O	**SCK0** — Serial clock for SPI0.
PIO3_0 to PIO3_5		I/O	**Port 3** — Port 3 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 3 pins depends on the function selected through the IOCONFIG register block. Pins PIO3_6 to PIO3_11 are not available.
PIO3_0/$\overline{\text{DTR}}$	36[1]	I/O	**PIO3_0** — General purpose digital input/output pin.
		O	**$\overline{\text{DTR}}$** — Data Terminal Ready output for UART.
PIO3_1/$\overline{\text{DSR}}$	37[1]	I/O	**PIO3_1** — General purpose digital input/output pin.
		I	**$\overline{\text{DSR}}$** — Data Set Ready input for UART.
PIO3_2/$\overline{\text{DCD}}$	43[1]	I/O	**PIO3_2** — General purpose digital input/output pin.
		I	**$\overline{\text{DCD}}$** — Data Carrier Detect input for UART.
PIO3_3/$\overline{\text{RI}}$	48[1]	I/O	**PIO3_3** — General purpose digital input/output pin.
		I	**$\overline{\text{RI}}$** — Ring Indicator input for UART.
PIO3_4	18[1]	I/O	**PIO3_4** — General purpose digital input/output pin.
PIO3_5	21[1]	I/O	**PIO3_5** — General purpose digital input/output pin.
$V_{DD(IO)}$	8[4]	I	3.3 V input/output supply voltage.
$V_{DD(3V3)}$	44[4]	I	3.3 V supply voltage to the internal regulator and the ADC. Also used as the ADC reference voltage.
V_{SSIO}	5	I	Ground.

Table 3. LPC1113/14 pin description table (LQFP48 package) *…continued*

Symbol	Pin	Type	Description
XTALIN	6[5]	I	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	7[5]	O	Output from the oscillator amplifier.
V_{SS}	41	I	Ground.

[1] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[2] I^2C-bus pads compliant with the I^2C-bus specification for I^2C standard mode and I^2C Fast-mode Plus.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant.

[4] Tie together $V_{DD(3V3)}$ and $V_{DD(IO)}$ externally. If separate supplies are used for $V_{DD(3V3)}$ and $V_{DD(IO)}$, ensure that the voltage difference between both supplies is smaller than or equal to 0.5 V.

[5] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

Table 4. LPC1114 pin description table (PLCC44 package)

Symbol	Pin	Type	Description
PIO0_0 to PIO0_11		I/O	**Port 0 —** Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
$\overline{\text{RESET}}$/PIO0_0	7	I	**$\overline{\text{RESET}}$ —** External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.
		I/O	**PIO0_0 —** General purpose digital input/output pin.
PIO0_1/CLKOUT/ CT32B0_MAT2	8[1]	I/O	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
		O	**CLKOUT —** Clockout pin.
		O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	14[1]	I/O	**PIO0_2 —** General purpose digital input/output pin.
		O	**SSEL0 —** Slave Select for SPI0.
		I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO0_3	18[1]	I/O	**PIO0_3 —** General purpose digital input/output pin.
PIO0_4/SCL	19[2]	I/O	**PIO0_4 —** General purpose digital input/output pin.
		I/O	**SCL —** I^2C-bus clock input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	20[2]	I/O	**PIO0_5 —** General purpose digital input/output pin.
		I/O	**SDA —** I^2C-bus data input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	26[1]	I/O	**PIO0_6 —** General purpose digital input/output pin.
		I/O	**SCK0 —** Serial clock for SPI0.
PIO0_7/$\overline{\text{CTS}}$	27[1]	I/O	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
		I	**$\overline{\text{CTS}}$ —** Clear To Send input for UART.
PIO0_8/MISO0/ CT16B0_MAT0	31[1]	I/O	**PIO0_8 —** General purpose digital input/output pin.
		I/O	**MISO0 —** Master In Slave Out for SPI0.
		O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.

Table 4. LPC1114 pin description table (PLCC44 package) *...continued*

Symbol	Pin	Type	Description
PIO0_9/MOSI0/ CT16B0_MAT1	32[1]	I/O	**PIO0_9** — General purpose digital input/output pin.
		I/O	**MOSI0** — Master Out Slave In for SPI0.
		O	**CT16B0_MAT1** — Match output 1 for 16-bit timer 0.
SWCLK/PIO0_10/ SCK0/CT16B0_MAT2	33[1]	I	**SWCLK** — Serial wire clock and test clock TCK for JTAG interface.
		I/O	**PIO0_10** — General purpose digital input/output pin.
		I/O	**SCK0** — Serial clock for SPI0.
		O	**CT16B0_MAT2** — Match output 2 for 16-bit timer 0.
TDI/PIO0_11/ AD0/CT32B0_MAT3	36[3]	I	**TDI** — Test Data In for JTAG interface.
		I/O	**PIO0_11** — General purpose digital input/output pin.
		I	**AD0** — A/D converter, input 0.
		O	**CT32B0_MAT3** — Match output 3 for 32-bit timer 0.
PIO1_0 to PIO1_11		I/O	**Port 1** — Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.
TMS/PIO1_0/ AD1/CT32B1_CAP0	37[3]	I	**TMS** — Test Mode Select for JTAG interface.
		I/O	**PIO1_0** — General purpose digital input/output pin.
		I	**AD1** — A/D converter, input 1.
		I	**CT32B1_CAP0** — Capture input 0 for 32-bit timer 1.
TDO/PIO1_1/ AD2/CT32B1_MAT0	38[3]	O	**TDO** — Test Data Out for JTAG interface.
		I/O	**PIO1_1** — General purpose digital input/output pin.
		I	**AD2** — A/D converter, input 2.
		O	**CT32B1_MAT0** — Match output 0 for 32-bit timer 1.
$\overline{\text{TRST}}$/PIO1_2/ AD3/CT32B1_MAT1	39[3]	I	**$\overline{\text{TRST}}$** — Test Reset for JTAG interface.
		I/O	**PIO1_2** — General purpose digital input/output pin.
		I	**AD3** — A/D converter, input 3.
		O	**CT32B1_MAT1** — Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/AD4/ CT32B1_MAT2	41[3]	I/O	**SWDIO** — Serial wire debug input/output.
		I/O	**PIO1_3** — General purpose digital input/output pin.
		I	**AD4** — A/D converter, input 4.
		O	**CT32B1_MAT2** — Match output 2 for 32-bit timer 1.
PIO1_4/AD5/ CT32B1_MAT3/WAKEUP	42[3]	I/O	**PIO1_4** — General purpose digital input/output pin.
		I	**AD5** — A/D converter, input 5.
		O	**CT32B1_MAT3** — Match output 3 for 32-bit timer 1.
		I	**WAKEUP** — Deep power-down mode wake-up pin.
PIO1_5/$\overline{\text{RTS}}$/ CT32B0_CAP0	2[1]	I/O	**PIO1_5** — General purpose digital input/output pin.
		O	**$\overline{\text{RTS}}$** — Request To Send output for UART.
		I	**CT32B0_CAP0** — Capture input 0 for 32-bit timer 0.
PIO1_6/RXD/ CT32B0_MAT0	3[1]	I/O	**PIO1_6** — General purpose digital input/output pin.
		I	**RXD** — Receiver input for UART.
		O	**CT32B0_MAT0** — Match output 0 for 32-bit timer 0.

Table 4. LPC1114 pin description table (PLCC44 package) *…continued*

Symbol	Pin	Type	Description
PIO1_7/TXD/ CT32B0_MAT1	4[1]	I/O	**PIO1_7** — General purpose digital input/output pin.
		O	**TXD** — Transmitter output for UART.
		O	**CT32B0_MAT1** — Match output 1 for 32-bit timer 0.
PIO1_8/CT16B1_CAP0	13[1]	I/O	**PIO1_8** — General purpose digital input/output pin.
		I	**CT16B1_CAP0** — Capture input 0 for 16-bit timer 1.
PIO1_9/CT16B1_MAT0	21[1]	I/O	**PIO1_9** — General purpose digital input/output pin.
		O	**CT16B1_MAT0** — Match output 0 for 16-bit timer 1.
PIO1_10/AD6/ CT16B1_MAT1	34[3]	I/O	**PIO1_10** — General purpose digital input/output pin.
		I	**AD6** — A/D converter, input 6.
		O	**CT16B1_MAT1** — Match output 1 for 16-bit timer 1.
PIO1_11/AD7	44[3]	I/O	**PIO1_11** — General purpose digital input/output pin.
		I	**AD7** — A/D converter, input 7.
PIO2_0 to PIO2_11		I/O	**Port 2** — Port 2 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 2 pins depends on the function selected through the IOCONFIG register block.
PIO2_0/$\overline{DTR}$/SSEL1	6[1]	I/O	**PIO2_0** — General purpose digital input/output pin.
		O	**$\overline{DTR}$** — Data Terminal Ready output for UART.
		O	**SSEL1** — Slave Select for SPI1.
PIO2_1/$\overline{DSR}$/SCK1	17[1]	I/O	**PIO2_1** — General purpose digital input/output pin.
		I	**$\overline{DSR}$** — Data Set Ready input for UART.
		I/O	**SCK1** — Serial clock for SPI1.
PIO2_2/$\overline{DCD}$/MISO1	30[1]	I/O	**PIO2_2** — General purpose digital input/output pin.
		I	**$\overline{DCD}$** — Data Carrier Detect input for UART.
		I/O	**MISO1** — Master In Slave Out for SPI1.
PIO2_3/$\overline{RI}$/MOSI1	40[1]	I/O	**PIO2_3** — General purpose digital input/output pin.
		I	**$\overline{RI}$** — Ring Indicator input for UART.
		I/O	**MOSI1** — Master Out Slave In for SPI1.
PIO2_4	23[1]	I/O	**PIO2_4** — General purpose digital input/output pin.
PIO2_5	24[1]	I/O	**PIO2_5** — General purpose digital input/output pin.
PIO2_6	5[1]	I/O	**PIO2_6** — General purpose digital input/output pin.
PIO2_7	15[1]	I/O	**PIO2_7** — General purpose digital input/output pin.
PIO2_8	16[1]	I/O	**PIO2_8** — General purpose digital input/output pin.
PIO2_9	28[1]	I/O	**PIO2_9** — General purpose digital input/output pin.
PIO2_10	29[1]	I/O	**PIO2_10** — General purpose digital input/output pin.
PIO2_11/SCK0	35[1]	I/O	**PIO2_11** — General purpose digital input/output pin.
		I/O	**SCK0** — Serial clock for SPI0.
PIO3_0 to PIO3_5		I/O	**Port 3** — Port 3 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 3 pins depends on the function selected through the IOCONFIG register block. Pins PIO3_0 to PIO3_3 and PIO3_6 to PIO3_11 are not available.
PIO3_4	22[1]	I/O	**PIO3_4** — General purpose digital input/output pin.
PIO3_5	25[1]	I/O	**PIO3_5** — General purpose digital input/output pin.

Table 4. LPC1114 pin description table (PLCC44 package) *…continued*

Symbol	Pin	Type	Description
$V_{DD(IO)}$	12[4]	I	3.3 V input/output supply voltage.
$V_{DD(3V3)}$	1[4]	I	3.3 V supply voltage to the internal regulator and the ADC. Also used as the ADC reference voltage.
V_{SSIO}	9	I	Ground.
XTALIN	10[5]	I	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	11[5]	O	Output from the oscillator amplifier.
V_{SS}	43	I	Ground.

[1] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[2] I^{2}C-bus pads compliant with the I^{2}C-bus specification for I^{2}C standard mode and I^{2}C Fast-mode Plus.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant.

[4] Tie together $V_{DD(3V3)}$ and $V_{DD(IO)}$ externally. If separate supplies are used for $V_{DD(3V3)}$ and $V_{DD(IO)}$, ensure that the voltage difference between both supplies is smaller than or equal to 0.5 V.

[5] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

Table 5. LPC1111/12/13/14 pin description table (HVQFN33 package)

Symbol	Pin	Type	Description
PIO0_0 to PIO0_11		I/O	**Port 0** — Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
RESET/PIO0_0	2	I	**RESET** — External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.
		I/O	**PIO0_0** — General purpose digital input/output pin.
PIO0_1/CLKOUT/ CT32B0_MAT2	3[1]	I/O	**PIO0_1** — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
		O	**CLKOUT** — Clock out pin.
		O	**CT32B0_MAT2** — Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	8[1]	I/O	**PIO0_2** — General purpose digital input/output pin.
		O	**SSEL0** — Slave select for SPI0.
		I	**CT16B0_CAP0** — Capture input 0 for 16-bit timer 0.
PIO0_3	9[1]	I/O	**PIO0_3** — General purpose digital input/output pin.
PIO0_4/SCL	10[2]	I/O	**PIO0_4** — General purpose digital input/output pin.
		I/O	**SCL** — I^2C-bus clock input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	11[2]	I/O	**PIO0_5** — General purpose digital input/output pin.
		I/O	**SDA** — I^2C-bus data input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	15[1]	I/O	**PIO0_6** — General purpose digital input/output pin.
		I/O	**SCK0** — Serial clock for SPI0.
PIO0_7/CTS	16[1]	I/O	**PIO0_7** — General purpose digital input/output pin (high-current output driver).
		I	**CTS** — Clear To Send input for UART.
PIO0_8/MISO0/ CT16B0_MAT0	17[1]	I/O	**PIO0_8** — General purpose digital input/output pin.
		I/O	**MISO0** — Master In Slave Out for SPI0.
		O	**CT16B0_MAT0** — Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	18[1]	I/O	**PIO0_9** — General purpose digital input/output pin.
		I/O	**MOSI0** — Master Out Slave In for SPI0.
		O	**CT16B0_MAT1** — Match output 1 for 16-bit timer 0.
SWCLK/PIO0_10/SCK0/ CT16B0_MAT2	19[1]	I	**SWCLK** — Serial wire clock and test clock TCK for JTAG interface.
		I/O	**PIO0_10** — General purpose digital input/output pin.
		I/O	**SCK0** — Serial clock for SPI0.
		O	**CT16B0_MAT2** — Match output 2 for 16-bit timer 0.
TDI/PIO0_11/AD0/ CT32B0_MAT3	21[3]	I	**TDI** — Test Data In for JTAG interface.
		I/O	**PIO0_11** — General purpose digital input/output pin.
		I	**AD0** — A/D converter, input 0.
		O	**CT32B0_MAT3** — Match output 3 for 32-bit timer 0.
PIO1_0 to PIO1_11		I/O	**Port 1** — Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.

Table 5. LPC1111/12/13/14 pin description table (HVQFN33 package) *…continued*

Symbol	Pin	Type	Description
TMS/PIO1_0/AD1/ CT32B1_CAP0	22[3]	I	**TMS** — Test Mode Select for JTAG interface.
		I/O	**PIO1_0** — General purpose digital input/output pin.
		I	**AD1** — A/D converter, input 1.
		I	**CT32B1_CAP0** — Capture input 0 for 32-bit timer 1.
TDO/PIO1_1/AD2/ CT32B1_MAT0	23[3]	O	**TDO** — Test Data Out for JTAG interface.
		I/O	**PIO1_1** — General purpose digital input/output pin.
		I	**AD2** — A/D converter, input 2.
		O	**CT32B1_MAT0** — Match output 0 for 32-bit timer 1.
$\overline{\text{TRST}}$/PIO1_2/AD3/ CT32B1_MAT1	24[3]	I	**$\overline{\text{TRST}}$** — Test Reset for JTAG interface.
		I/O	**PIO1_2** — General purpose digital input/output pin.
		I	**AD3** — A/D converter, input 3.
		O	**CT32B1_MAT1** — Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/AD4/ CT32B1_MAT2	25[3]	I/O	**SWDIO** — Serial wire debug input/output.
		I/O	**PIO1_3** — General purpose digital input/output pin.
		I	**AD4** — A/D converter, input 4.
		O	**CT32B1_MAT2** — Match output 2 for 32-bit timer 1.
PIO1_4/AD5/ CT32B1_MAT3/WAKEUP	26[3]	I/O	**PIO1_4** — General purpose digital input/output pin.
		I	**AD5** — A/D converter, input 5.
		O	**CT32B1_MAT3** — Match output 3 for 32-bit timer 1.
		I	**WAKEUP** — Deep power-down mode wake-up pin.
PIO1_5/$\overline{\text{RTS}}$/ CT32B0_CAP0	30[1]	I/O	**PIO1_5** — General purpose digital input/output pin.
		O	**$\overline{\text{RTS}}$** — Request To Send output for UART.
		I	**CT32B0_CAP0** — Capture input 0 for 32-bit timer 0.
PIO1_6/RXD/ CT32B0_MAT0	31[1]	I/O	**PIO1_6** — General purpose digital input/output pin.
		I	**RXD** — Receiver input for UART.
		O	**CT32B0_MAT0** — Match output 0 for 32-bit timer 0.
PIO1_7/TXD/ CT32B0_MAT1	32[1]	I/O	**PIO1_7** — General purpose digital input/output pin.
		O	**TXD** — Transmitter output for UART.
		O	**CT32B0_MAT1** — Match output 1 for 32-bit timer 0.
PIO1_8/CT16B1_CAP0	7[1]	I/O	**PIO1_8** — General purpose digital input/output pin.
		I	**CT16B1_CAP0** — Capture input 0 for 16-bit timer 1.
PIO1_9/CT16B1_MAT0	12[1]	I/O	**PIO1_9** — General purpose digital input/output pin.
		O	**CT16B1_MAT0** — Match output 0 for 16-bit timer 1.
PIO1_10/AD6/ CT16B1_MAT1	20[3]	I/O	**PIO1_10** — General purpose digital input/output pin.
		I	**AD6** — A/D converter, input 6.
		O	**CT16B1_MAT1** — Match output 1 for 16-bit timer 1.
PIO1_11/AD7	27[3]	I/O	**PIO1_11** — General purpose digital input/output pin.
		I	**AD7** — A/D converter, input 7.
PIO2_0		I/O	**Port 2** — Port 2 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 2 pins depends on the function selected through the IOCONFIG register block. Pins PIO2_1 to PIO2_11 are not available.

Table 5. LPC1111/12/13/14 pin description table (HVQFN33 package) *…continued*

Symbol	Pin	Type	Description
PIO2_0/$\overline{DTR}$	1[1]	I/O	**PIO2_0 —** General purpose digital input/output pin.
		O	**$\overline{DTR}$ —** Data Terminal Ready output for UART.
PIO3_0 to PIO3_5		I/O	**Port 3 —** Port 3 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 3 pins depends on the function selected through the IOCONFIG register block. Pins PIO3_0, PIO3_1, PIO3_3 and PIO3_6 to PIO3_11 are not available.
PIO3_2	28[1]	I/O	**PIO3_2 —** General purpose digital input/output pin.
PIO3_4	13[1]	I/O	**PIO3_4 —** General purpose digital input/output pin.
PIO3_5	14[1]	I/O	**PIO3_5 —** General purpose digital input/output pin.
$V_{DD(IO)}$	6[4]	I	3.3 V input/output supply voltage.
$V_{DD(3V3)}$	29[4]	I	3.3 V supply voltage to the internal DC-DC converter and the ADC. Also used as the ADC reference voltage.
XTALIN	4[5]	I	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	5[5]	O	Output from the oscillator amplifier.
V_{SS}	33	-	Thermal pad. Connect to ground.

[1] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[2] I^2C-bus pads compliant with the I^2C-bus specification for I^2C standard mode and I^2C Fast-mode Plus.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled, and the pin is not 5 V tolerant.

[4] Tie together $V_{DD(3V3)}$ and $V_{DD(IO)}$ externally. If separate supplies are used for $V_{DD(3V3)}$ and $V_{DD(IO)}$, ensure that the voltage difference between both supplies is smaller than or equal to 0.5 V.

[5] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

7. Functional description

7.1 ARM Cortex-M0 processor

The ARM Cortex-M0 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption.

7.2 On-chip flash program memory

The LPC1111/12/13/14 contain 32 kB (LPC1114), 24 kB (LPC1113), 16 kB (LPC1112), or 8 kB (LPC1111) of on-chip flash memory.

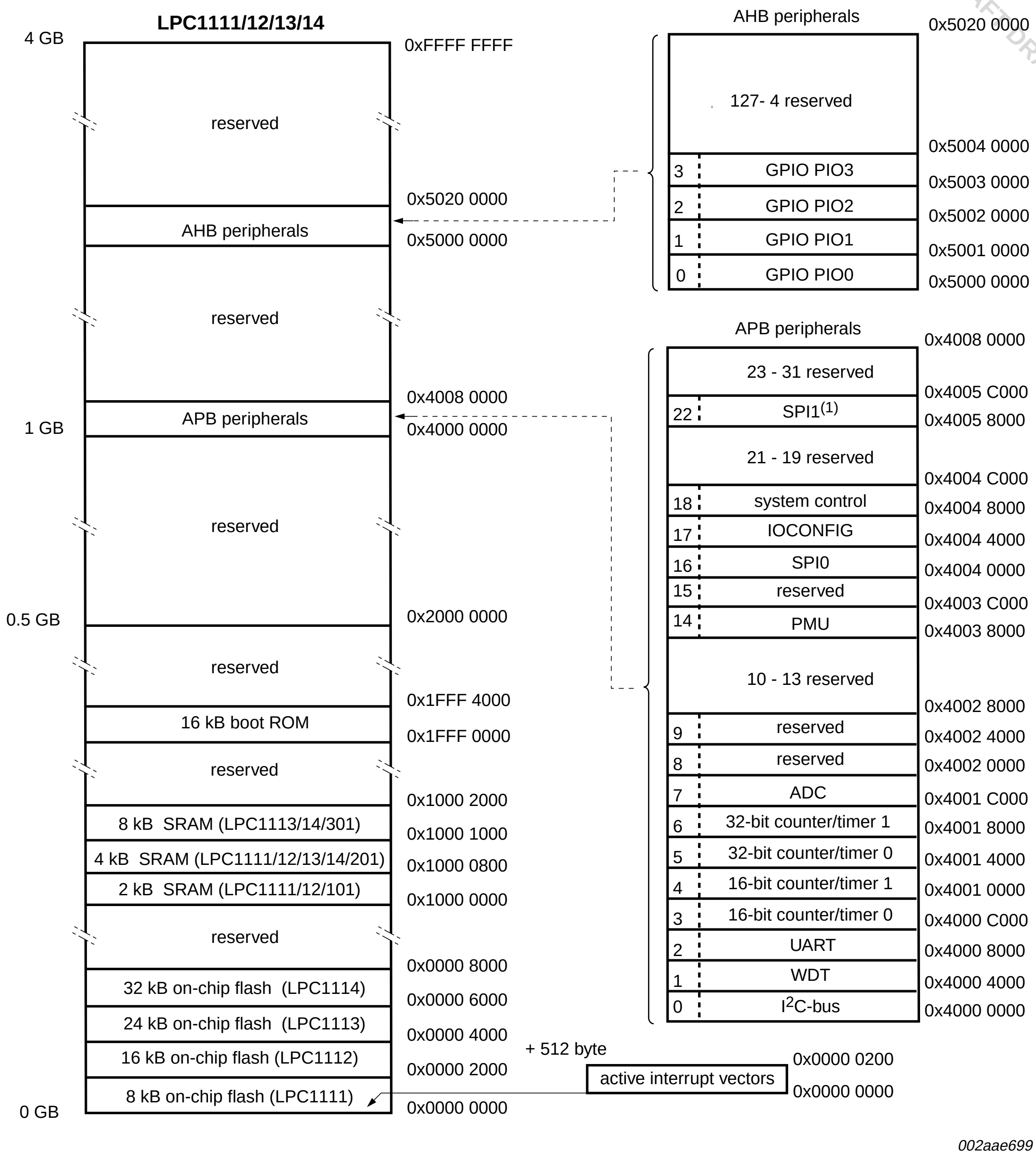
7.3 On-chip SRAM

The LPC1111/12/13/14 contain a total of 8 kB, 4 kB, or 2 kB on-chip static RAM memory.

7.4 Memory map

The LPC1111/12/13/14 incorporates several distinct memory regions, shown in the following figures. Figure 5 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 megabyte in size, and is divided to allow for up to 128 peripherals. The APB peripheral area is 1 megabyte in size and is divided to allow for up to 64 peripherals. Each peripheral of either type is allocated 16 kilobytes of space. This allows simplifying the address decoding for each peripheral.



(1) LQFP48/PLCC44 packages only.

Fig 5. LPC1111/12/13/14 memory map

7.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.

- In the LPC1111/12/13/14, the NVIC supports 32 vectored interrupts including up to 13 inputs to the start logic from individual GPIO pins.
- 8 programmable interrupt priority levels, with hardware priority level masking
- Relocatable vector table.
- Software interrupt generation.

7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any GPIO pin (total of up to 42 pins) regardless of the selected function, can be programmed to generate an interrupt on a level, or rising edge or falling edge, or both.

7.6 IOCONFIG block

The IOCONFIG block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

7.7 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back as well as the current state of the port pins.

LPC1111/12/13/14 use accelerated GPIO functions:

- GPIO registers are a dedicated AHB peripheral and are accessed through the AHB so that the fastest possible I/O timing can be achieved.
- Entire port value can be written in one instruction.

Additionally, any GPIO pin (total of up to 42 pins) providing a digital function can be programmed to generate an interrupt on a level, a rising or falling edge, or both.

7.7.1 Features

- Bit level set and clear registers allow a single instruction to set or clear any number of bits in one port.
- Direction control of individual bits.
- All I/O default to inputs with pull-ups enabled after reset.
- Pull-up/pull-down resistor configuration can be programmed through the IOCONFIG block for each GPIO pin.

7.8 UART

The LPC1111/12/13/14 contains one UART.

Support for RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The UART includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.8.1 Features

- 16 Byte Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.

7.9 SPI serial I/O controller

The LPC1111/12/13/14 contain two SPI controllers on the LQFP48/PLCC44 packages and one SPI controller on the HVQFN33 packages (SPI0). Both SPI controllers support SSP features.

The SPI controller is capable of operation on a SSP, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SPI supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.9.1 Features

- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

7.10 I^{2}C-bus serial I/O controller

The LPC1111/12/13/14 contain one I^{2}C-bus controller.

The I^{2}C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^{2}C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.10.1 Features

- The I^{2}C-interface is a standard I^{2}C compliant bus interface with open-drain pins. I^{2}C0 also supports Fast mode plus with bit rates up to 1 Mbit/s.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^{2}C-bus can be used for test and diagnostic purposes.
- The I^{2}C-bus controller supports multiple address recognition and a bus monitor mode.

7.11 10-bit ADC

The LPC1111/12/13/14 contains one ADC. It is a single 10-bit successive approximation ADC with eight channels.

7.11.1 Features

- 10-bit successive approximation ADC.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 V to $V_{DD(3V3)}$.
- 10-bit conversion time $\geq$ 2.44 μs.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or Timer Match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.

7.12 General purpose external event counters/timers

The LPC1111/12/13/14 includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.12.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- One capture channel per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

7.13 System tick timer

The ARM Cortex-M0 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a 10 ms interval.

7.14 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to ‘feed’ (or reload) the watchdog within a predetermined amount of time.

7.14.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the Internal RC oscillator (IRC), the Watchdog oscillator, or the main clock. This gives a wide range of potential timing choices of Watchdog operation under different power reduction conditions. It also provides the ability to run the WDT from an entirely internal source that is not dependent on an external crystal and its associated components and wiring for increased reliability.

7.15 Clocking and power control

7.15.1 Crystal oscillators

The LPC1111/12/13/14 include three independent oscillators. These are the system oscillator, the Internal RC oscillator (IRC), and the Watchdog oscillator. Each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the LPC1111/12/13/14 will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 6 for an overview of the LPC1111/12/13/14 clock generation.

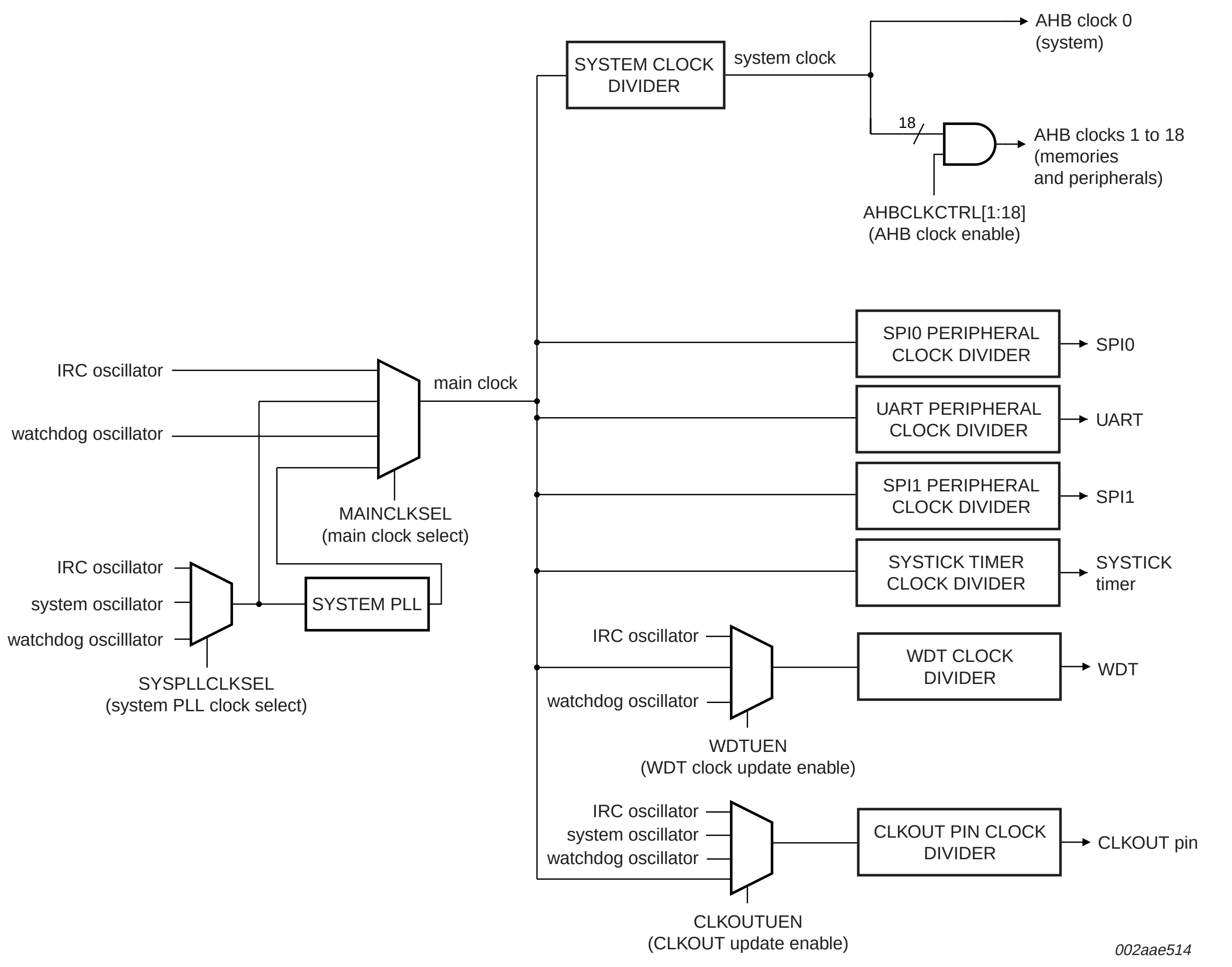


Fig 6. LPC1111/12/13/14 clocking generation block diagram

7.15.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

Upon power-up or any chip reset, the LPC1111/12/13/14 use the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.15.1.2 System oscillator

The system oscillator can be used as the clock source for the CPU, with or without using the PLL.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL. The ARM processor clock frequency is referred to as CCLK elsewhere in this document.

7.15.2 System PLL (PLL0)

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

7.15.3 Clock output

The LPC1111/12/13/14 features a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

7.15.4 Wake-up process

The LPC1111/12/13/14 begin operation at power-up and when awakened from Deep power-down mode by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

7.15.5 Power control

The LPC1111/12/13/14 support a variety of power control features. There are three special modes of processor power reduction: Sleep mode, Deep-sleep mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.15.5.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.15.5.2 Deep-sleep mode

In Deep-sleep mode, the chip is in Sleep mode, and in addition analog blocks are shut down for increased power savings. The user can configure the Deep-sleep mode to a large extend, selecting any of the oscillators, any of the PLLs, BOD, the ADC, and the flash to be shut down or remain powered during Deep-sleep mode. The user can also select which of the oscillators and analog blocks will be powered up after the chip exits from Deep-sleep mode.

The GPIO pins (up to 15 pins total) serve as external wake-up pins to a dedicated start logic to wake up the chip from Deep-sleep mode.

The timing of the wake-up process from Deep-sleep mode depends on which blocks are selected to be powered down during deep-sleep.

For lowest power consumption, the clock source should be switched to IRC before entering Deep-sleep mode, all oscillators and PLLs should be turned off during deep-sleep, and the IRC should be selected as clock source when the chip wakes up from deep-sleep. The IRC can be switched on and off glitch-free and provides a clean clock signal after start-up.

If power consumption is not a concern, any of the oscillators and/or PLLs can be left running in Deep-sleep mode to obtain short wake-up times when waking up from deep-sleep.

7.15.5.3 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip with the exception of the WAKEUP pin. The LPC1111/12/13/14 can wake up from Deep power-down mode via the WAKEUP pin.

7.16 System control

7.16.1 Reset

Reset has four sources on the LPC1111/12/13/14: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

7.16.2 Brownout detection

The LPC1111/12/13/14 includes four levels for monitoring the voltage on the $V_{DD(3V3)}$ pin. If this voltage falls below one of the four selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; if not, software can monitor the signal by reading a dedicated status register. An additional threshold level can be selected to cause a forced reset of the chip.

7.16.3 Code security (Code Read Protection - CRP)

This feature of the LPC1111/12/13/14 allows user to enable different levels of security in the system so that access to the on-chip flash and use of the JTAG and ISP can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

There are three levels of Code Read Protection:

1. CRP1 disables access to chip via the JTAG and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.
2. CRP2 disables access to chip via the JTAG and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected fully disables any access to chip via the JTAG pins and the ISP. This mode effectively disables ISP override using PIO0_1 pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via UART0.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_1 for valid user code can be disabled. For details see the *LPC11xx user manual*.

7.16.4 APB interface

The APB peripherals are located on one APB bus.

7.16.5 AHBLite

The AHBLite connects the CPU bus of the ARM Cortex-M0 to the flash memory, the main static RAM, and the Boot ROM.

7.16.6 External interrupt inputs

All GPIO pins can be level or edge sensitive interrupt inputs.

7.16.7 Memory mapping control

The Cortex-M0 incorporates a mechanism that allows remapping the interrupt vector table to alternate locations in the memory map. This is controlled via the Vector Table Offset Register contained in the NVIC.

The vector table may be located anywhere within the bottom 1 GB of Cortex-M0 address space. The vector table must be located on a 128 word (512 byte) boundary.

7.17 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0. Serial wire debug with four breakpoints and two watchpoints is supported.

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)	core and external rail		1.8	3.6	V
$V_{DD(IO)}$	input/output supply voltage	on pin V_{DDIO}		1.8	3.6	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the $V_{DD(IO)}$ supply voltage is present	[2]	–0.5	+5.5	V
I_{DD}	supply current	per supply pin	[3]	-	100	mA
I_{SS}	ground current	per ground pin	[3]	-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(IO)}) < V_I < (1.5V_{DD(IO)})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[4]	–65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model; all pins	[5]	–5000	+5000	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] The peak current is limited to 25 times the corresponding maximum current.

[4] Dependent on package type.

[5] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

9. Static characteristics

Table 7. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)			1.8	3.3	3.6	V
$V_{DD(IO)}$	input/output supply voltage			1.8	3.3	3.6	V
I_{DD}	supply current	active mode; $V_{DD(3V3)}$ = 3.3 V; T_{amb} = 25 °C; code `while(1){}` executed from flash; all peripherals enabled					
		CCLK = 10 MHz		-	<tbd>	-	mA
		CCLK = 50 MHz		-	<tbd>	-	mA
		Sleep mode; $V_{DD(3V3)}$ = 3.3 V; T_{amb} = 25 °C		-	<tbd>	-	μA
		Deep-sleep mode; $V_{DD(3V3)}$ = 3.3 V; T_{amb} = 25 °C		-	<tbd>	-	μA
		Deep power-down mode; $V_{DD(3V3)}$ = 3.3 V; T_{amb} = 25 °C		-	<tbd>	-	μA
Standard port pins, RESET							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	-	3	μA
I_{IH}	HIGH-level input current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	-	3	μA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD(IO)}$; on-chip pull-up/down resistors disabled		-	-	3	μA
V_I	input voltage	pin configured to provide a digital function	[2][3][4]	0	-	5.0	V
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	[5]	$V_{DD(IO)}$ − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	[5]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)}$ − 0.4 V	[5]	−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[5]	4	-	-	mA

Table 7. Static characteristics *...continued*

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[6]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(IO)}$	[6]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V		−15	−50	−85	μA
		$V_{DD(IO)} < V_I < 5$ V		0	0	0	μA
High-drive output pin (PIO0_7)							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	-	3	μA
I_{IH}	HIGH-level input current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	-	3	μA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD(IO)}$; on-chip pull-up/down resistors disabled		-	-	3	μA
V_I	input voltage	pin configured to provide a digital function	[2][3][4]	0	-	5.0	V
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	[5]	$V_{DD(IO)}$ − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	[5]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V	[5]	20	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[5]	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[6]	10	50	150	μA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(IO)}$	[6]	−15	−50	−85	μA
I_{pd}	pull-down current	V_I = 5 V		0	0	0	μA
I_{pu}	pull-up current	V_I = 0 V		-	-	3	μA
		$V_{DD(IO)} < V_I < 5$ V		-	-	3	μA
I^2C-bus pins (PIO0_4 and PIO0_5)							
V_{IH}	HIGH-level input voltage			$0.7V_{DD(IO)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			-	$0.5V_{DD(IO)}$	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 20 mA	[5]	-	-	0.4	V

Table 7. Static characteristics *...continued*

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{LI}	input leakage current	$V_I = V_{DD(IO)}$	[7]	-	2	4	μA
		V_I = 5 V		-	10	22	μA
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage			0	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage			0	1.8	1.95	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] Including voltage on outputs in 3-state mode.

[3] $V_{DD(3V3)}$ and $V_{DD(IO)}$ supply voltages must be present.

[4] 3-state outputs go into 3-state mode when $V_{DD(IO)}$ is grounded.

[5] Accounts for 100 mV voltage drop in all supply lines.

[6] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[7] To V_{SS}.

Table 8. ADC static characteristics

T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 4.5 MHz, $V_{DD(3V3)}$ = 2.5 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{IA}	analog input voltage			0	-	$V_{DD(3V3)}$	V
C_{ia}	analog input capacitance			-	-	1	pF
E_D	differential linearity error		[2][3][4]	-	± 1	-	LSB
$E_{L(adj)}$	integral non-linearity		[2][5]	-	± 1.5	-	LSB
E_O	offset error		[2][6]	-	± 2.5	-	LSB
E_G	gain error		[2][7]	-	0.5	-	%
E_T	absolute error		[2][8]	-	± 3	-	LSB

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] Conditions: V_{SS} = 0 V, $V_{DD(3V3)}$ = 3.3 V.

[3] The ADC is monotonic, there are no missing codes.

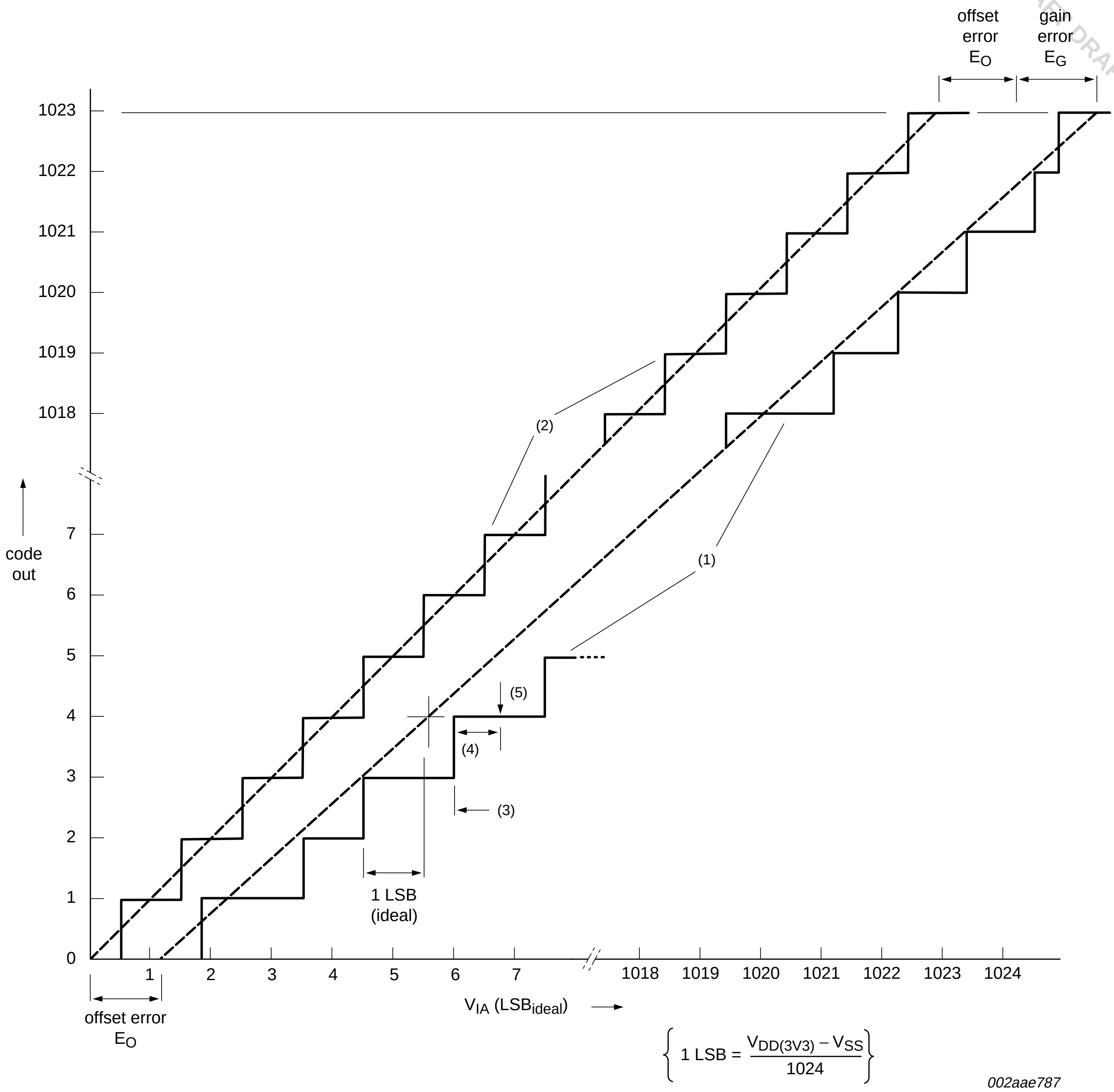
[4] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 7.

[5] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 7.

[6] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 7.

[7] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 7.

[8] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 7.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 7. ADC characteristics

9.1 BOD static characteristics

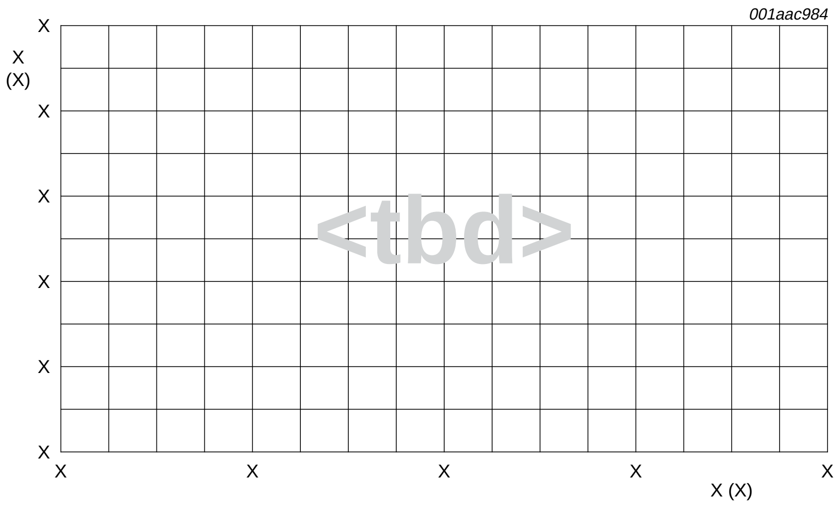
Table 9. BOD static characteristics[1]

T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 0				
		assertion	-	1.69	-	V
		de-assertion	-	1.84	-	V
		interrupt level 1				
		assertion	-	2.29	-	V
		de-assertion	-	2.44	-	V
		interrupt level 2				
		assertion	-	2.59	-	V
		de-assertion	-	2.74	-	V
		interrupt level 3				
		assertion	-	2.87	-	V
		de-assertion	-	2.98	-	V
		reset level 0				
		assertion	-	1.49	-	V
		de-assertion	-	1.64	-	V

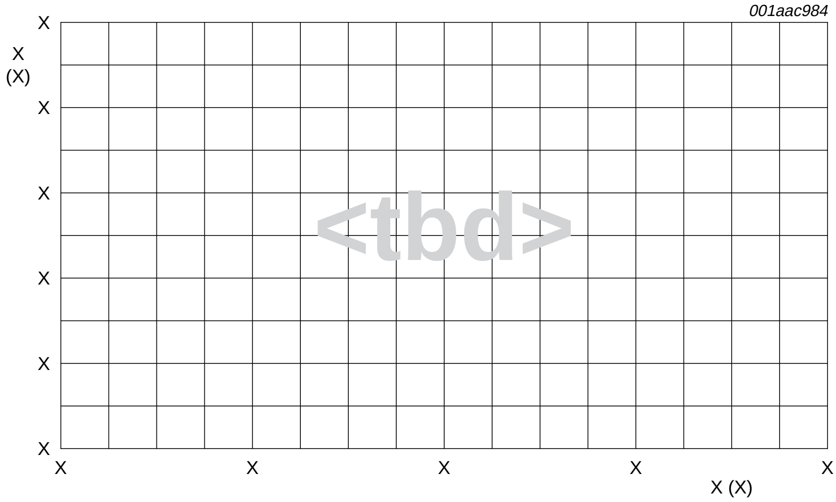
[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *LPC11xx user manual*.

9.2 Power consumption



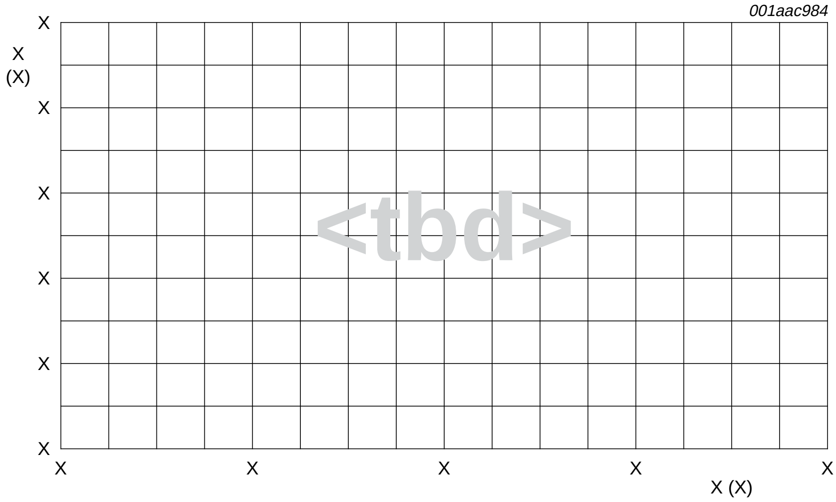
Conditions: T_{amb} = 25 °C; active mode entered executing code from flash; core voltage 3.3 V; all peripherals enabled but not configured to run.

Fig 8. Supply current at different core frequencies in active mode



Conditions: T_{amb} = 25 °C; active mode entered executing code from flash; all peripherals enabled but not configured to run.

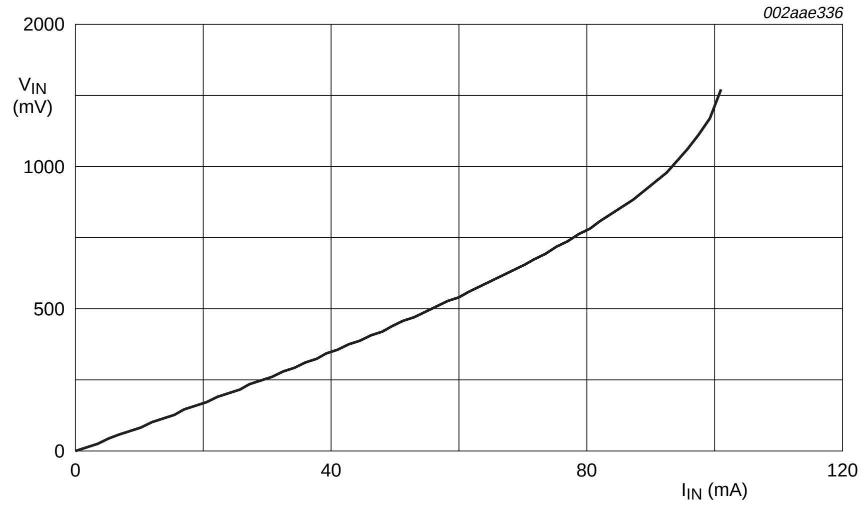
Fig 9. Supply current at different core voltages in active mode



Conditions: active mode entered executing code from flash; core voltage 3.3 V; all peripherals enabled but not configured to run.

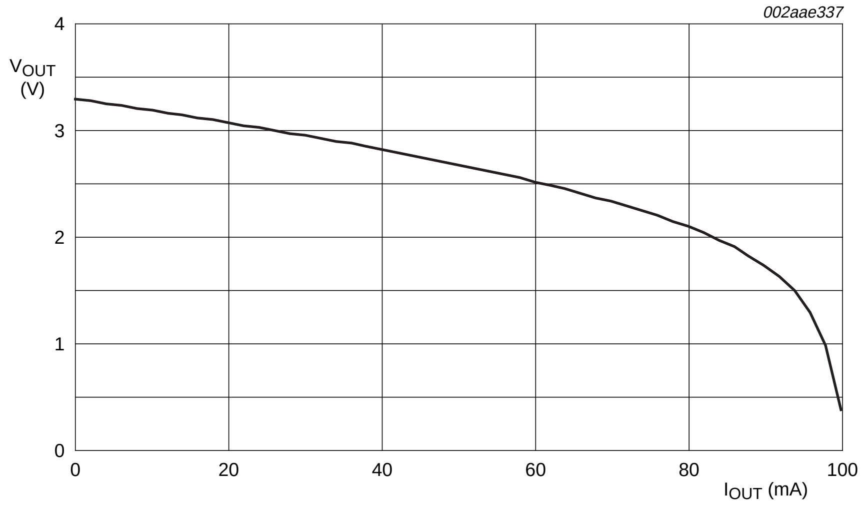
Fig 10. Supply current at different temperatures in active mode

9.3 Electrical pin characteristics



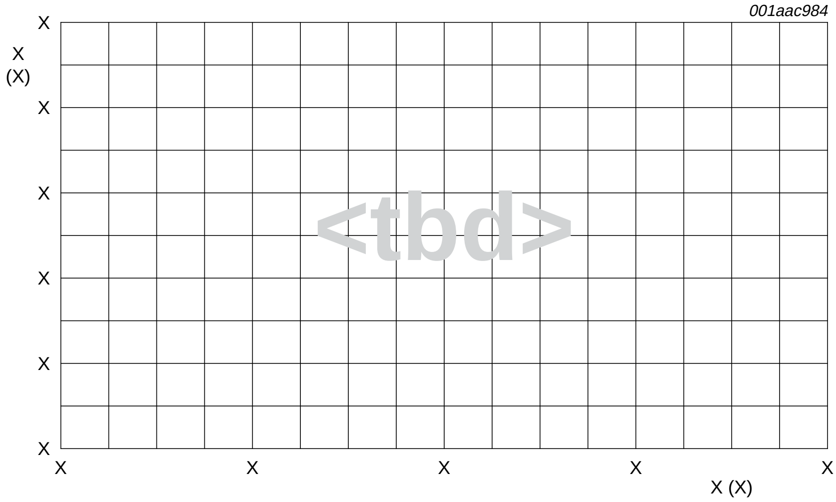
Conditions: $V_{DD(IO)}$ = 3.3 V; T_{amb} = 25 °C.

Fig 11. I²C-bus current (I_{IL} vs. V_{IL})



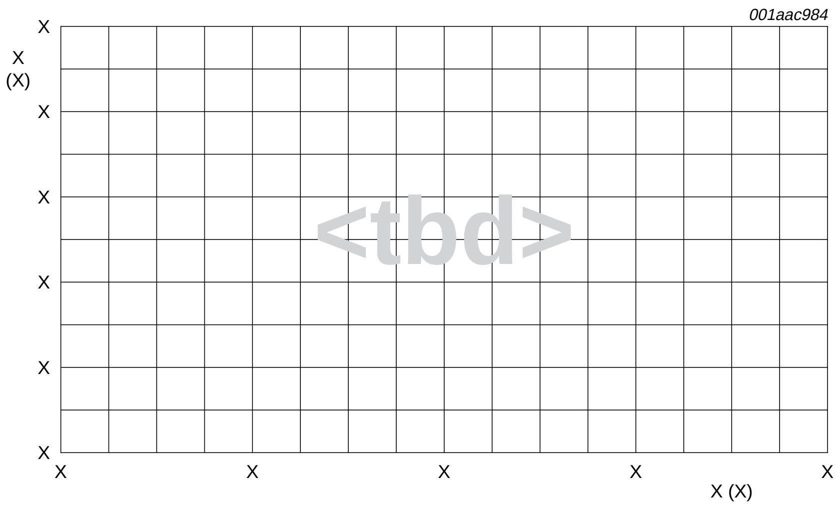
Conditions: $V_{DD(IO)}$ = 3.3 V; T_{amb} = 25 °C.

Fig 12. High drive output (I_{OH} vs. V_{OH}) on pin PIO0_7



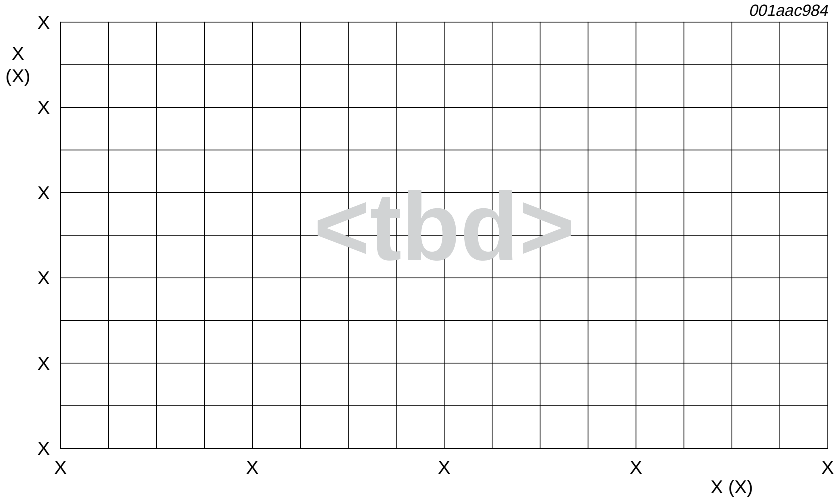
Measured on pins Pn.m; $V_{DD(3V3)}$ = x.x V.

Fig 13. Typical LOW-level output I_{OL} current versus LOW-level output V_{OL}



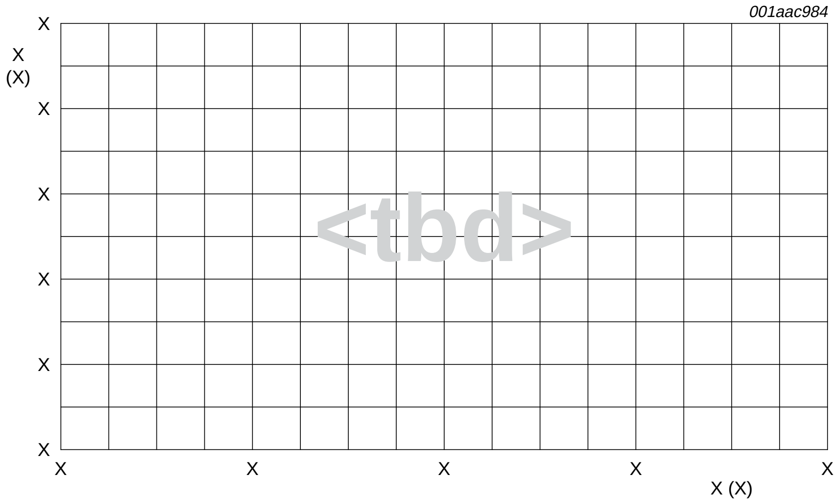
Measured on pins Pn.m; $V_{DD(3V3)}$ = x.x V.

Fig 14. Typical HIGH-level output I_{OH} current versus HIGH-level output voltage V_{OH}



Measured on pins Pn.m; $V_{DD(3V3)}$ = x.x V.

Fig 15. Typical pull-up current I_{pu} versus input voltage V_i



Measured on pins Pn.m; $V_{DD(3V3)}$ = x.x V.

Fig 16. Typical pull-down current I_{pd} versus input voltage V_i

10. Dynamic characteristics

10.1 Flash memory

Table 10. Flash characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	-	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		20	-	-	years

[1] Number of program/erase cycles.

10.2 External clock

Table 11. Dynamic characteristic: external clock

T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

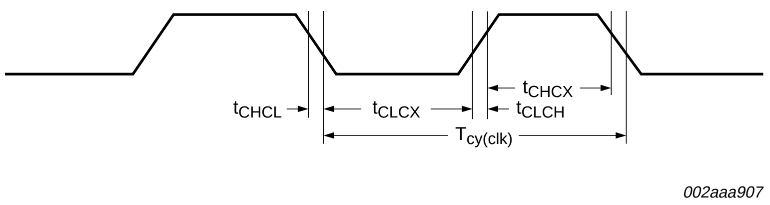


Fig 17. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

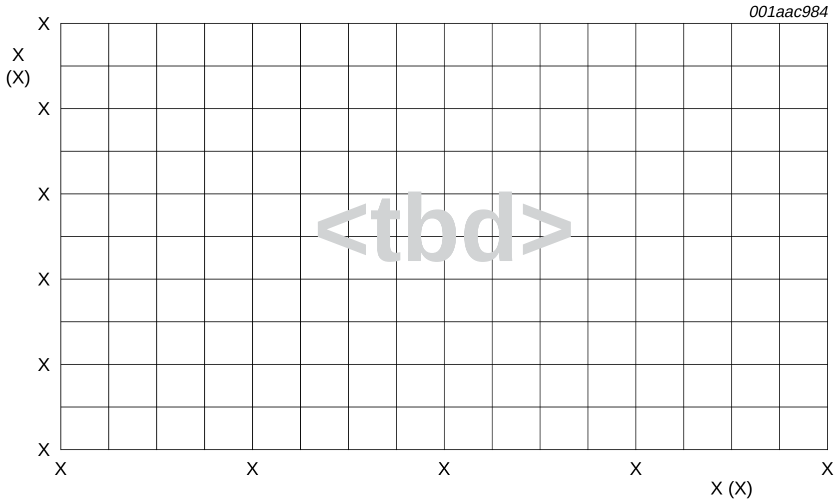
10.3 Internal oscillators

Table 12. Dynamic characteristic: internal oscillators
T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	11.88	12	12.12	MHz

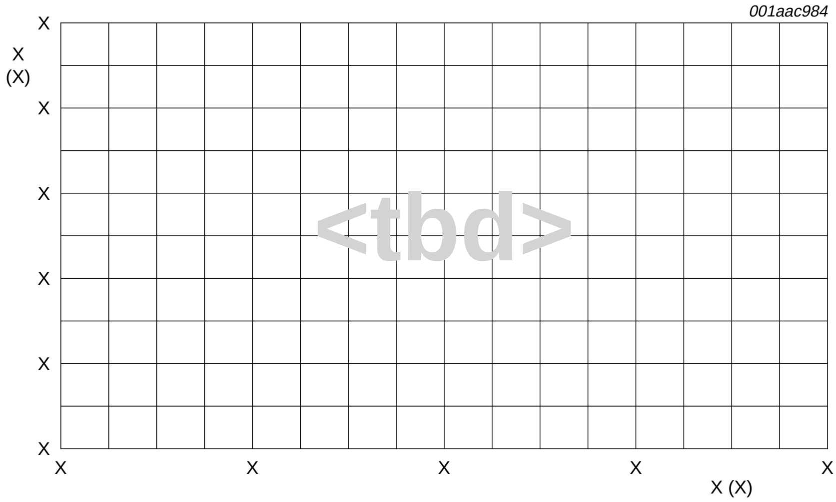
[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



conditions: <tbd>

Fig 18. Internal RC oscillator frequency vs. temperature



conditions: <tbd>

Fig 19. Internal RC oscillator frequency vs. core voltage

10.4 I²C-bus

Table 13. Dynamic characteristic: I²C-bus pins (Fast-mode Plus)

T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ = $V_{DD(IO)}$ = 3.3 V.[1][2][3]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency		-	-	1	MHz
t_f	fall time		-	-	45	ns
$t_{SU;DAT}$	data set-up time	-	50	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Main clock frequency 10 MHz; system clock divider AHBCLKDIV = 0x1; I²C-bus interface configured in master mode.

[3] Bus capacitance C_b = 550 pF; external pull-up resistance of 103 Ω.

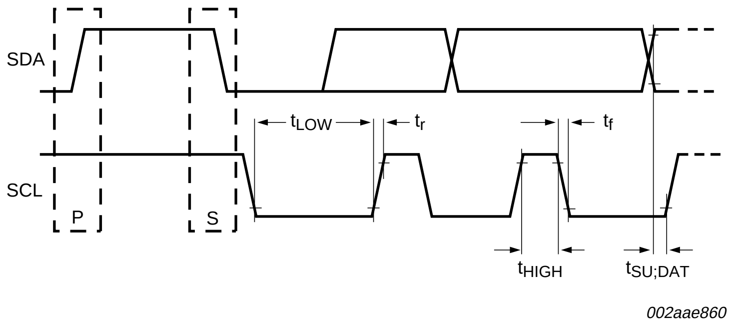


Fig 20. I²C-bus pins clock timing

10.5 SPI interfaces

Table 14. Dynamic characteristics of SPI pins in SPI mode

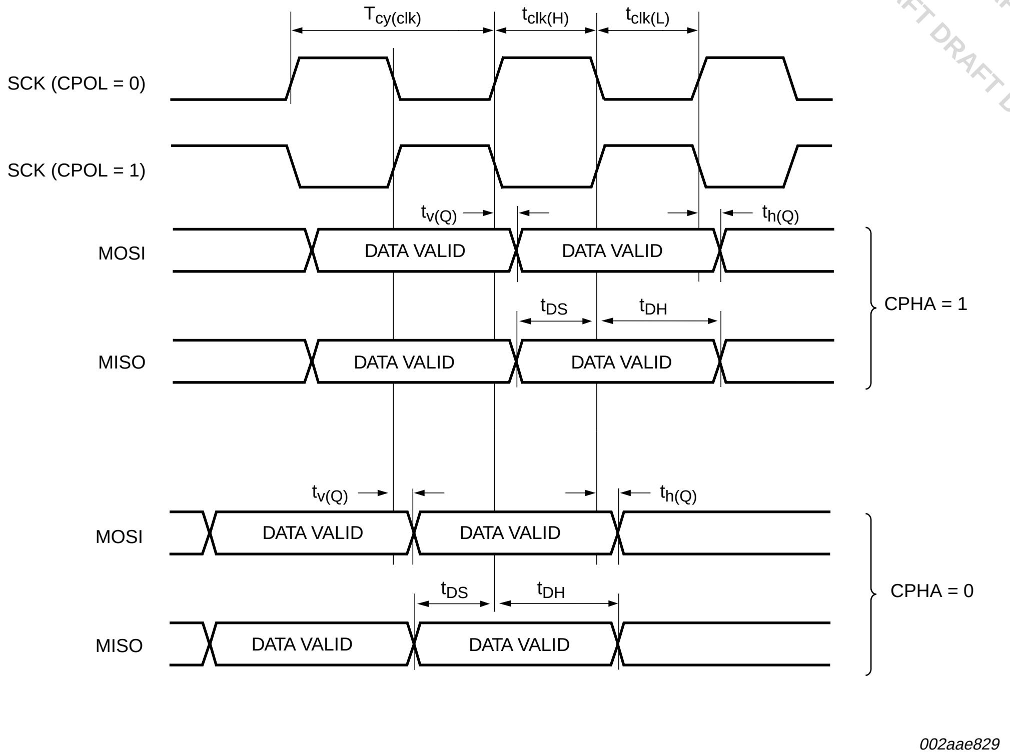
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$T_{cy(PCLK)}$	PCLK cycle time			13.9	-	-	ns
$T_{cy(clk)}$	clock cycle time		[1]	27.8	-	-	ns
SPI master (in SPI mode)							
t_{DS}	data set-up time	in SPI mode	[2]	15	-	$T_{cy(clk)}$	ns
t_{DH}	data hold time	in SPI mode	[2]	-	-	0	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[2]	-	-	10	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[2]	-	-	0	ns
SPI slave (in SPI mode)							
t_{DS}	data set-up time	in SPI mode	[3][4]	0	-	-	ns
t_{DH}	data hold time	in SPI mode	[3][4]	$3 \times T_{cy(PCLK)} + 4$	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[3][4]	-	-	$3 \times T_{cy(PCLK)} + 11$	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[3][4]	-	-	$2 \times T_{cy(PCLK)} + 5$	ns

[1] $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSDVSR) / f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SPI peripheral clock divider (SSPCLKDIV), the SPI SCR parameter (specified in the SSP0CR0 register), and the SPI CPSDVSR parameter (specified in the SPI clock prescale register).

[2] T_{amb} = –40 °C to 85 °C; $V_{DD(3V3)}$ = 2.0 V to 3.6 V; $V_{DD(IO)}$ = 2.0 V to 3.6 V.

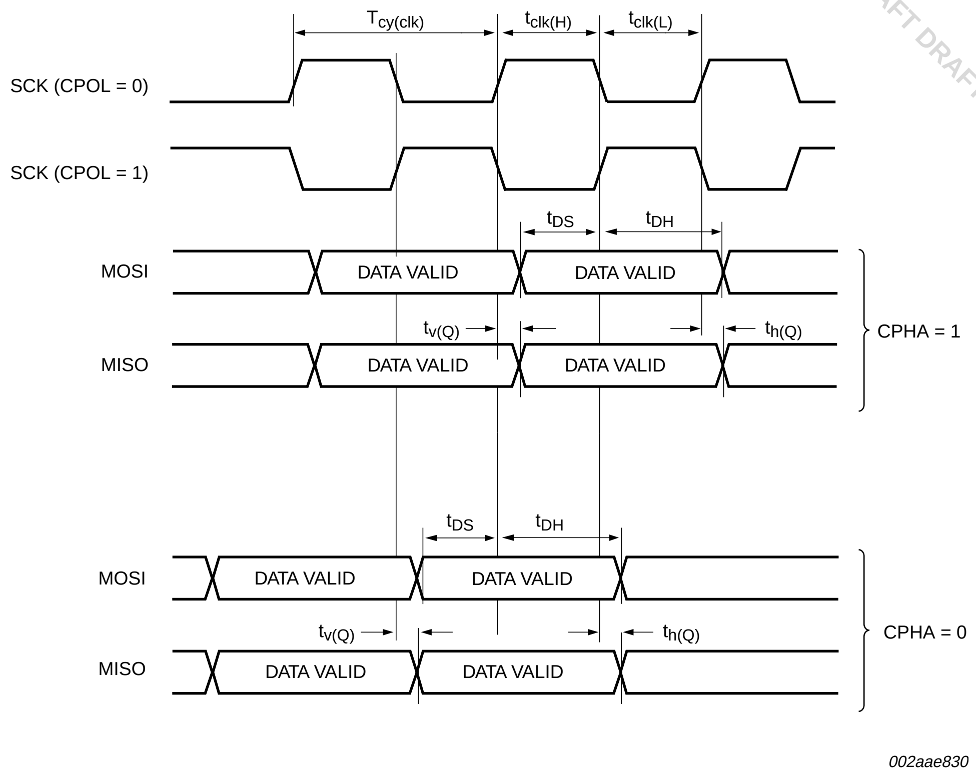
[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$.

[4] T_{amb} = 25 °C; $V_{DD(3V3)}$ = 3.3 V; $V_{DD(IO)}$ = 3.3 V.



Pin names SCK, MISO, and MOSI refer to pins for both SPI peripherals, SPI0 and SPI1.

Fig 21. SPI master timing in SPI mode



Pin names SCK, MISO, and MOSI refer to pins for both SPI peripherals, SPI0 and SPI1.

Fig 22. SPI slave timing in SPI mode

11. Application information

11.1 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

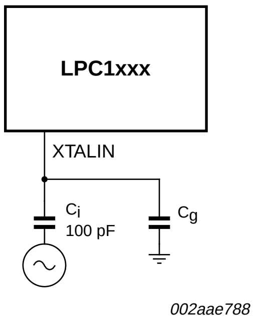


Fig 23. Slave mode operation of the on-chip oscillator

11.2 XTAL Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1},C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

11.3 Standard I/O pad configuration

Figure 24 shows the possible pin modes for standard I/O pins. The pull-up and pull-down resistors (R_{pu} and R_{pd}) can be enabled or disabled. The default value for each standard port pin is input with R_{pu} enabled. For details on pin modes and hysteresis control, see the *LPC11xx user manual*.

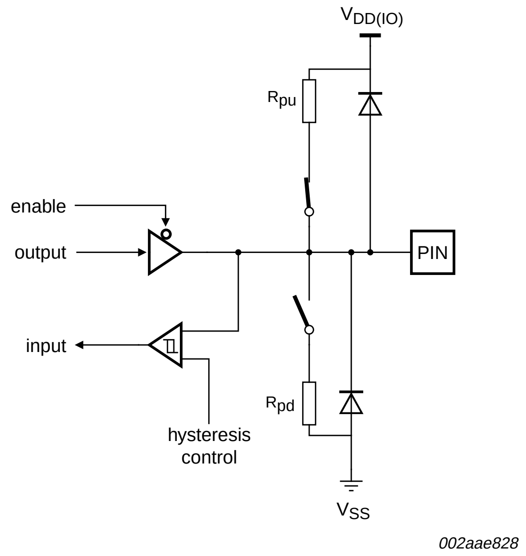
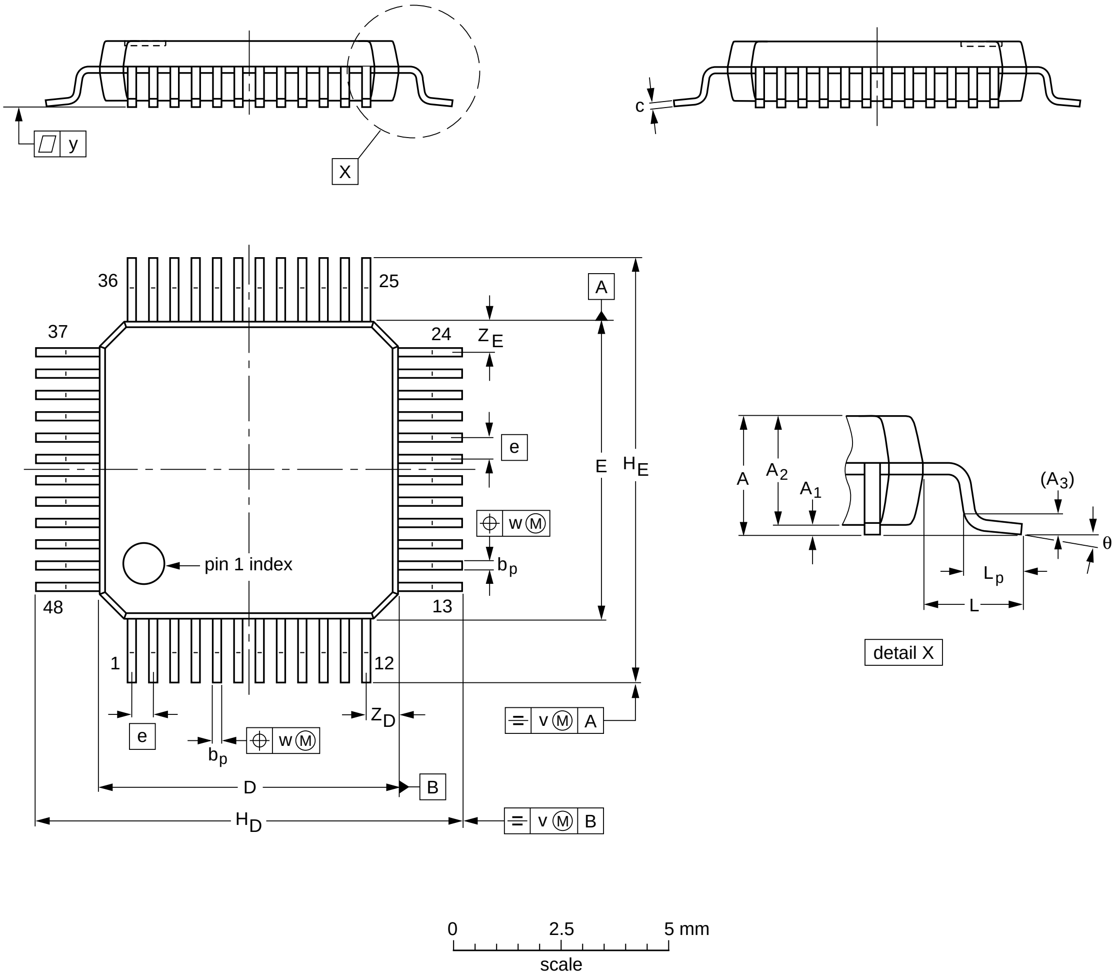


Fig 24. Standard I/O pad configuration

12. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

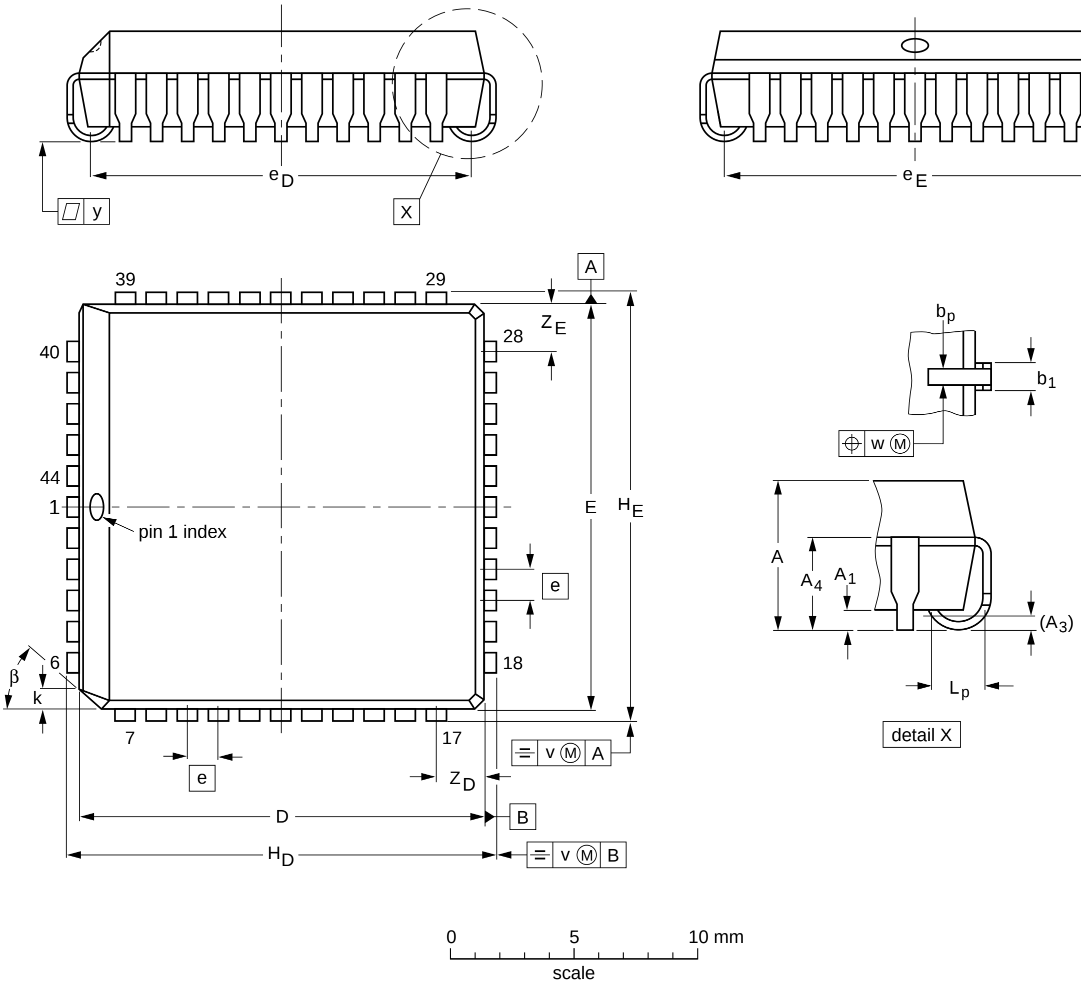
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 25. Package outline SOT313-2 (LQFP48)

PLCC44: plastic leaded chip carrier; 44 leads **SOT187-2**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.63 0.59	0.63 0.59	0.695 0.685	0.695 0.685	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

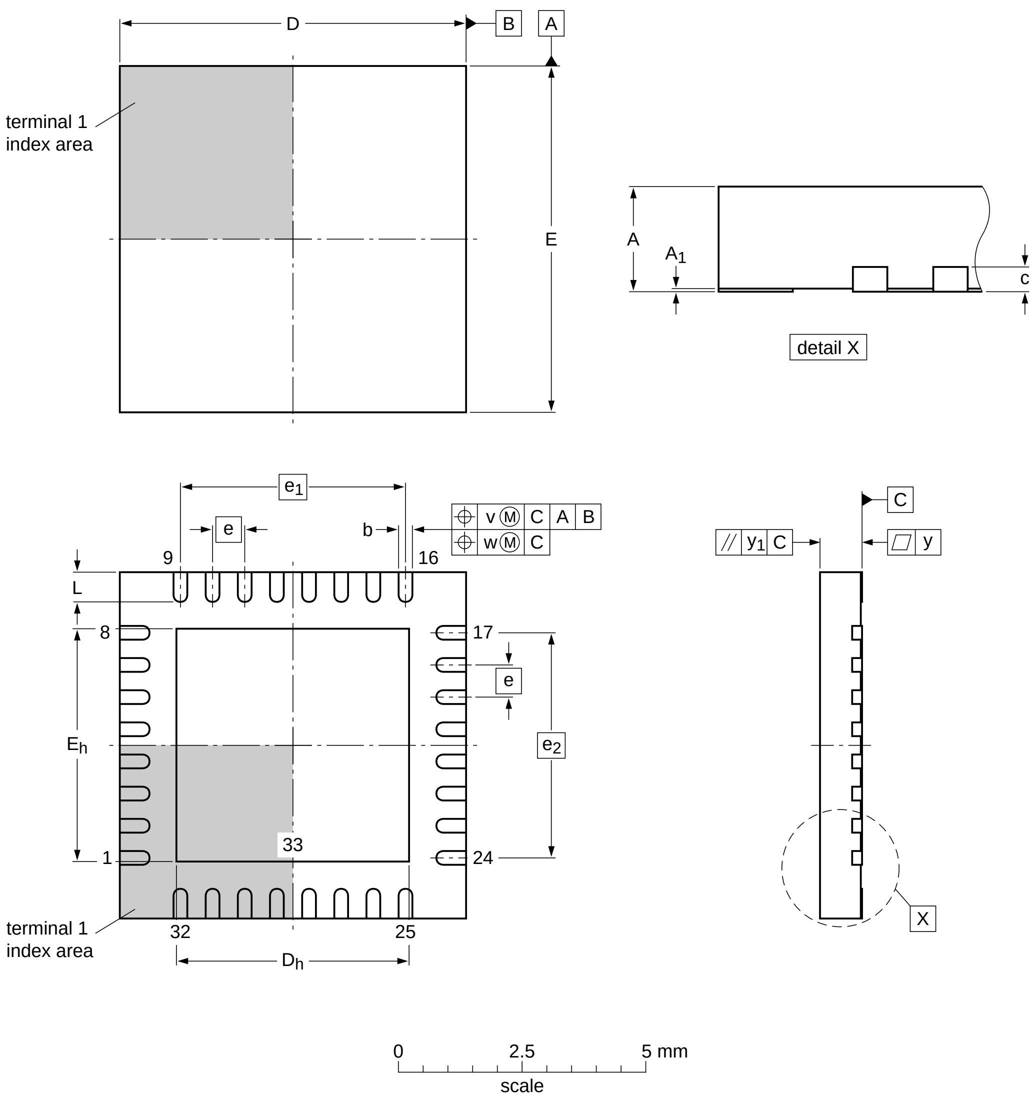
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT187-2	112E10	MS-018	EDR-7319			~~99-12-27~~ 01-11-14

Fig 26. Package outline PLCC44

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 x 7 x 0.85 mm



Dimensions

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	1.00	0.05	0.35		7.1	4.85	7.1	4.85				0.75				
	nom	0.85	0.02	0.28	0.2	7.0	4.70	7.0	4.70	0.65	4.55	4.55	0.60	0.1	0.05	0.08	0.1
	min	0.80	0.00	0.23		6.9	4.55	6.9	4.55				0.45				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

hvqfn33_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
			- - -			~~09-03-17~~ 09-03-23

Fig 27. Package outline (HVQFN33)

13. Abbreviations

Table 15. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
ETM	Embedded Trace Macrocell
GPIO	General Purpose Input/Output
PLL	Phase-Locked Loop
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter

14. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC1111_12_13_14_0.11	<tbd>	Objective data sheet	-	LPC1111_12_13_0.09
Modifications:	• Part LPC1114 added. • Parts LPC1111/101, LPC1112/101 added. • Flash and SRAM configuration changed (see Table 2).			
LPC1111_12_13_0.09	<tbd>	Objective data sheet	-	LPC1111_13_0.06
Modifications:	• Part LPC1112 added. • PLCC44 package added.			
LPC1111_13_0.06	<tbd>	Objective data sheet	-	LPC1111_13_0.05
Modifications:	SWO removed from pin description			
LPC1111_13_0.05	<tbd>	Objective data sheet	-	LPC1111_13_0.04
Modifications:	Editorial updates.			
LPC1111_13_0.04	<tbd>	Objective data sheet	-	LPC11xx_0.03
Modifications:	SPI1 interface added for LQFP48 packages.			
LPC11xx_0.03	<tbd>	Objective data sheet	-	-

15. Legal information

16. Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Date of release: 13 November 2009
Document identifier: LPC1111_12_13_14_0