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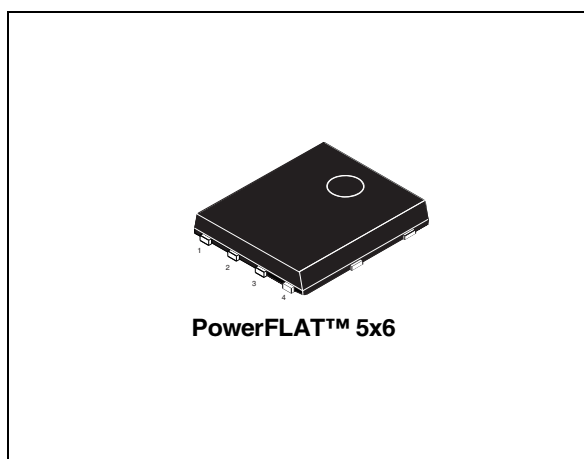
# STL80N3LLH6

N-channel 30 V, 0.0046 Ω, 21 A PowerFLAT™ 5x6  
 STripFET™ VI DeepGATE™ Power MOSFET

## Features

Order code	V <sub>DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub>
STL80N3LLH6	30 V	0.0052 Ω	21 A <sup>(1)</sup>

- The value is rated according R<sub>thj-pcb</sub>
- R<sub>DS(on)</sub> \* Q<sub>g</sub> industry benchmark
  - Extremely low on-resistance R<sub>DS(on)</sub>
  - High avalanche ruggedness
  - Low gate drive power losses
  - Very low switching gate charge



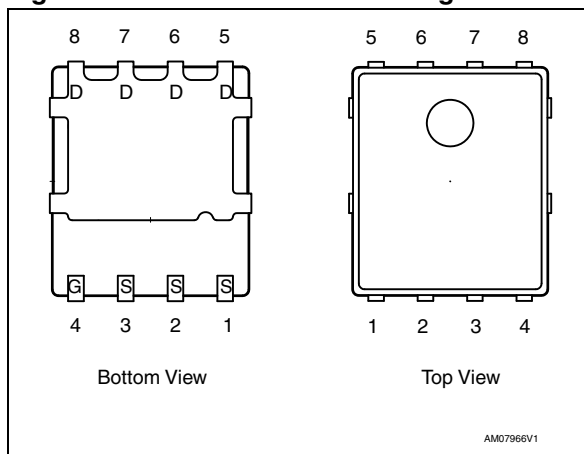
## Applications

- Switching applications

## Description

This device is an N-channel Power MOSFET developed using the 6<sup>th</sup> generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R<sub>DS(on)</sub> in all packages.

**Figure 1. Internal schematic diagram**



**Table 1. Device summary**

Order code	Marking	Package	Packaging
STL80N3LLH6	80N3LLH6	PowerFLAT™ 5x6	Tape and reel

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## Contents

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Electrical ratings

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	30	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	80	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 70\text{ }^\circ\text{C}$	60	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	51	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	21	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb}=70\text{ }^\circ\text{C}$	15.7	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb}=100\text{ }^\circ\text{C}$	13.1	A
$I_{DM}^{(3)}$	Drain current (pulsed)	84	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	60	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4	W
	Derating factor	0.03	W/ $^\circ\text{C}$
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. The value is rated according to  $R_{thj-c}$ .
2. The value is rated according to  $R_{thj-pcb}$ .
3. Pulse width limited by safe operating area.

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (drain, steady state)	2.08	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-ambient	31.3	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu, t < 10 sec.

Electrical characteristics

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## 2 Electrical characteristics

(T<sub>CASE</sub> = 25 °C unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	30			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = 30 V, V <sub>DS</sub> = 30 V at T <sub>C</sub> = 125 °C			1 10	μA μA
I <sub>GSS</sub>	Gate body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±20 V			±100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1	1.7	2.5	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10.5 A V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10.5 A		0.0046 0.0067	0.0052 0.0076	Ω Ω

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input capacitance Output capacitance Reverse transfer capacitance	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0	1350 230 140	1690 290 176	2030 350 210	pF pF pF
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 21 A V <sub>GS</sub> = 4.5 V (see Figure 14)		17 8 6		nC nC nC
R <sub>G</sub>	Gate input resistance	f = 1 MHz Gate DC Bias = 0 Test signal level = 20 mV open drain	1.25	1.7	2	Ω

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Electrical characteristics

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15\text{ V}$ , $I_D=10.5\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ <i>(see Figure 13)</i>		9.5		ns	
$t_r$	Rise time		-	30	-	ns	
$t_{d(off)}$	Turn-off delay time				37		ns
$t_f$	Fall time				12		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current		-		21	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		84	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 21\text{ A}$ , $V_{GS}=0$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 10.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}=25\text{ V}$		24		ns
$Q_{rr}$	Reverse recovery charge		-	16.8		nC
$I_{RRM}$	Reverse recovery current				1.4	

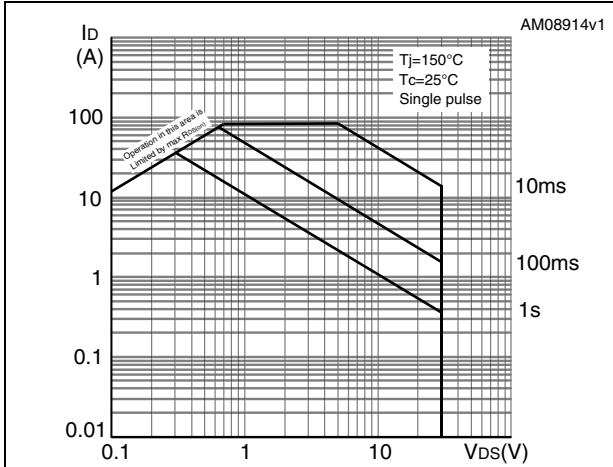
1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

**Electrical characteristics**

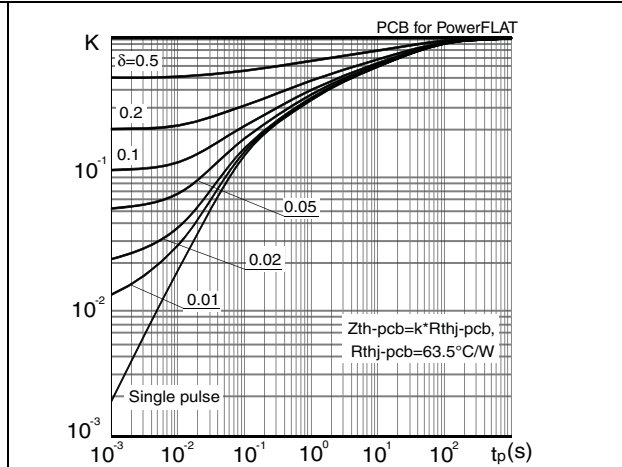
**STL80N3LLH6**

**2.1 Electrical characteristics (curves)**

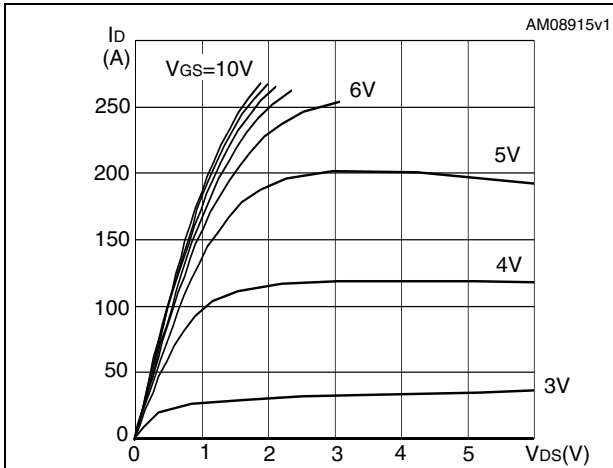
**Figure 2. Safe operating area**



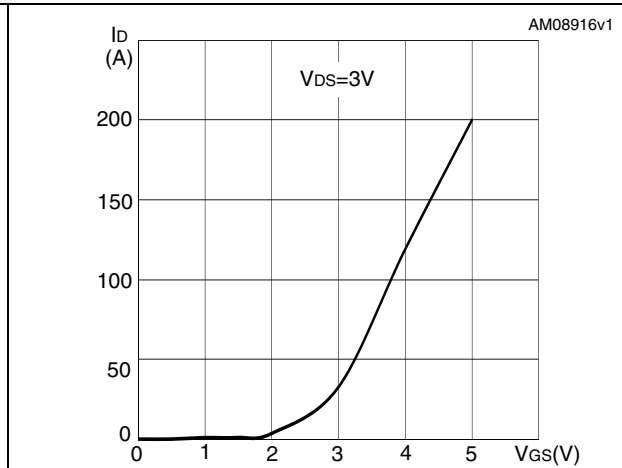
**Figure 3. Thermal impedance**



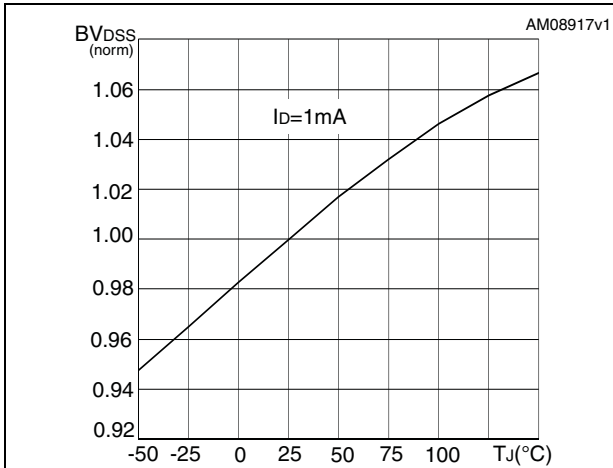
**Figure 4. Output characteristics**



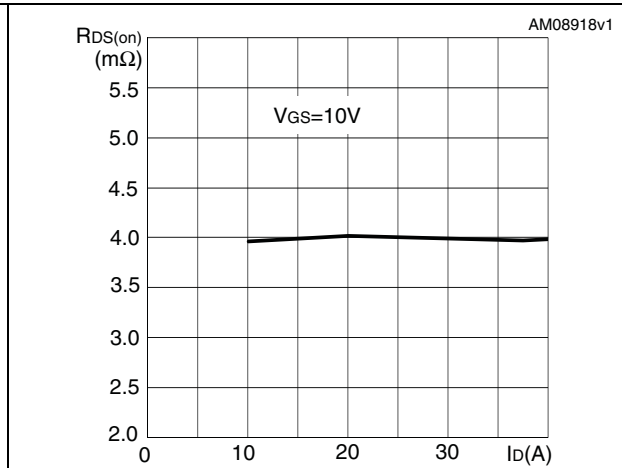
**Figure 5. Transfer characteristics**



**Figure 6. Normalized  $B_{VDSS}$  vs temperature**



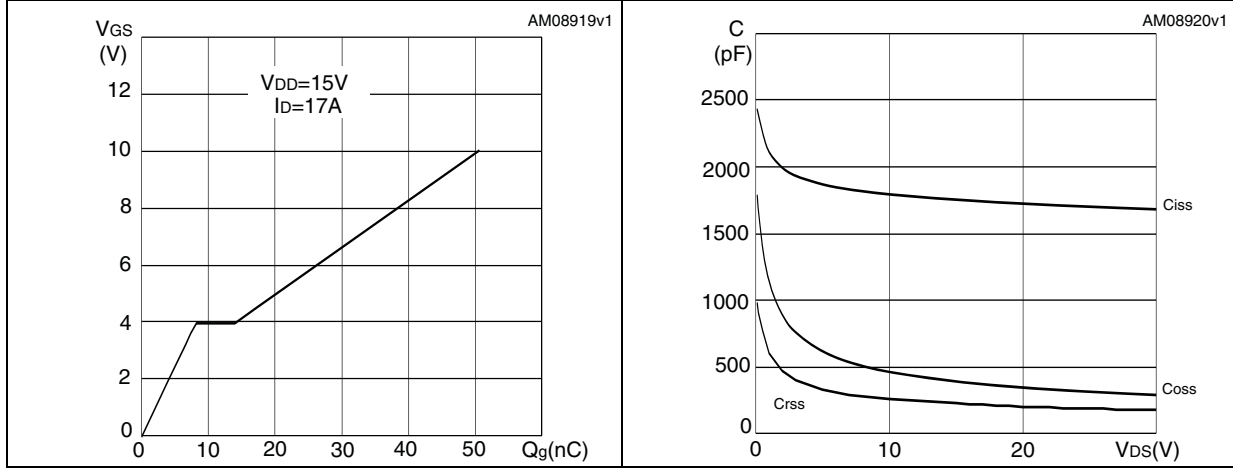
**Figure 7. Static drain-source on resistance**



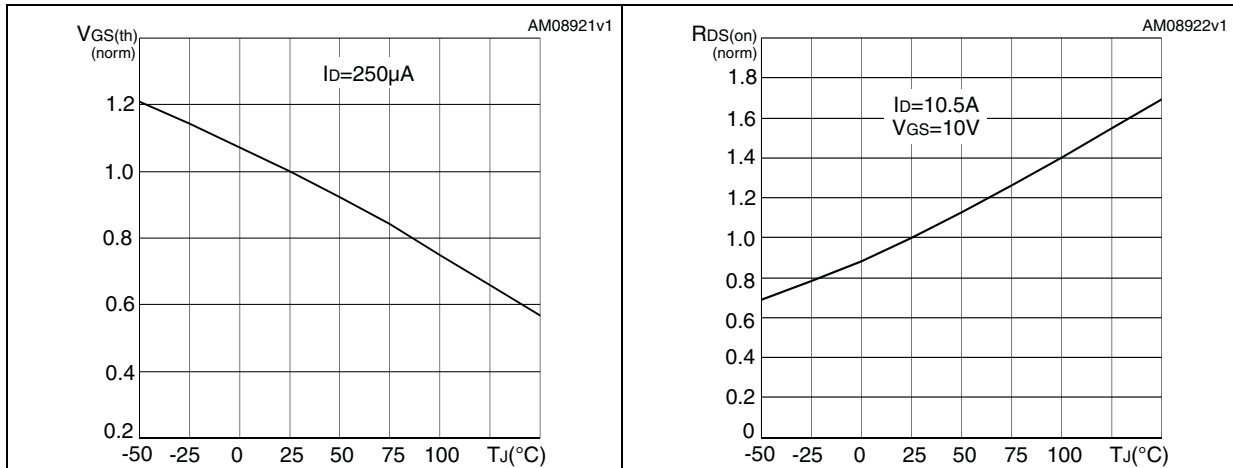
**STL80N3LLH6**

**Electrical characteristics**

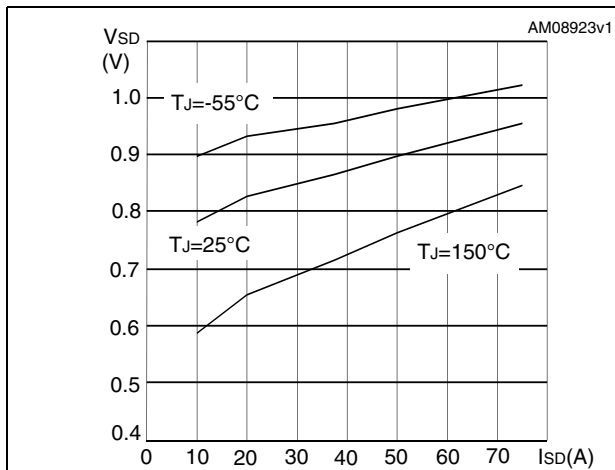
**Figure 8. Gate charge vs gate-source voltage** **Figure 9. Capacitance variations**



**Figure 10. Normalized gate threshold voltage vs temperature** **Figure 11. Normalized on resistance vs temperature**



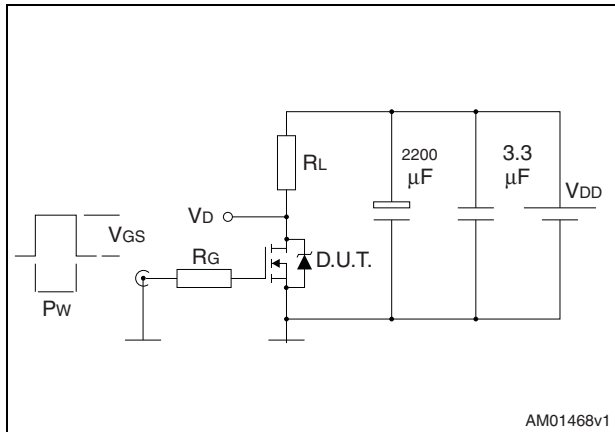
**Figure 12. Source-drain diode forward characteristics**





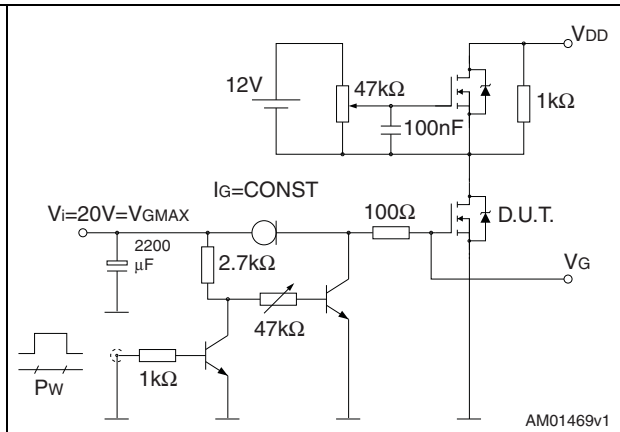
### 3 Test circuits

Figure 13. Switching times test circuit for resistive load



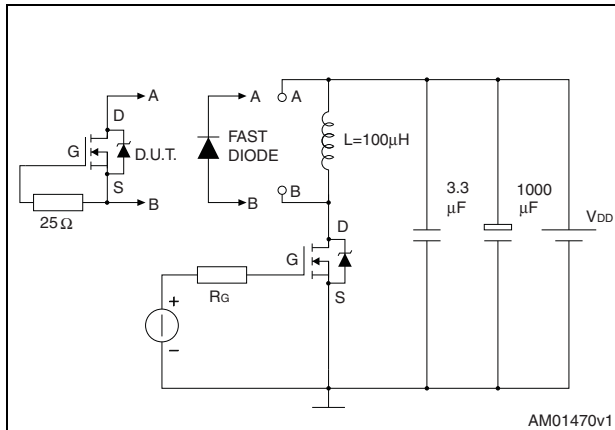
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Figure 14. Gate charge test circuit



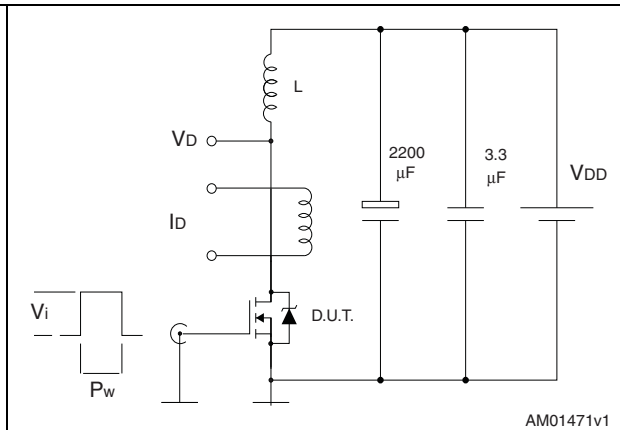
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Figure 15. Test circuit for inductive load switching and diode recovery times



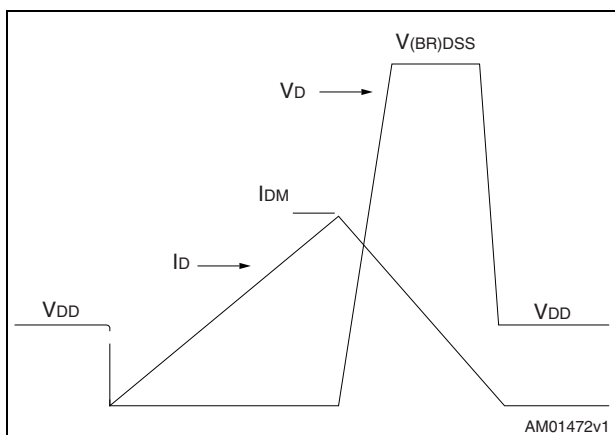
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Figure 16. Unclamped inductive load test circuit



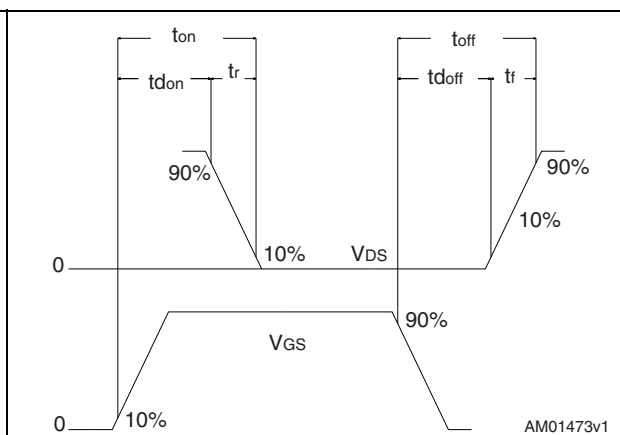
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Figure 17. Unclamped inductive waveform



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Figure 18. Switching time waveform



AM01473v1

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

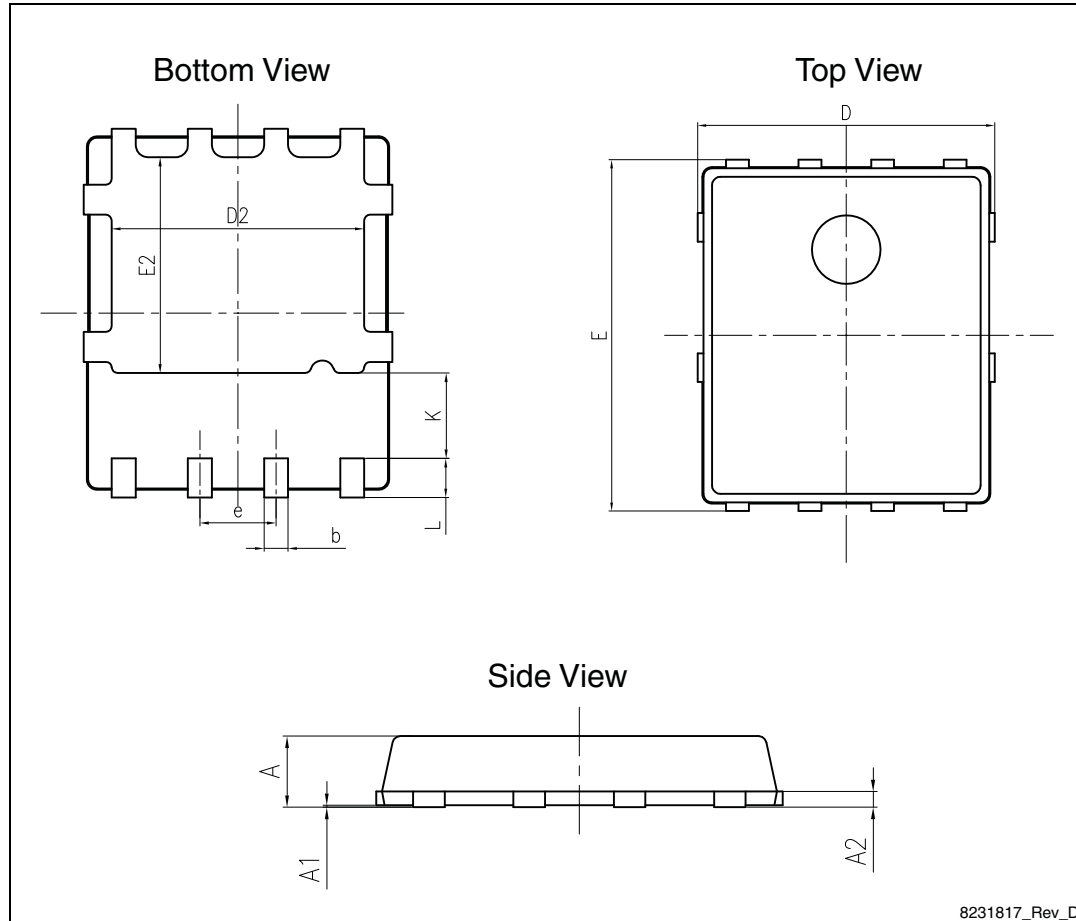
**Package mechanical data**

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**Table 8. PowerFLAT 5x6 type S-R mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
L	0.50		0.80
K	1.275		1.575

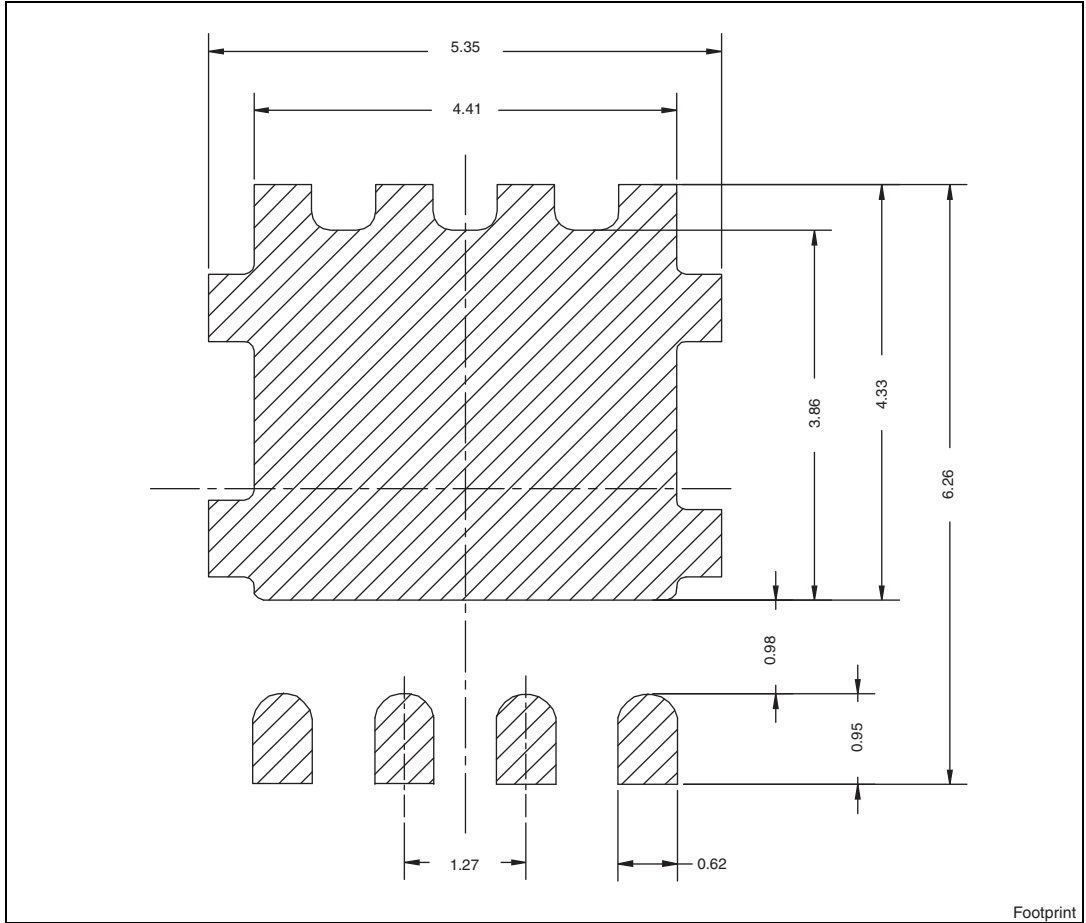
**Figure 19. PowerFLAT 5x6 type S-R drawing**



**STL80N3LLH6**

**Package mechanical data**

**Figure 20. PowerFLAT™ 5x6 recommended footprint (dimensions in mm)**



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
12-Nov-2009	1	First release.
30-Mar-2010	2	$R_{DS(on)}$ values changed in <a href="#">Table 4: On/off states</a>
26-Sep-2011	3	<ul style="list-style-type: none"> <li>– Document status promoted from preliminary data to datasheet;</li> <li>– Inserted <math>I_D</math> value @ 70 °C, in <a href="#">Table 2: Absolute maximum ratings</a>.</li> </ul>
02-Dec-2011	4	<a href="#">Section 4: Package mechanical data</a> has been updated. Minor text changes.

## STL80N3LLH6

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