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Vishay/Siliconix
DG2034DN-T1-E4

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Single 4:1 Low r_{ON} Multiplexers

DESCRIPTION

The DG2034 is a low voltage, low r_{ON}, high bandwidth single 4 to 1 analog multiplexer designed for high performance switching of analog and video signals. Combining low power; fast switching; low on-resistance, flatness and matching; and small physical size, the DG2034 is ideal for portable and battery applications.

Built on Vishay Siliconix's low voltage CMOS process, the DG2034 has an epitaxial layer which prevents latchup. Break-before-make is guaranteed.

FEATURES

- Low voltage operation (1.8 V to 5.5 V)
- Low on-resistance - $r_{DS(on)}$: 4 Ω
- Off-isolation and crosstalk: - 55 dB at 10 MHz
- Fast switch - 25 ns t_{ON}
- Low charge injection - Q_{INJ}: 4.7 pC
- Low power consumption - 4 µW

Pb-free
RoHS COMPLIANT

BENEFITS

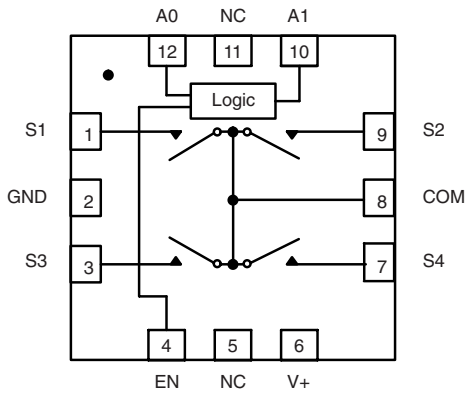
- High accuracy
- High bandwidth
- TTL and low voltage logic compatibility
- Low power consumption
- Reduced PCB space

APPLICATIONS

- Mixed signal routing
- Portable and battery operated systems
- Low voltage data acquisition
- Modems
- PCMCIA cards

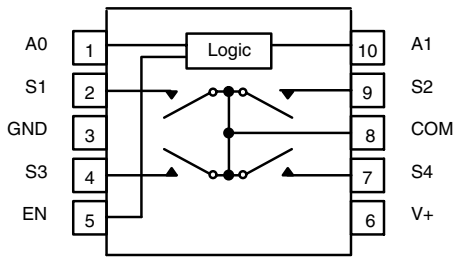
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

12-Pin QFN (3 x 3 mm)



Top View

MSOP-10



Top View

TRUTH TABLE			
A1	A0	EN	ON Switch
X	X	0	None
0	0	1	S1
0	1	1	S2
1	0	1	S3
1	1	1	S4

ORDERING INFORMATION		
Temp Range	Package	Part Number
- 40 °C to 85 °C	MSOP-10	DG2034DQ-T1-E3
	12-pin QFN (3 x 3 mm)	DG2034DN-T1-E4

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
Referenced V+ to GND		- 0.3 to + 6	V
A_X, E_N, S_X, COM[a]		- 0.3 to (V+ + 0.3)	
Continuous Current (Any Terminal)		± 50	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 100	
Power Dissipation (Packages)[b]	QFN-12 (3 x 3 mm)[c]	1295	mW
	MSOP-10[d]	320	
Storage Temperature (D Suffix)		- 65 to 150	°C

Notes:
a. Signals on S_X, D_X, EN or A_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 16.2 mV/°C above 70 °C.
d. Derate 4.0 mV/°C above 70 °C.

SPECIFICATIONS (V+ = 3 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, V_{AL} = 0.4 V, V_{AH} = 1.5 V[e]		Temp.[a]	Limits - 40 to 85 °C Min.[c]	Typ.[b]	Max.[c]	Unit
Analog Switch								
Analog Signal Range[d]	V_{ANALOG}			Full	0		V+	V
On-Resistance	r_{ON}	V+ = 2.7 V, V_{COM} = 0.5 V/1.5 V/2.0 V, I_S = 10 mA		Room Full		4	7 9	Ω
r_{ON} Match	Δr_{ON}			Room		0.1	0.3	
r_{ON} Flatness[d,f]	r_{ON} Flatness			Room		0.3	1.5	
Off Leakage Current[g]	$I_{S(off)}$	V+ = 3.3 V, V_S = 1 V/3 V, V_{COM} = 3 V/1 V, V_{EN} = 0 V		Room Full	- 1 - 10	0.3	1 10	nA
COM Off Leakage Current[g]	$I_{COM(off)}$			Room Full	- 1 - 10	0.3	1 10	
Channel-On Leakage Current[g]	$I_{COM(on)}$	V+ = 3.3 V, V_{COM} = V_S = 1 V/3 V		Room Full	- 1 - 10	0.3	1 10	
Digital Control								
Input Current[d]	I_A or I_{EN}	$V_{A/EN}$ = 0 or V+, See Truth Table		Full	- 1.0		1.0	µA
Input High Voltage[d]	V_{AH} or V_{ENH}			Full	1.5			V
Input Low Voltage[d]	V_{AL} or V_{ENL}			Full			0.4	
Dynamic Characteristics								
Turn-On Time	t_{ON}	V_S = 1.5 V, R_L = 300 Ω		Room Full		25	35 45	ns
Turn-Off Time	t_{OFF}			Room Full		15	25 35	
Break-Before-Make Time[d]	t_D			Room		10.5		
Transition Time	t_{trans}	V_S = 1.5 V/0 V, V_S = 0 V/1.5 V, R_L = 300 Ω		Room Full		30	45 55	
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{gen} = 0 V, R_{gen} = 0 Ω		Room		- 4.7		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF	f = 1 MHz	Room		- 73		dB
			f = 10 MHz	Room		- 54		
Channel-to-Channel Crosstalk[d]	X_{TALK}	R_L = 50 Ω, C_L = 5 pF	f = 1 MHz	Room		- 77		
			f = 10 MHz	Room		- 59		
Off Capacitance[d]	$C_{S(off)}$	V+ = 2.7 V, f = 1 MHz		Room		14		pF
COM Off Capacitance[d]	$C_{COM(off)}$			Room		46		
COM On Capacitance[d]	$C_{COM(on)}$			Room		67		
Power Supply								
Power Supply Range	V+				2.7		3.3	V
Power Supply Current[d]	I+	V+ = 3.3 V, $V_{A/EN}$ = 0 or 3.3 V, See Truth Table		Full			1.0	µA

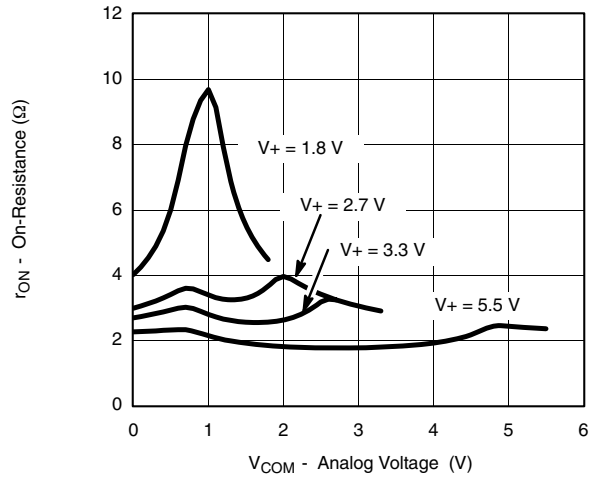
SPECIFICATIONS (V+ = 5 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, V_{AL} = 0.8 V or V_{AH} = 2.4 V[e]	Temp.[a]	Limits - 40 to 85 °C Min.[c]	Typ.[b]	Max.[c]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	0		V+	V
On-Resistance	r_{ON}	V+ = 4.5 V, V_{COM} = 1.5 V/2.5 V/3.5 V, I_S = 10 mA	Room Full		3	5.5 7	Ω
r_{ON} Match	Δr_{ON}		Room		0.16	0.5	
r_{ON} Flatness[d,f]	r_{ON} Flatness		Room		0.6	1.5	
Off Leakage Current	$I_{S(off)}$	V+ = 5.5 V, V_S = 1 V/4.5 V, V_{COM} = 4.5 V/1 V, V_{EN} = 0 V	Room Full	- 1 - 10	0.5	1 10	nA
COM Off Leakage Current	$I_{COM(off)}$		Room Full	- 1 - 10	0.5	1 10	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 5.5 V, V_{COM} = V_S = 1 V/4.5 V	Room Full	- 1 - 10	0.5	1 10	
Digital Control							
Input Current[d]	I_{AH} or I_{ENH}	V_A or V_{EN} = 0 or V+, See Truth Table	Full	- 1.0		1.0	µA
Input High Voltage[d]	V_{AH} or V_{ENH}		Full	2.4			V
Input Low Voltage[d]	V_{AL} or V_{ENL}		Full			0.8	
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_S = 3.0 V, R_L = 300 Ω	Room Full		18	30 40	ns
Turn-Off Time	t_{OFF}		Room Full		12	20 30	
Break-Before-Make Time[d]	t_D		Room		10.5		
Transition Time	t_{trans}	V_S = 3 V/0 V, V_S = 0 V/3 V, R_L = 300 Ω	Room Full		25	40 50	
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 p, f = 1 MHz	Room		- 73		dB
		f = 10 MHz	Room		- 53.5		
Channel-to-Channel Crosstalk[d]	X_{TALK}	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		- 77		
		f = 10 MHz	Room		- 60.2		
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room		- 4.4		pC
Off Capacitance[d]	$C_{S(off)}$	V+ = 5 V, f = 1 MHz	Room		13		pF
COM Off Capacitance[d]	$C_{COM(off)}$		Room		43		
COM On Capacitance[d]	$C_{COM(on)}$		Room		64		
Power Supply							
Power Supply Range	V+			4.5		5.5	V
Power Supply Current	I+	V+ = 5.5 V, $V_{A/EN}$ = 0 or 5.5 V, See Truth Table	Full			1.0	µA

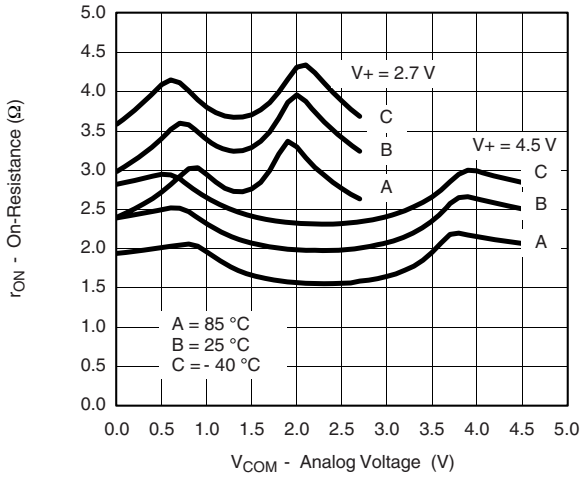
Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, not subjected to production test.
e. V_A, E_N = input voltage to perform proper function.
f. Difference of min and max values.
g. Guaranteed by 5 V testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

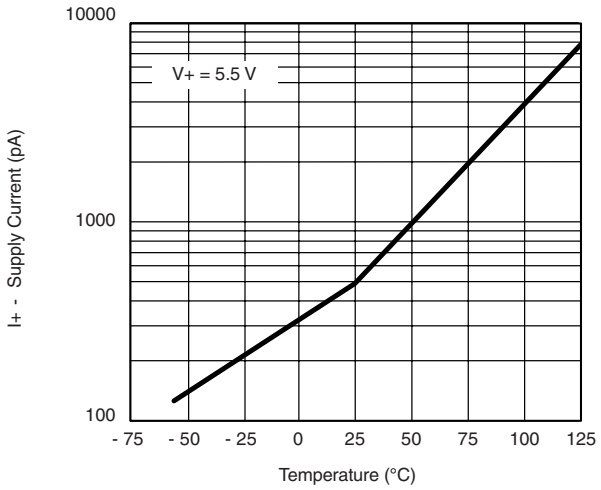
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



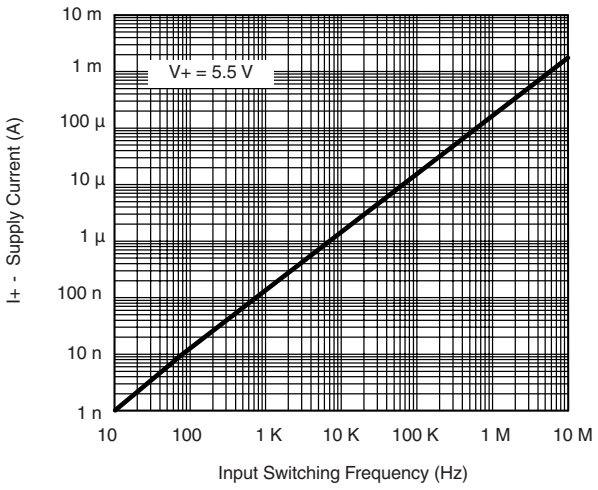
r_{ON} vs. V_{COM} and Supply Voltage



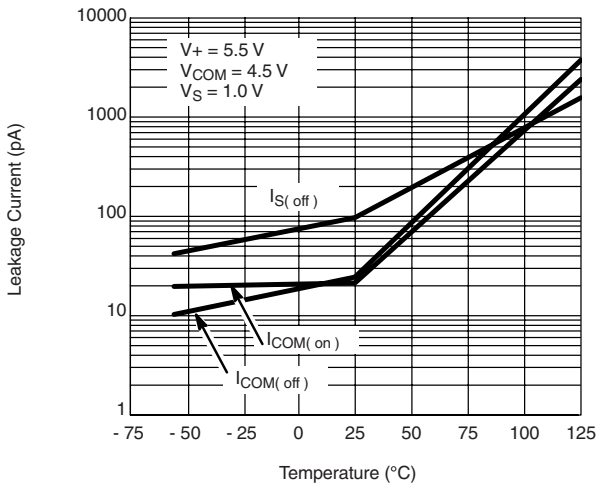
r_{ON} vs. Analog Voltage and Temperature



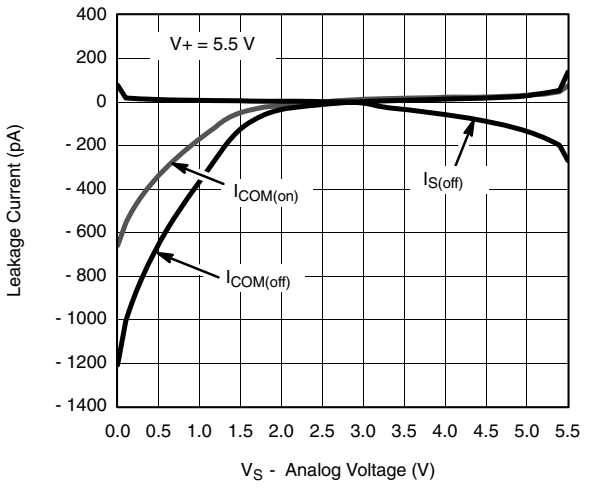
Supply Current vs. Temperature



Supply Current vs. Input Switching Frequency

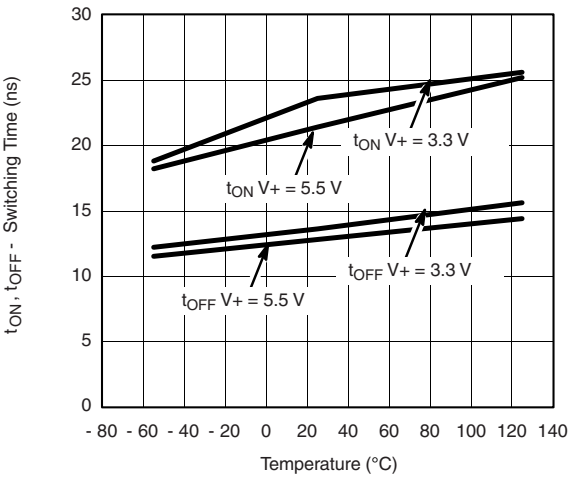


Leakage Current vs. Temperature

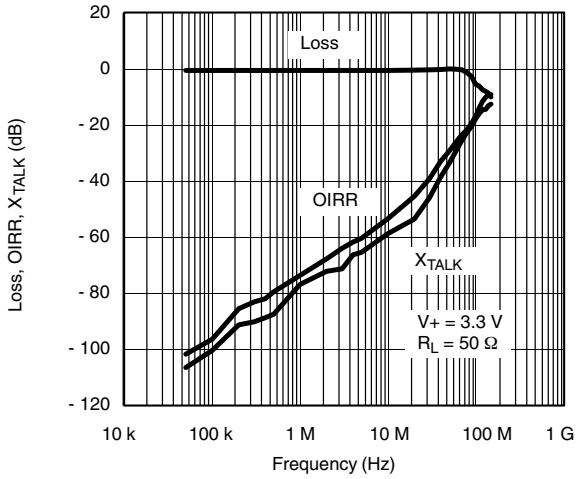


Leakage vs. Analog Voltage

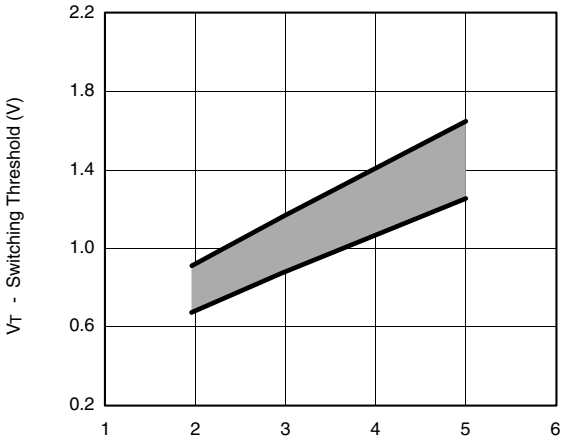
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



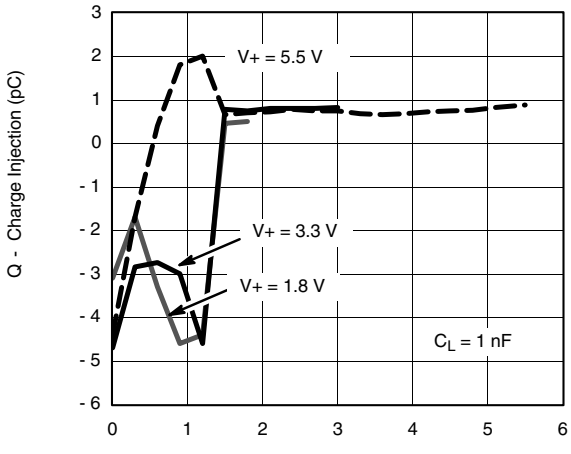
Switching Time vs. Temperature



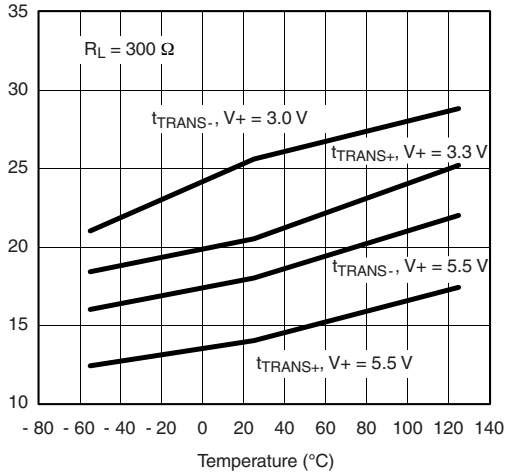
Insertion Loss, Off-Isolation Crosstalk vs. Frequency



Switching Threshold vs. Supply Voltage



Charge Injection vs. Analog Voltage



Transistion Time vs. Temperature

TEST CIRCUITS

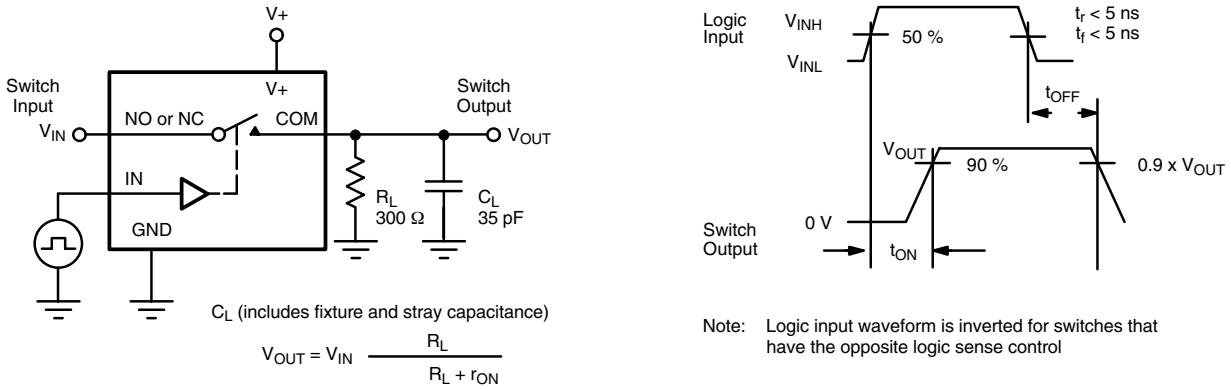


Figure 1. Switching Time

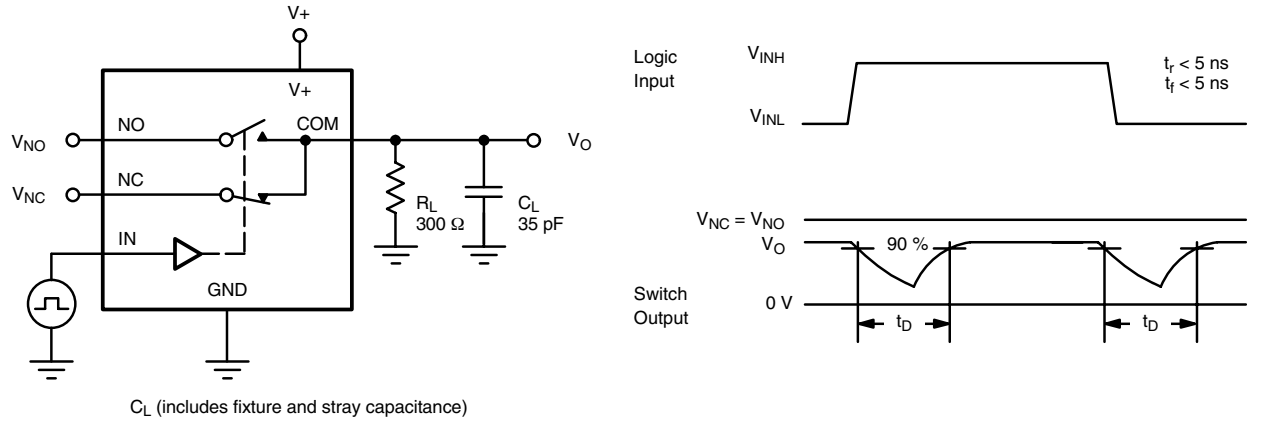


Figure 2. Break-Before-Make

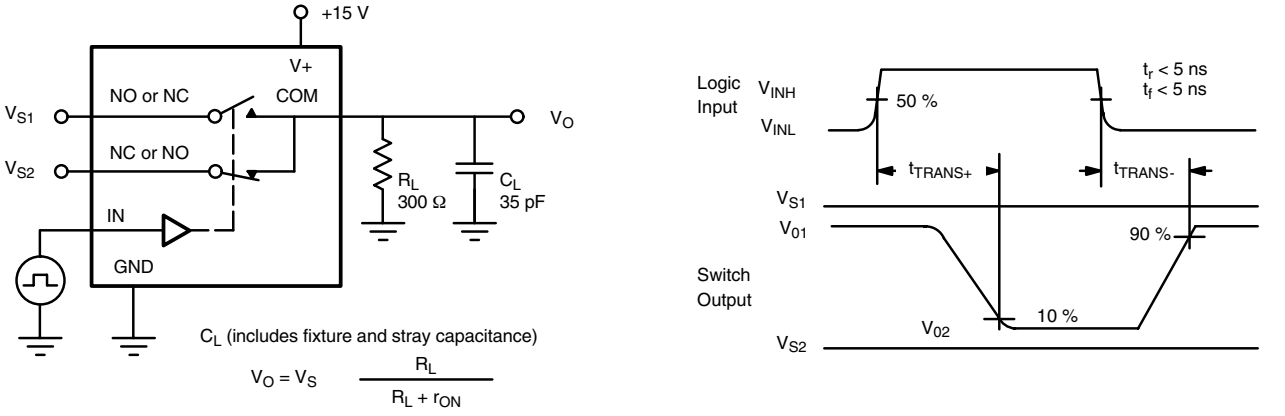


Figure 3. Transition Time

TEST CIRCUITS

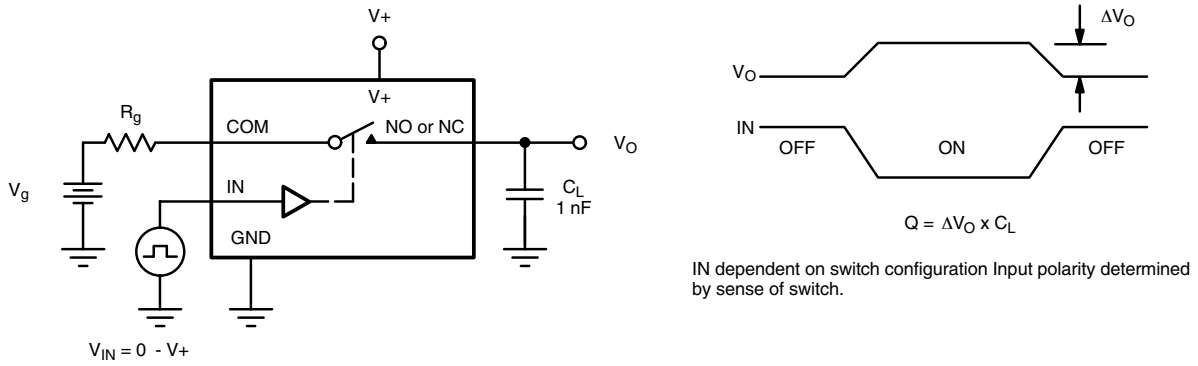


Figure 4. Charge Injection

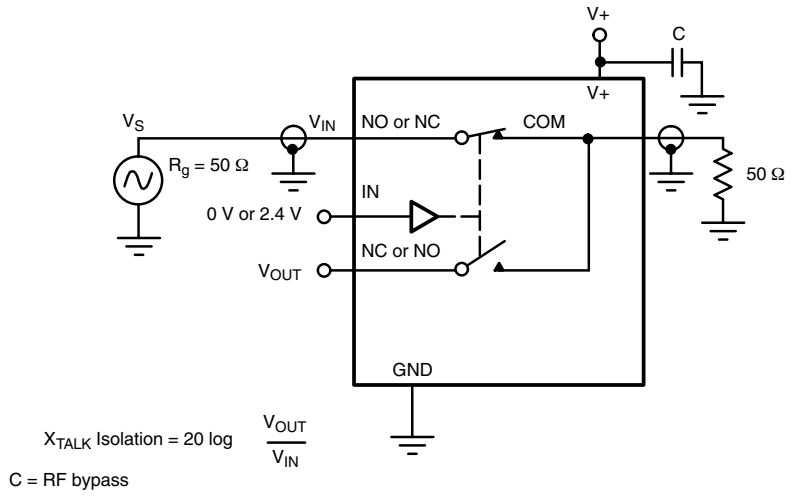


Figure 5. Crosstalk

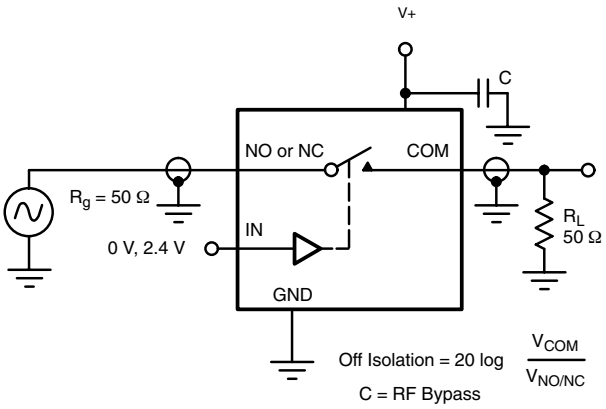


Figure 6. Off Isolation

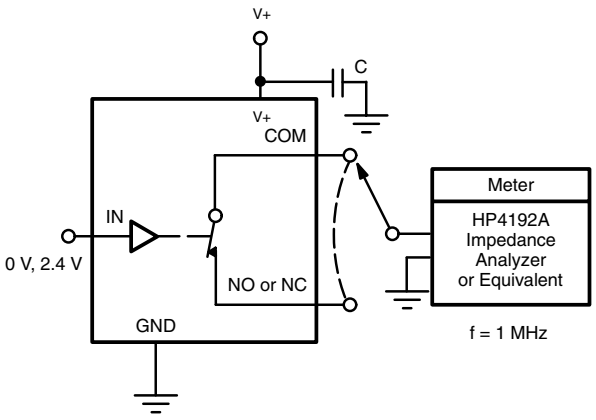
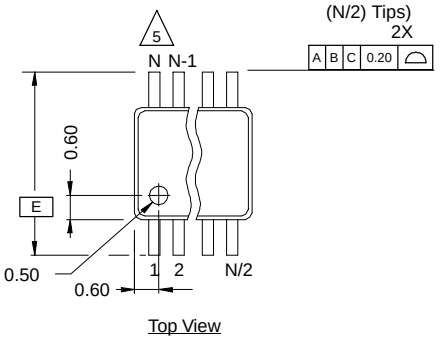


Figure 7. Source/Drain Capacitances

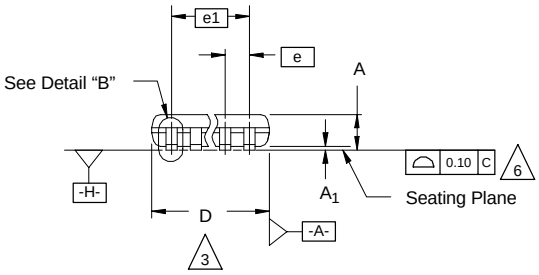
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?72418.

Package Information
Vishay Siliconix

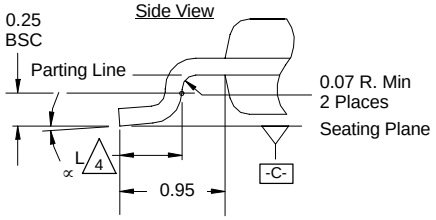
MSOP: 10-LEADS
JEDEC Part Number: MO-187, (Variation AA and BA)



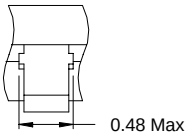
Top View



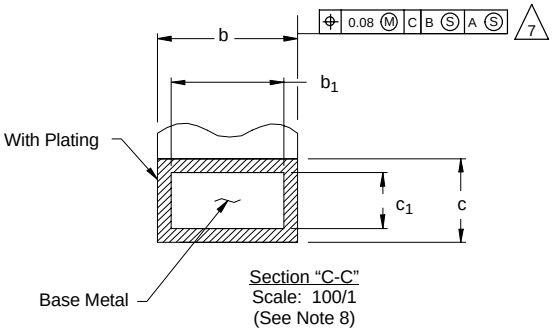
Side View



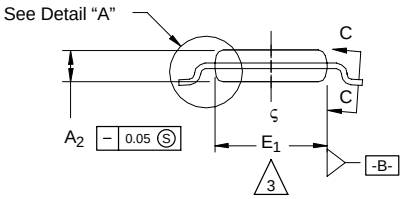
Detail "A"
(Scale: 30/1)



Detail "B"
(Scale: 30/1)
Dambar Protrusion



Section "C-C"
Scale: 100/1
(See Note 8)



End View

NOTES:

1. Die thickness allowable is 0.203 ± 0.0127.
2. Dimensioning and tolerances per ANSI.Y14.5M-1994.
3. Dimensions "D" and "E_1" do not include mold flash or protrusions, and are measured at Datum plane -H- , mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimension is the length of terminal for soldering to a substrate.
5. Terminal positions are shown for reference only.
6. Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
7. The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
8. Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
9. Controlling dimension: millimeters.
10. This part is compliant with JEDEC registration MO-187, variation AA and BA.
11. Datums -A- and -B- to be determined Datum plane -H- .
12. Exposed pad area in bottom side is the same as teh leadframe pad size.

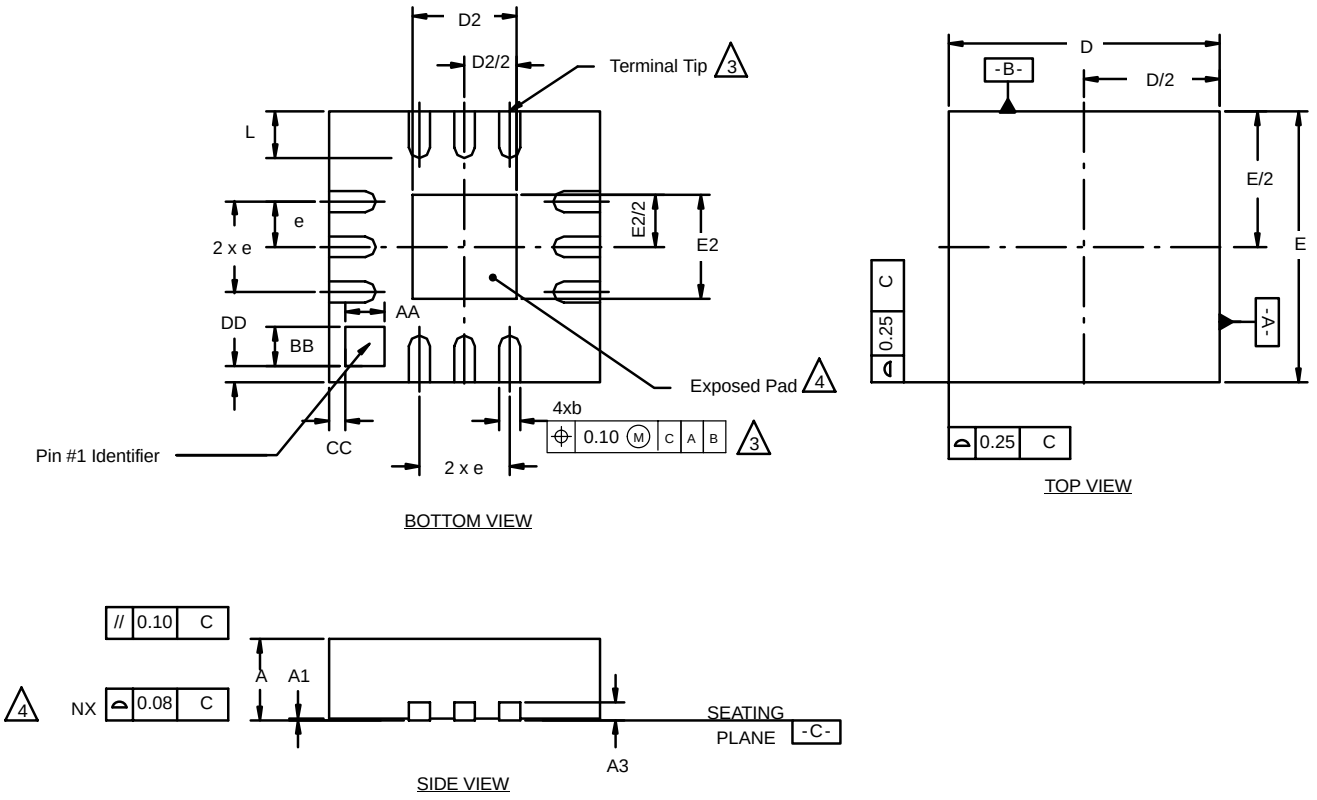
N = 10L

Dim	MILLIMETERS			Note
	Min	Nom	Max	
A	-	-	1.10	
A_1	0.05	0.10	0.15	
A_2	0.75	0.85	0.95	
b	0.17	-	0.27	8
b_1	0.17	0.20	0.23	8
c	0.13	-	0.23	
c_1	0.13	0.15	0.18	
D	3.00 BSC			3
E	4.90 BSC			
E_1	2.90	3.00	3.10	3
e	0.50 BSC			
e_1	2.00 BSC			
L	0.40	0.55	0.70	4
N	10			5
∝	0°	4°	6°	

ECN: T-02080—Rev. C, 15-Jul-02
DWG: 5867

Package Information
Vishay Siliconix

QFN-12 LEAD (3 X 3)



NOTES:

1. All dimensions are in millimeters.
2. N is the total number of terminals.
3. Dimension b applies to metallized terminal and is measured between 0.25 and 0.30 mm from terminal tip.
4. Coplanarity applies to the exposed heat sink slug as well as the terminal.
5. The pin #1 identifier may be either a mold or marked feature, it must be located within the zone iindicated.

Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.90	1.00	0.032	0.035	0.039
b	0.18	0.23	0.30	0.007	0.009	0.012
D		3.00 BSC			0.118 BSC	
D2	1.00	1.15	1.25	0.039	0.045	0.049
E		3.00 BSC			0.118 BSC	
E2	1.00	1.15	1.25	0.039	0.045	0.049
e		0.50 BSC			0.02 BSC	
L	0.45	0.55	0.65	0.018	0.022	0.026
AA		0.435			0.017	
BB		0.435			0.017	
CC		0.18			0.007	
DD		0.18			0.007	

ECN: C-03092—Rev. A, 14-Apr-03
DWG: 5898

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