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Vishay/Siliconix
DG2531DQ-T1-E3

For any questions, you can email us directly:
sales@integrated-circuit.com

0.4-Ω Low-Voltage Dual SPDT Analog Switch

DESCRIPTION

The DG2531/DG2532 is a sub 1-Ω (0.4 Ω at 2.7 V) dual SPDT analog switches designed for low voltage applications.

The DG2531/DG2532 has on-resistance matching (less than 0.05 Ω at 2.7 V) and flatness (less than 0.2 Ω at 2.7 V) that are guaranteed over the entire voltage range. Additionally, low logic thresholds makes the DG2531/DG2532 an ideal interface to low voltage DSP control signals.

The DG2531/DG2532 has fast switching speed (on/off time at 40 and 35 ns) with break-before-make guaranteed. In the On condition, all switching elements conduct equally in both directions. Off-isolation and crosstalk is - 69 dB at 100 kHz.

The DG2531/DG2532 is built on Vishay Siliconix's high-density low voltage CMOS process. An eptiaxial layer is built in to prevent latchup. The DG2531/DG2532 contains the additional benefit of 2000 V ESD protection.

Packaged in space saving MSOP-10, the DG2531/DG2532 is a high performance, low r_{ON} switches for battery powered applications.

FEATURES

- Low Voltage Operation (1.8 V to 5.5 V)
- Low On-Resistance - r_{ON}: 0.4 Ω at 2.7 V
- - 69 dB OIRR at 2.7 V, 100 kHz
- MSOP-10 Package
- ESD Protection > 2000 V

Pb-free
RoHS COMPLIANT

BENEFITS

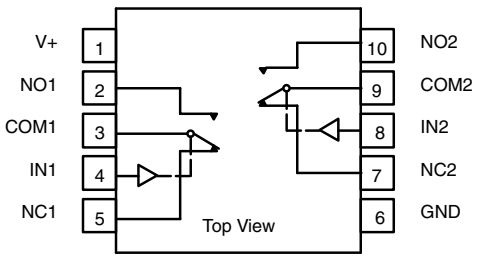
- Reduced Power Consumption
- High Accuracy
- Reduce Board Space
- 1.6 V Logic Compatible
- High Bandwidth

APPLICATIONS

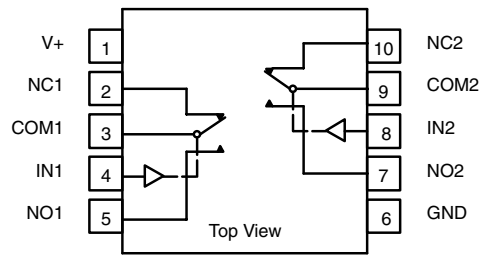
- Cellular Phones
- Speaker Headset Switching
- Audio and Video Signal Routing
- PCMCIA Cards
- Battery Operated Systems
- Relay Replacement

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG2531
MSOP-10



DG2532
MSOP-10



TRUTH TABLE		
Logic	**NC1 and NC2**	**NO1 and NO2**
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
- 40 to 85 °C	MSOP-10	DG2531DQ-T1-E3 DG2532DQ-T1-E3

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
Reference V+ to GND		- 0.3 to + 6	V
IN, COM, NC, NO[a]		- 0.3 to (V+ + 0.3)	
Continuous Current (NO, NC, COM)		± 300	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 500	
Storage Temperature	(D Suffix)	- 65 to 150	°C
PESD per Method 3015.7		> 2	kV
Power Dissipation (Packages)[b]	MSOP-10[c]	320	mW

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 4.0 mW/°C above 70 °C.

SPECIFICATIONS (V+ = 3 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, V_{IN} = 0.5 V or 1.4 V[e]	Temp[a]	Limits - 40 to 85 °C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	r_{ON}	V+ = 2.7 V, V_{COM} = 0.6 V/1.5 V, I_{NO}, I_{NC} = 100 mA	Room Full		0.4	0.6 0.7	Ω
r_{ON} Flatness[d]	r_{ON} Flatness		Room		0.12	0.2	
On-Resistance Match Between Channels[d]	$\Delta r_{DS(on)}$		Room			0.05	
Switch Off Leakage Current	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 3.3 V, V_{NO}, V_{NC} = 0.3 V/3 V, V_{COM} = 3 V/0.3 V	Room Full	- 1 - 10		1 10	nA
	$I_{COM(off)}$		Room Full	- 1 - 10		1 10	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 0.3 V/3 V	Room Full	- 1 - 10		1 10	
Digital Control							
Input High Voltage[d]	V_{INH}		Full	1.4			V
Input Low Voltage	V_{INL}		Full			0.5	
Input Capacitance	C_{in}		Full		7		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	1		1	µA

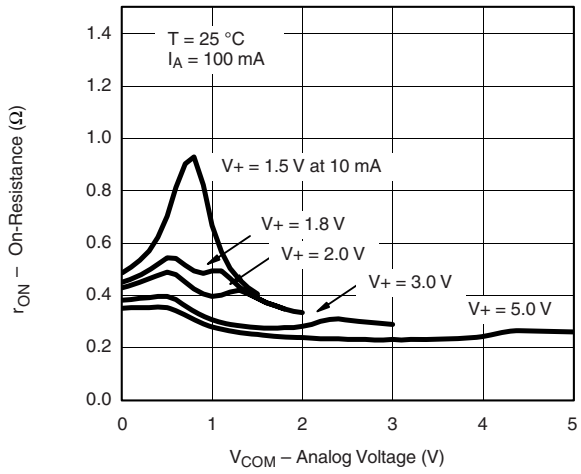
SPECIFICATIONS (V+ = 3 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, V_{IN} = 0.5 V or 1.4 V[e]	Temp[a]	Limits - 40 to 85 °C Min[b]	Typ[c]	Max[b]	Unit
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 2.0 V, R_L = 50 Ω, C_L = 35 pF	Room Full		40	70 77	ns
Turn-Off Time	t_{OFF}		Room Full		35	65 72	
Break-Before-Make Time	t_d		Room	1	4		
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 1.5 V, R_{GEN} = 0 Ω	Room		54		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz	Room		- 69		dB
Crosstalk[d]	X_{TALK}		Room		- 69		
N_O, N_C Off Capacitance[d]	$C_{NO(off)}$ $C_{NC(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		143		pF
Channel-On Capacitance[d]	$C_{NO(on)}$ $C_{NC(on)}$		Room		403		
Power Supply							
Power Supply Range	V+			1.8		5.5	V
Power Supply Current	I+	V_{IN} = 0 or V+	Full			1.0	µA

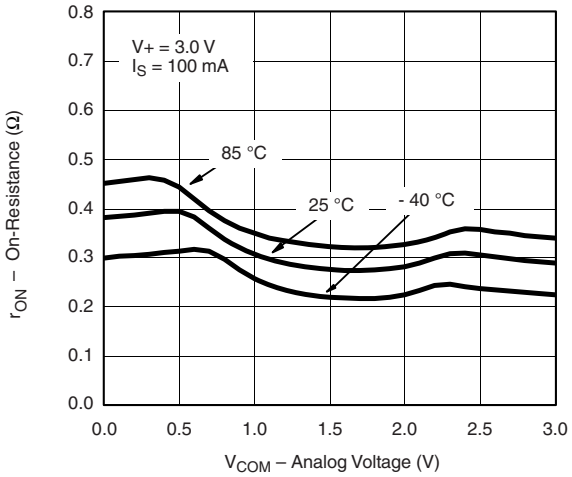
Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

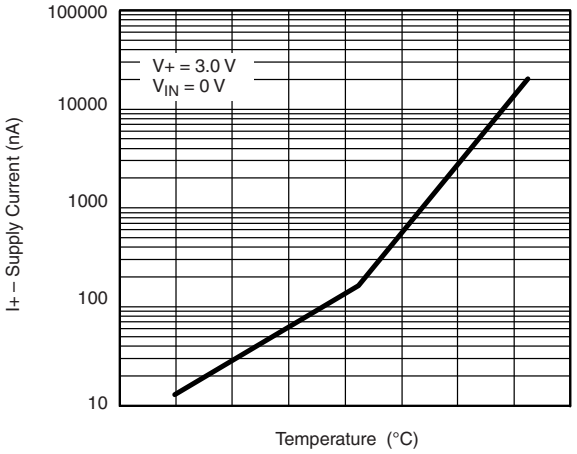
TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



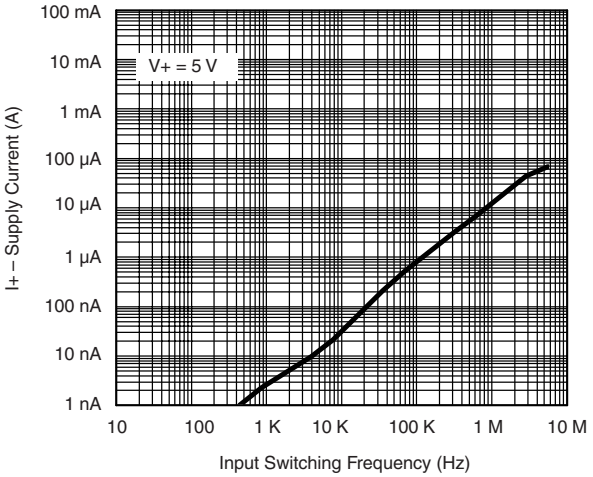
r_{ON} vs. V_{COM} and Supply Voltage



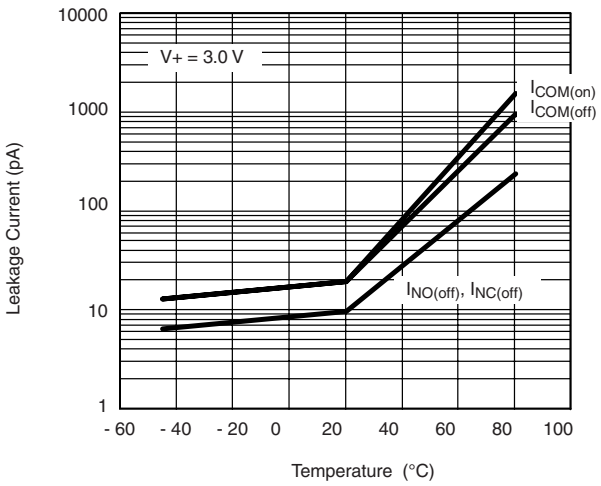
r_{ON} vs. Analog Voltage and Temperature (NC1)



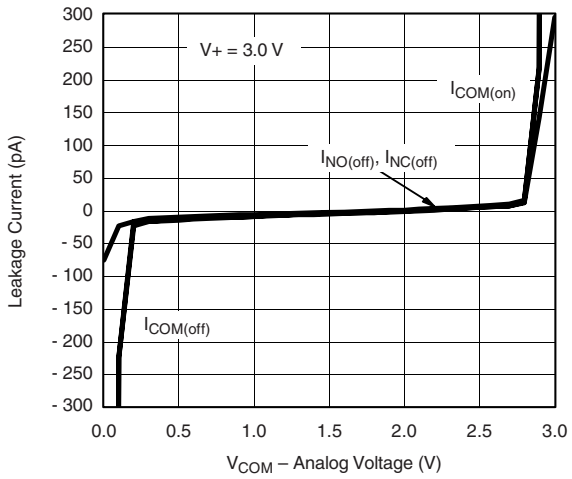
Supply Current vs. Temperature



Supply Current vs. Input Switching Frequency

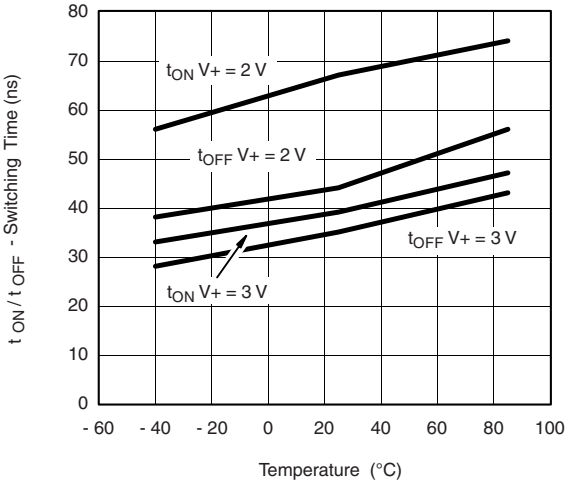


Leakage Current vs. Temperature

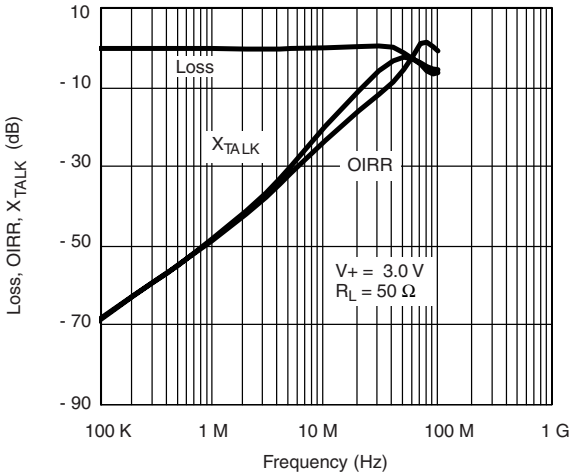


Leakage vs. Analog Voltage

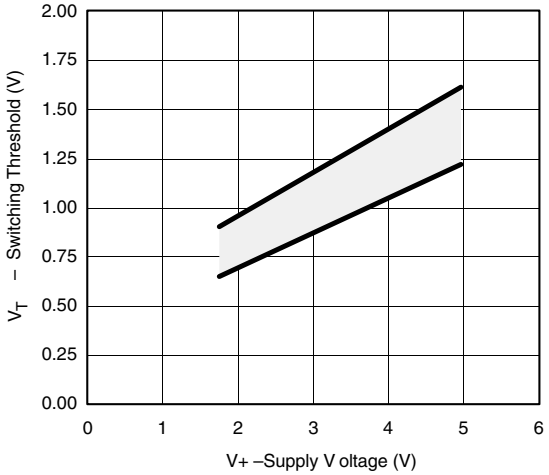
TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



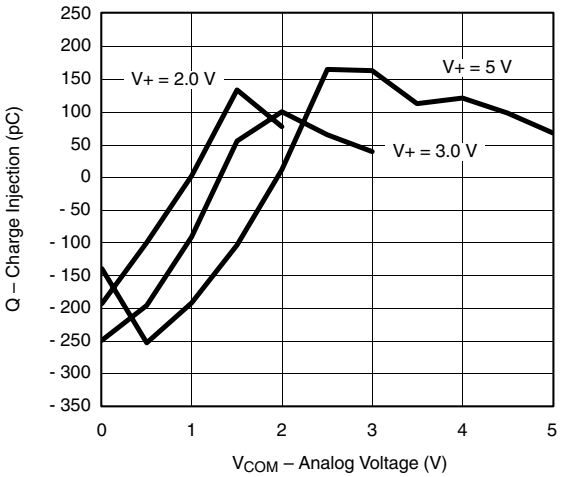
Switching Time vs. Temperature



Insertion Loss, Off-Isolation, Crosstalk vs. Frequency

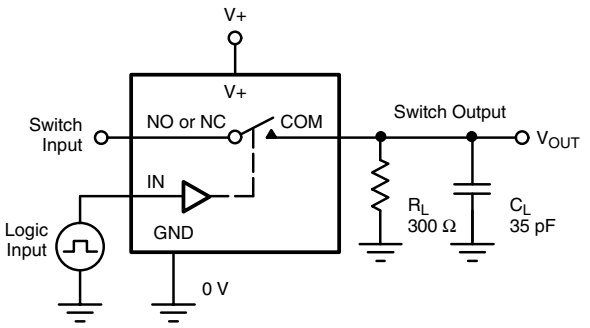


Switching Threshold vs. Supply Voltage



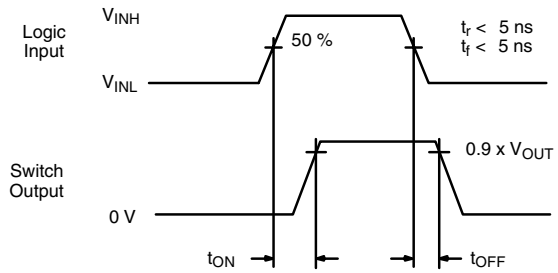
Charge Injection vs. Analog Voltage

TEST CIRCUITS



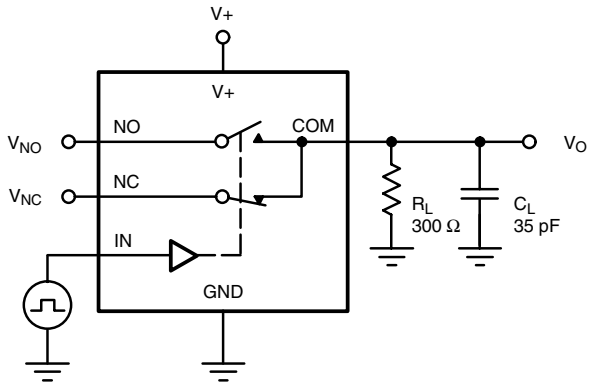
C_L (includes fixture and stray capacitance)

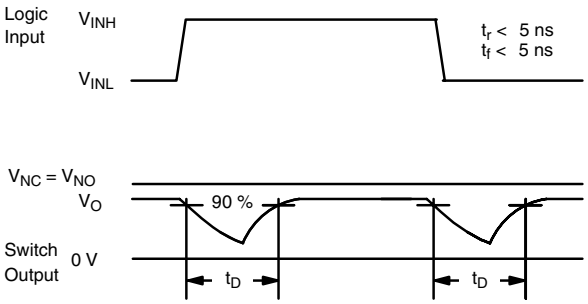
$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

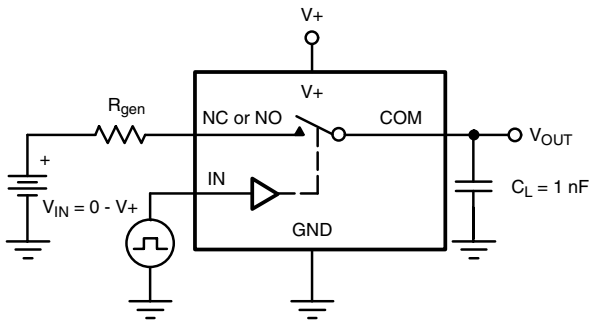
Figure 1. Switching Time

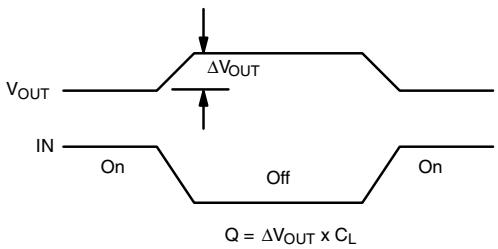




C_L (includes fixture and stray capacitance)

Figure 2. Break-Before-Make Interval





$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

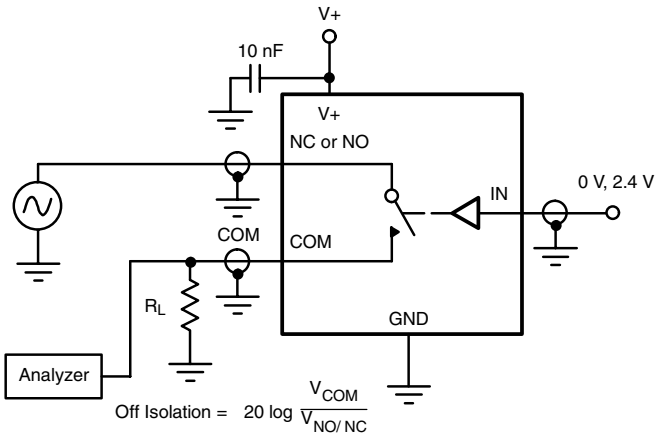


Figure 4. Off-Isolation

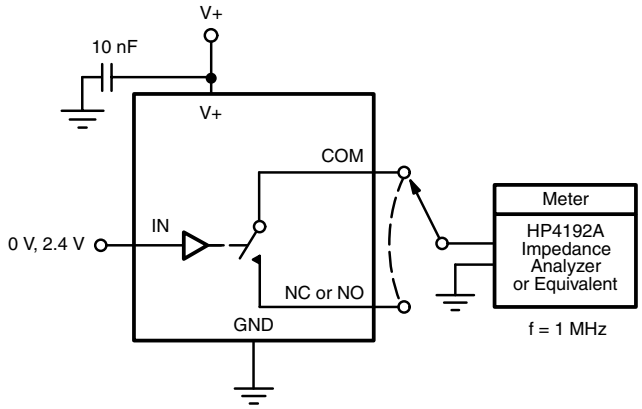


Figure 5. Channel Off/On Capacitance

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