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[Vishay/Siliconix](#)
[SI4158DY-T1-GE3](#)

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sales@integrated-circuit.com



N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
20	0.0025 at V _{GS} = 10 V	36.5	40 nC
	0.003 at V _{GS} = 4.5 V	33.3	

FEATURES

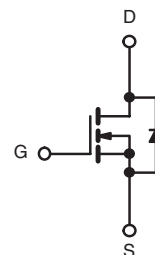
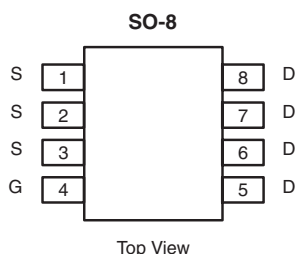
- Halogen-free
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested



RoHS
COMPLIANT

APPLICATIONS

- Low-Side MOSFET for Synchronous Buck
- OR-ing



Ordering Information: Si4158DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	± 16	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	A
		T _C = 70 °C	
		T _A = 25 °C	
		T _A = 70 °C	
Pulsed Drain Current	I _{DM}	70	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	
		T _A = 25 °C	
Single Pulse Avalanche Current	I _{AS}	40	
Avalanche Energy	E _{AS}	80	
Maximum Power Dissipation	P _D	T _C = 25 °C	W
		T _C = 70 °C	
		T _A = 25 °C	
		T _A = 70 °C	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 s	R _{thJA}	33	42	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	16	21	

Notes:

- Based on T_C = 25 °C.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under Steady State conditions is 85 °C/W.

New Product

Si4158DY

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SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		24		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-5.4		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0		2.1	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 16\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		0.002	0.0025	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		0.0024	0.003	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 20\text{ A}$		120		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		5710		μF
Output Capacitance	C_{oss}			1000		
Reverse Transfer Capacitance	C_{rss}			505		
Total Gate Charge	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		88	132	nC
				40	60	
Gate-Source Charge	Q_{gs}	$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		11.5		
Gate-Drain Charge	Q_{gd}			9.0		
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.2	0.8	1.6	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 1\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		37	70	ns
Rise Time	t_r			20	35	
Turn-Off Delay Time	$t_{d(off)}$			68	120	
Fall Time	t_f			32	60	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 1\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		13	25	
Rise Time	t_r			11	22	
Turn-Off Delay Time	$t_{d(off)}$			49	90	
Fall Time	t_f			8	16	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			5.4	A
Pulse Diode Forward Current ^a	I_{SM}				70	
Body Diode Voltage	V_{SD}	$I_S = 2.7\text{ A}$		0.71	1.1	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		29	44	ns
Body Diode Reverse Recovery Charge	Q_{rr}			21	32	nC
Reverse Recovery Fall Time	t_a			16		ns
Reverse Recovery Rise Time	t_b			13		

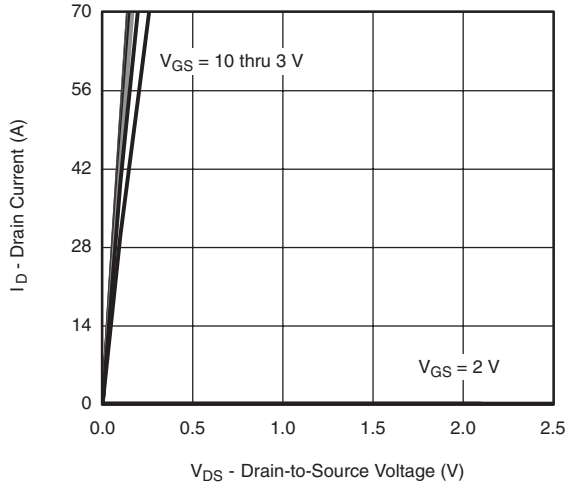
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
- b. Guaranteed by design, not subject to production testing.

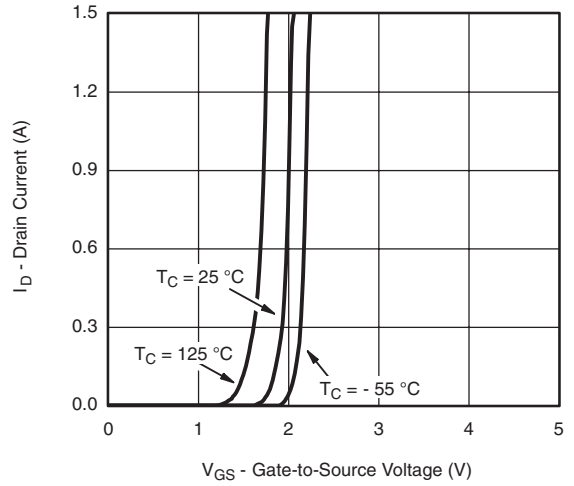
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



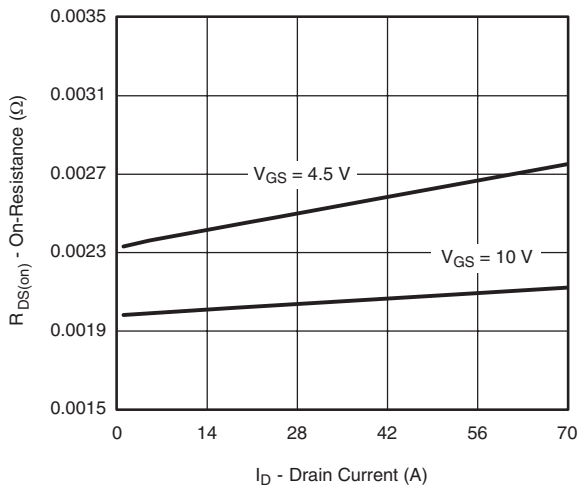
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



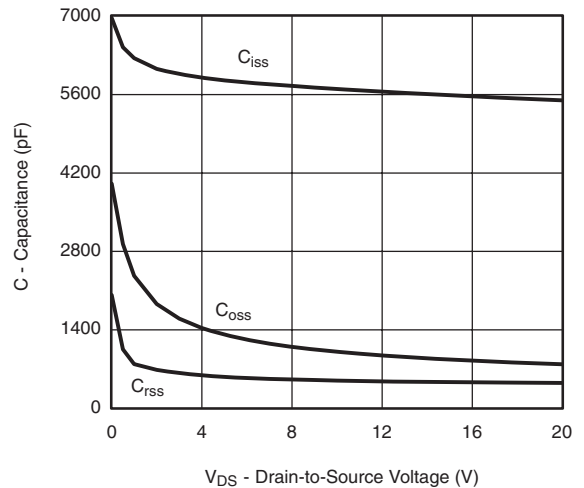
Output Characteristics



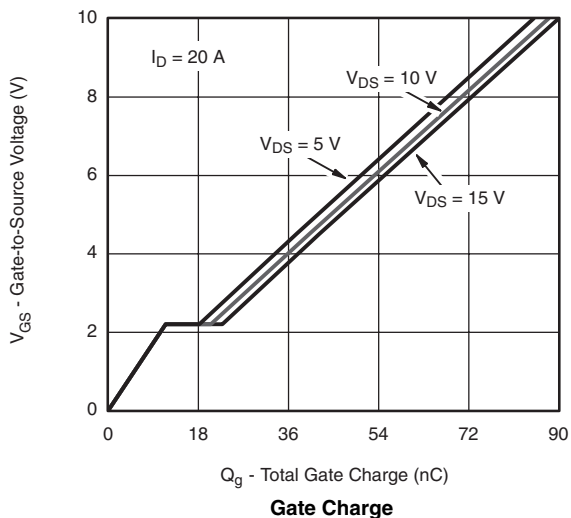
Transfer Characteristics



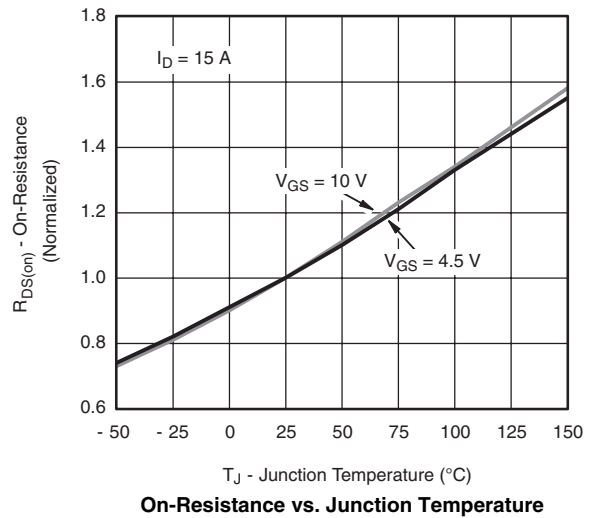
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



Gate Charge



On-Resistance vs. Junction Temperature

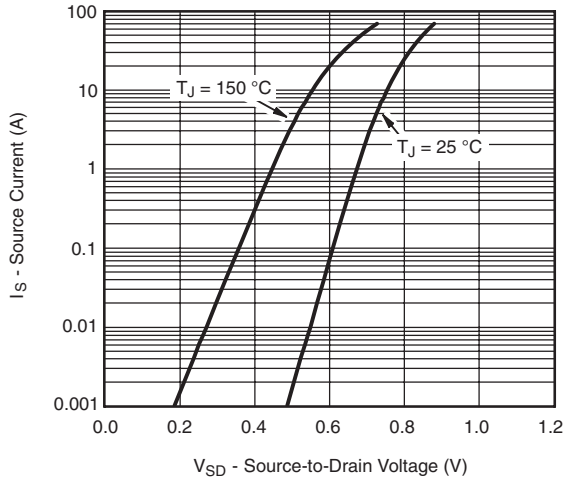
New Product

Si4158DY

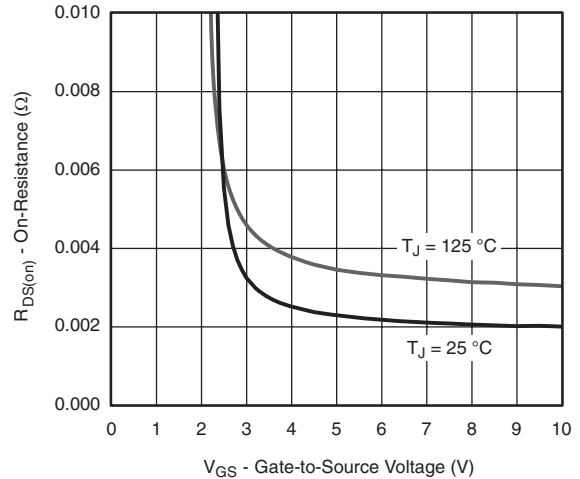
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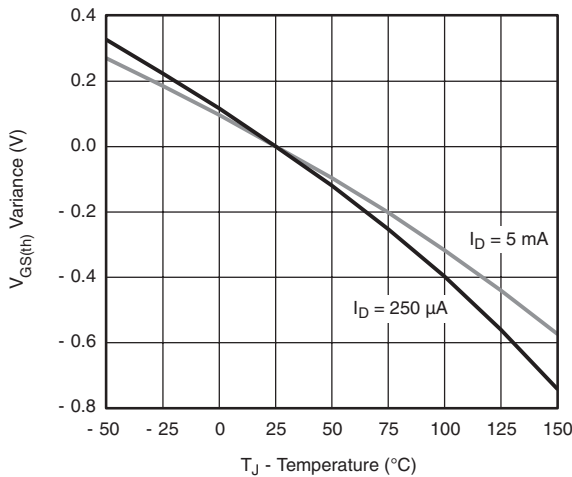
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



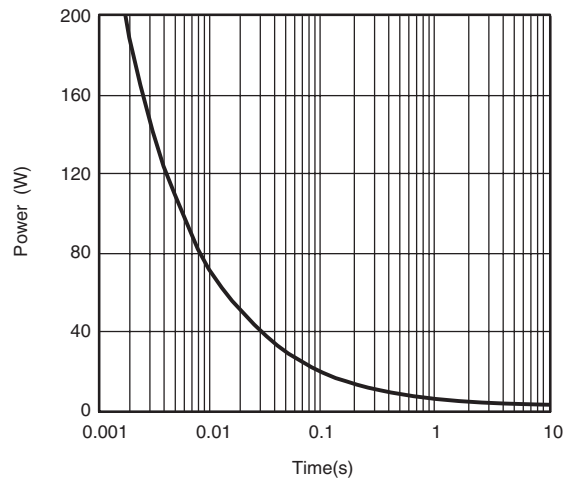
Source-Drain Diode Forward Voltage



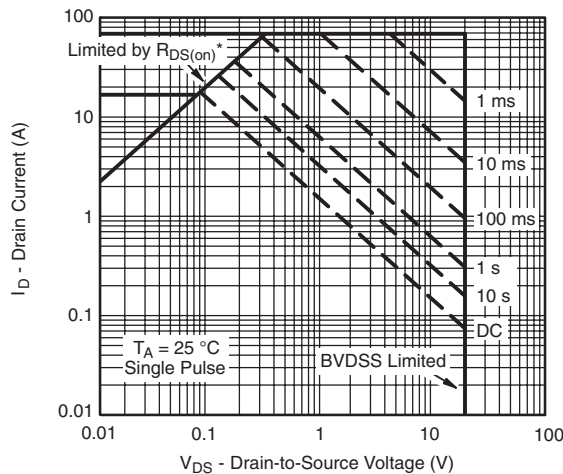
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

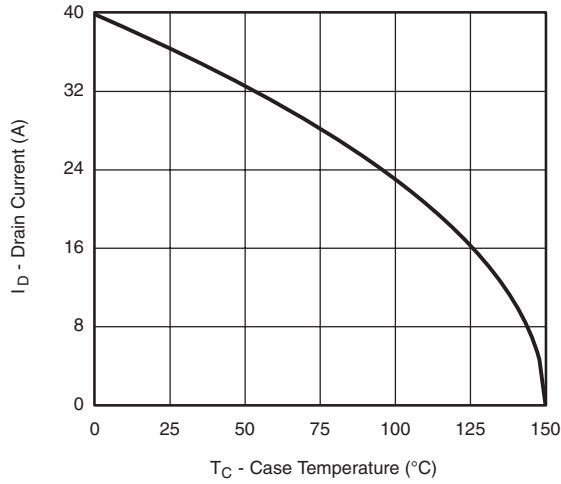
Safe Operating Area, Junction-to-Ambient

New Product



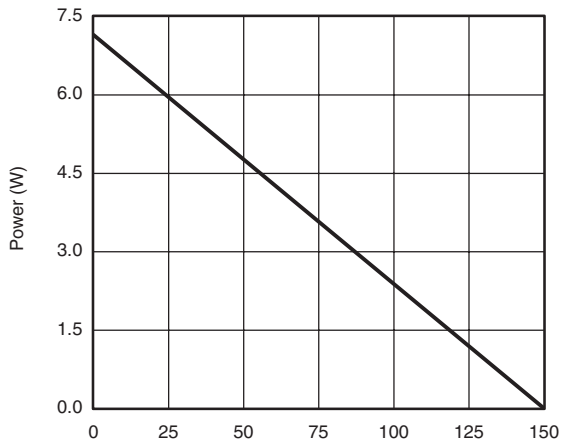
Si4158DY
Vishay Siliconix

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



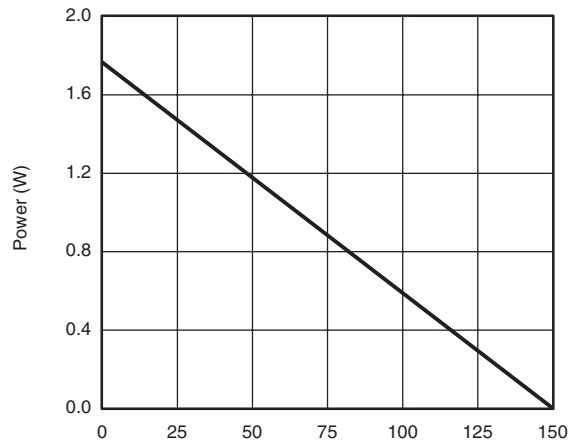
T_C - Case Temperature (°C)

Current Derating*



T_C - Case Temperature (°C)

Power, Junction-to-Foot



T_A - Ambient Temperature (°C)

Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

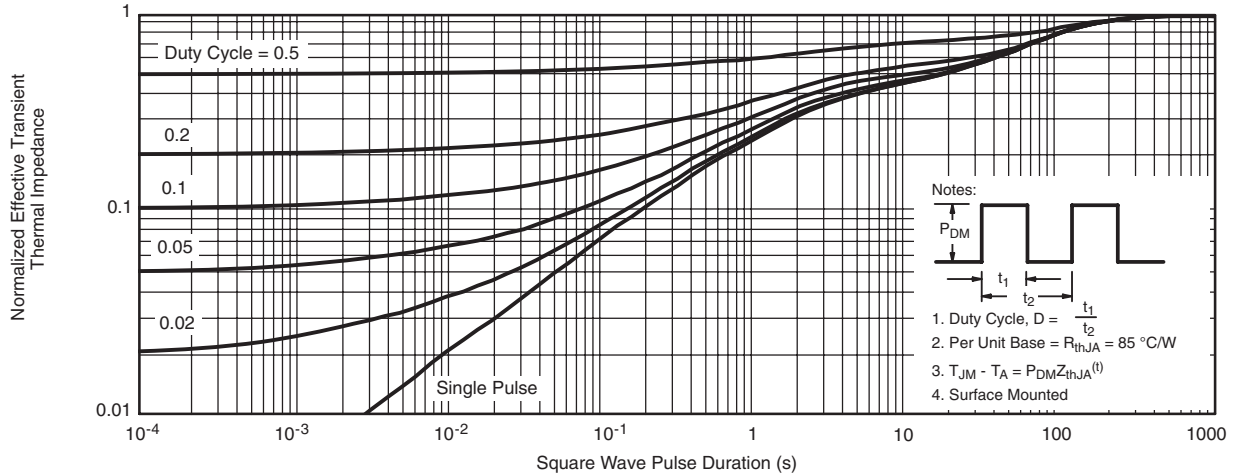
New Product

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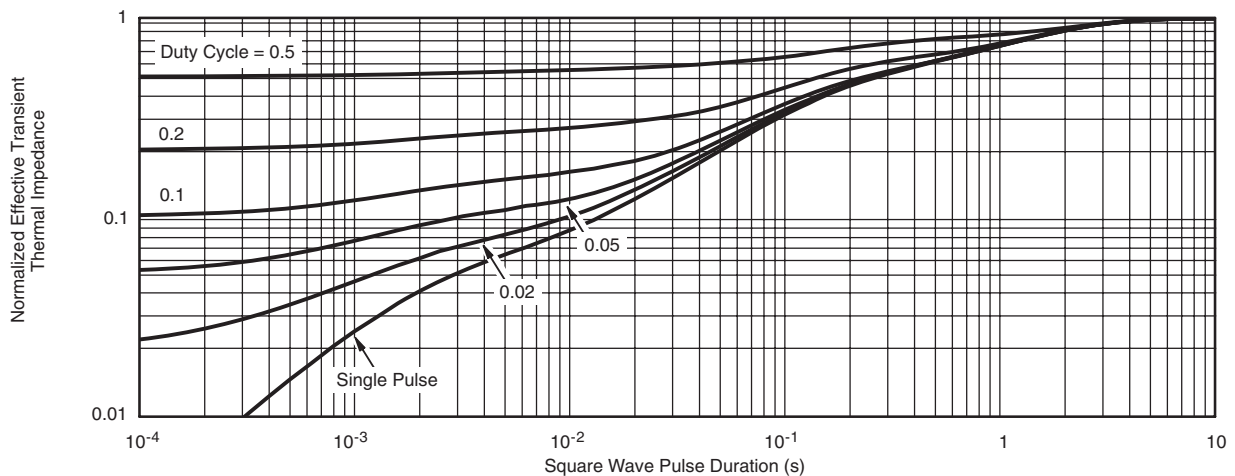
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?69054>.

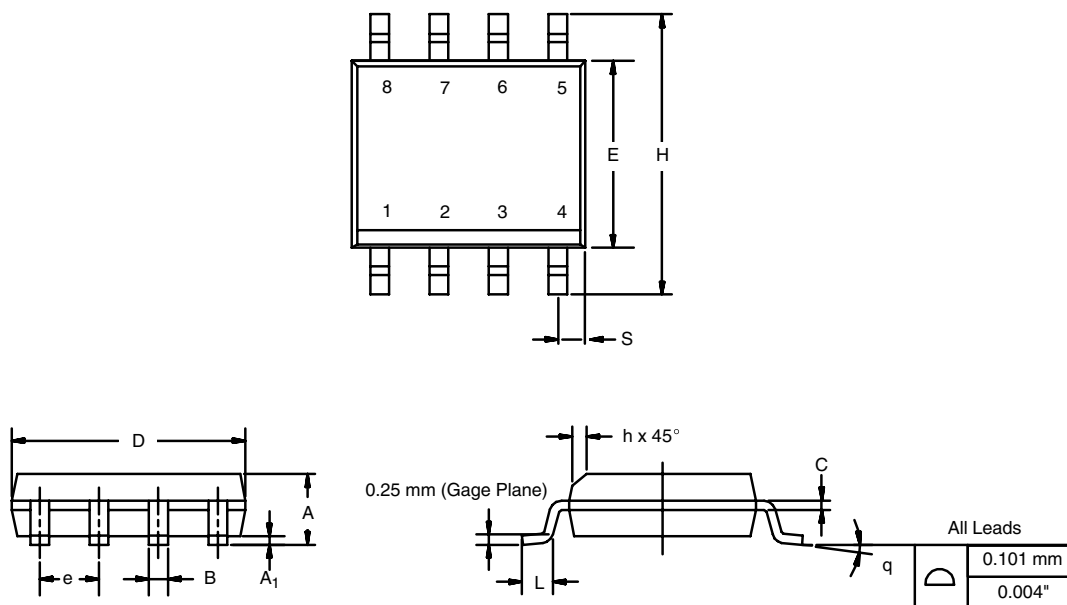


Package Information

Vishay Siliconix

SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026

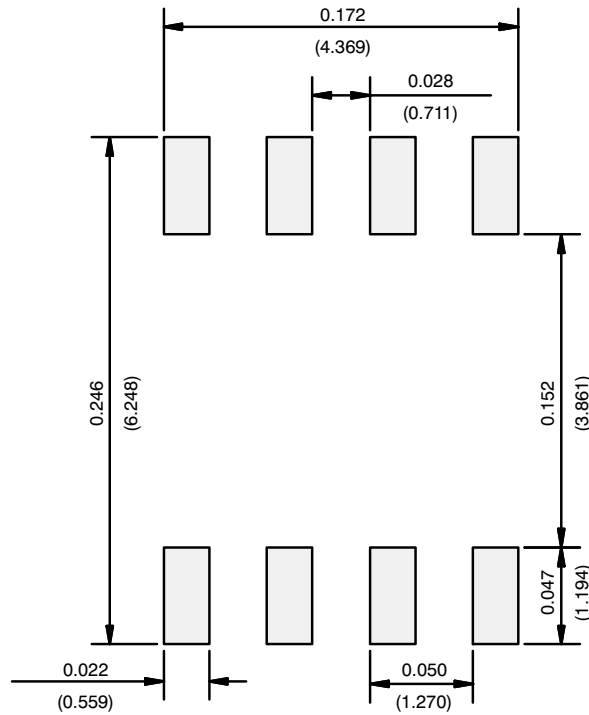
ECN: C-06527-Rev. I, 11-Sep-06
DWG: 5498

Application Note 826

Vishay Siliconix



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
 Dimensions in Inches/(mm)

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APPLICATION NOTE



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