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[Vishay/Siliconix](#)
[SI4532ADY-T1-E3](#)

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sales@integrated-circuit.com



Si4532ADY
 Vishay Siliconix

N- and P-Channel 30 V (D-S) MOSFET

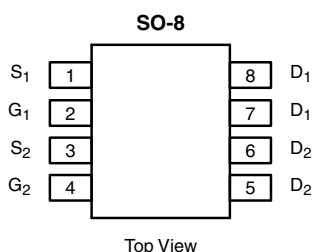
PRODUCT SUMMARY			
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)
N-Channel	30	0.053 at V _{GS} = 10 V	4.9
		0.075 at V _{GS} = 4.5 V	4.1
P-Channel	- 30	0.080 at V _{GS} = - 10 V	- 3.9
		0.135 at V _{GS} = - 4.5 V	- 3.0

FEATURES

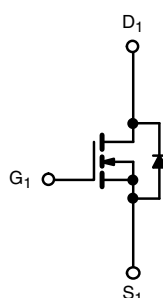
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFETs
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC



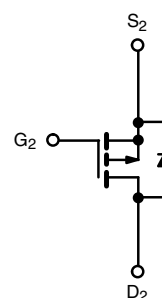
RoHS
 COMPLIANT
 HALOGEN
FREE
 Available



Ordering Information:
 Si4532ADY-T1-E3 (Lead (Pb-free))
 Si4532ADY-T1-GE3 (Lead (Pb-free and Halogen-free))



N-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)							
Parameter	Symbol	N-Channel		P-Channel		Unit	
		10 s	Steady State	10 s	Steady State		
Drain-Source Voltage	V _{DS}	30		- 30		V	
Gate-Source Voltage	V _{GS}	± 20		± 20		V	
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	4.9	3.7	- 3.9	- 3.0	A
		T _A = 70 °C	3.9	2.9	- 3.1	- 2.4	
Pulsed Drain Current	I _{DM}	20				A	
Continuous Source Current (Diode Conduction) ^a	I _S	1.7	0.94	- 1.7	- 1.0	A	
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	2	1.13	2	1.2	W
		T _A = 70 °C	1.3	0.73	1.3	0.76	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150				°C	

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	N-Channel		P-Channel		Unit	
		Typ.	Max.	Typ.	Max.		
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 10 s	55	62.5	54	62.5	°C/W
		Steady State	90	110	87	105	
Maximum Junction-to-Foot (Drain)	R _{thJF}	40	50	34	45	°C/W	

Note:

a. Surface mounted on 1" x 1" FR4 board.

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SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	N-Ch	1			V
		$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	P-Ch	-1			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$	N-Ch			± 100	nA
		$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$	P-Ch			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\ \text{V}, V_{GS} = 0\ \text{V}$	N-Ch			1	μA
		$V_{DS} = -30\ \text{V}, V_{GS} = 0\ \text{V}$	P-Ch			-1	
		$V_{DS} = 30\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55\text{ }^\circ\text{C}$	N-Ch			5	
		$V_{DS} = -30\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55\text{ }^\circ\text{C}$	P-Ch			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}, V_{GS} = 10\ \text{V}$	N-Ch	20			A
		$V_{DS} \leq -5\ \text{V}, V_{GS} = -10\ \text{V}$	P-Ch	-20			
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\ \text{V}, I_D = 4.9\ \text{A}$	N-Ch		0.044	0.053	Ω
		$V_{GS} = -10\ \text{V}, I_D = -3.9\ \text{A}$	P-Ch		0.062	0.080	
		$V_{GS} = 4.5\ \text{V}, I_D = 4.1\ \text{A}$	N-Ch		0.062	0.075	
		$V_{GS} = -4.5\ \text{V}, I_D = -3\ \text{A}$	P-Ch		0.105	0.135	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}, I_D = 4.9\ \text{A}$	N-Ch		11		S
		$V_{DS} = -15\ \text{V}, I_D = -2.5\ \text{A}$	P-Ch		5		
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.7\ \text{A}, V_{GS} = 0\ \text{V}$	N-Ch		0.80	1.2	V
		$I_S = -1.7\ \text{A}, V_{GS} = 0\ \text{V}$	P-Ch		-0.82	-1.2	
Dynamic^b							
Total Gate Charge	Q_g	N-Channel $V_{DS} = 10\ \text{V}, V_{GS} = 10\ \text{V}, I_D = 4.9\ \text{A}$	N-Ch		8	16	nC
Gate-Source Charge	Q_{gs}		P-Ch		10	20	
Gate-Drain Charge	Q_{gd}	P-Channel $V_{DS} = -4\ \text{V}, V_{GS} = -10\ \text{V}, I_D = -3.9\ \text{A}$	N-Ch		1.4		
			P-Ch		2		
Gate Resistance ^c	R_g	$f = 1\ \text{MHz}$	N-Ch	0.4	1.6	3.2	Ω
			P-Ch	1.5	6.2	12	
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 10\ \text{V}, R_L = 10\ \Omega$ $I_D \cong 1\ \text{A}, V_{GEN} = 10\ \text{V}, R_g = 6\ \Omega$	N-Ch		12	20	ns
Rise Time	t_r		P-Ch		8	15	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -10\ \text{V}, R_L = 10\ \Omega$ $I_D \cong -1\ \text{A}, V_{GEN} = -10\ \text{V}, R_g = 6\ \Omega$	N-Ch		23	45	
			P-Ch		21	40	
Fall Time	t_f		N-Ch		8	15	
			P-Ch		10	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.7\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$	N-Ch		25	40	
		$I_F = -1.7\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$	P-Ch		27	40	

Notes:

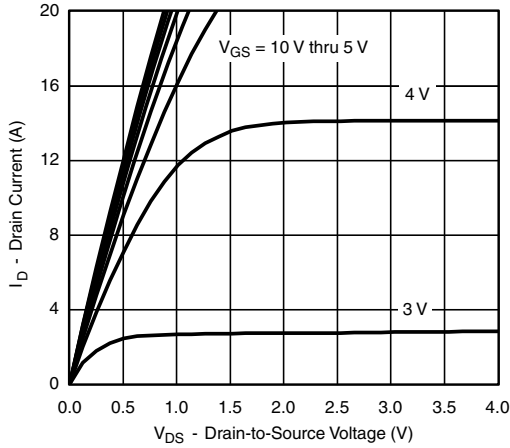
- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

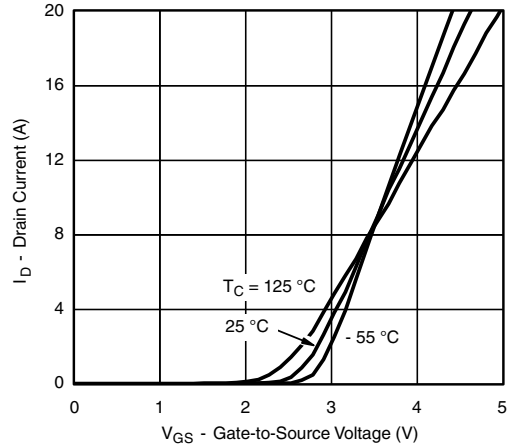


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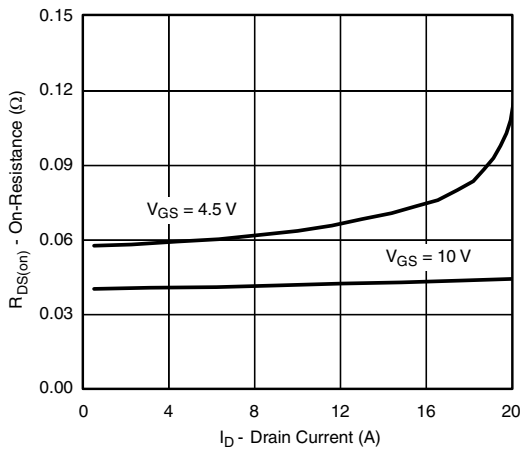
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



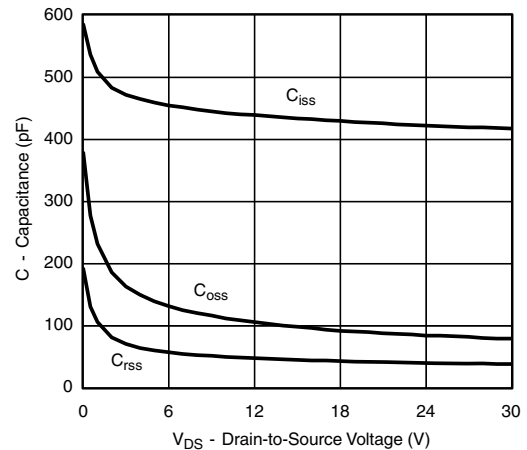
Output Characteristics



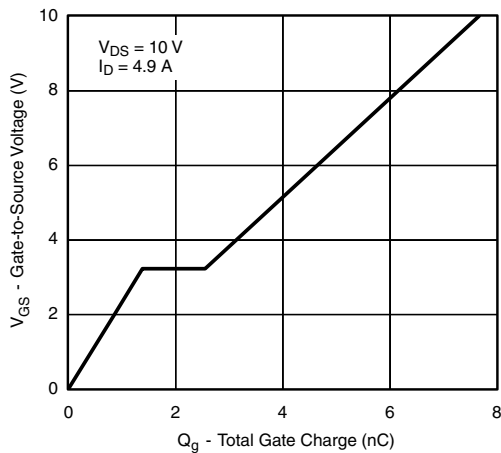
Transfer Characteristics



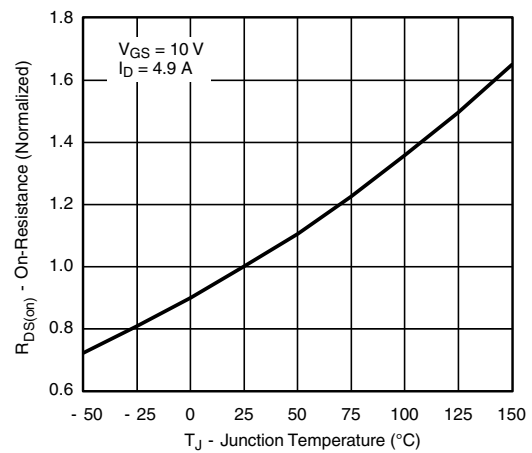
On-Resistance vs. Drain Current



Capacitance



Gate Charge

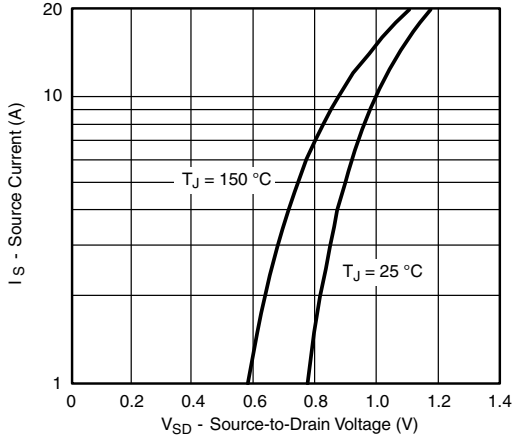


On-Resistance vs. Junction Temperature

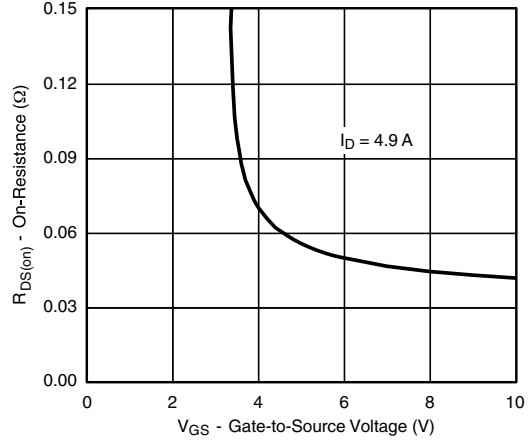
Si4532ADY
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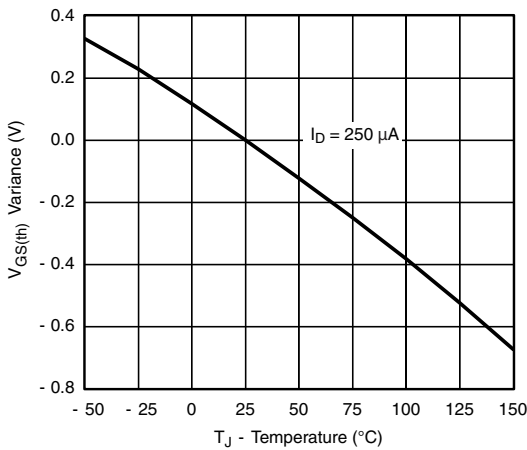
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



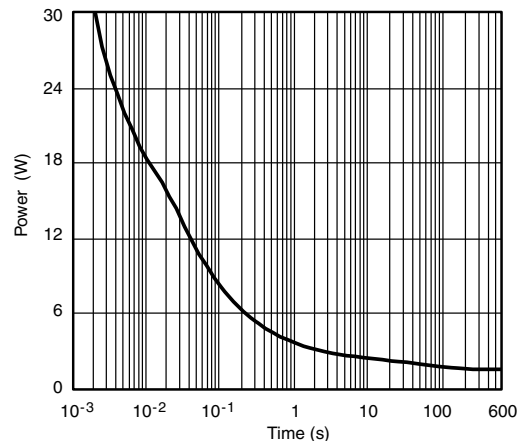
Source-Drain Diode Forward Voltage



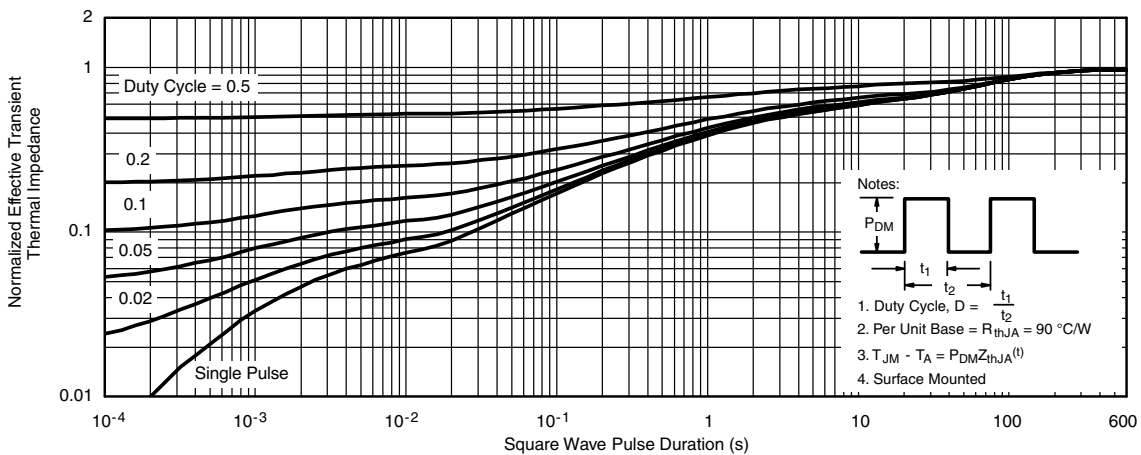
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power

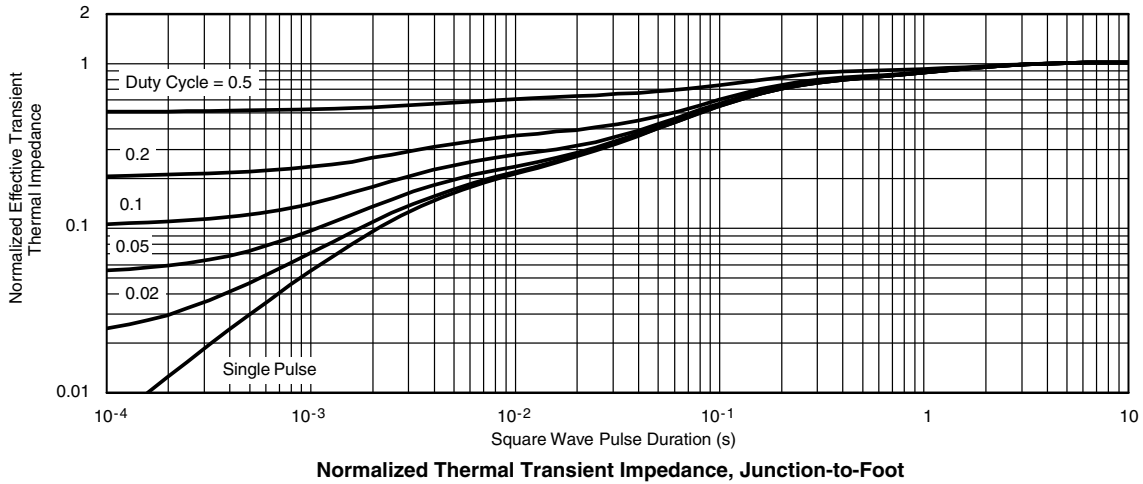


Normalized Thermal Transient Impedance, Junction-to-Ambient



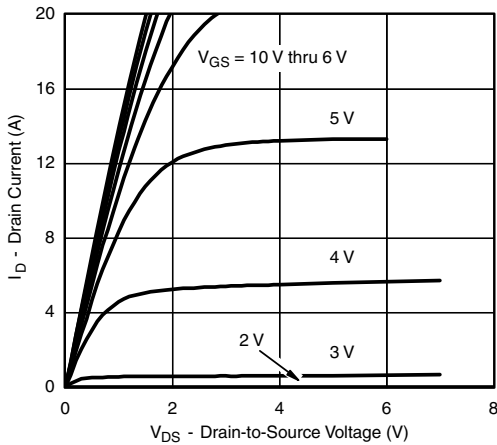
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N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

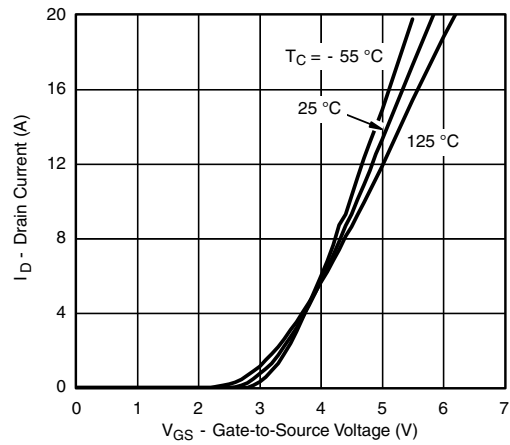


Normalized Thermal Transient Impedance, Junction-to-Foot

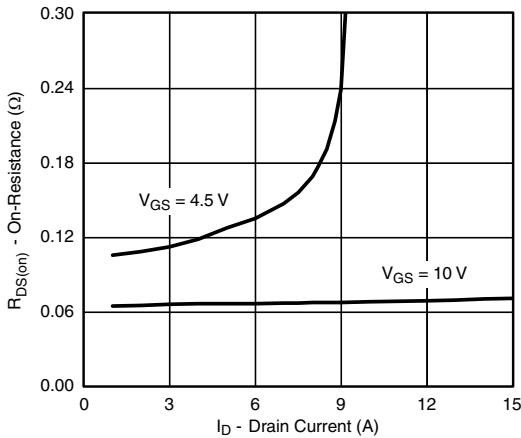
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



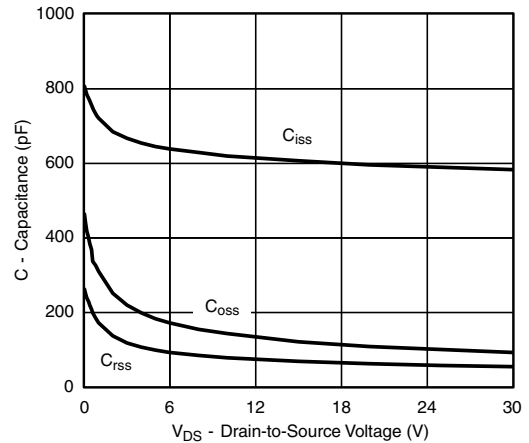
Output Characteristics



Transfer Characteristics



On-Resistance vs. Drain Current



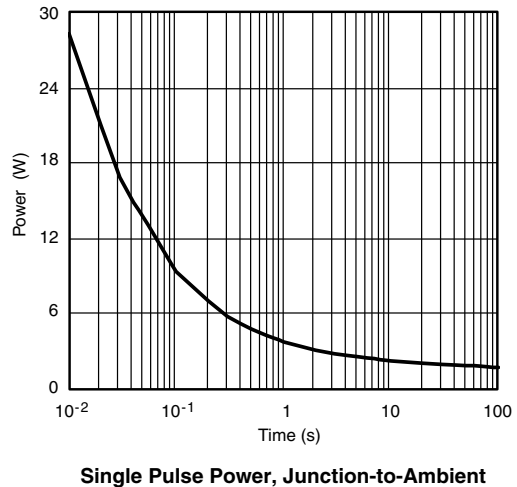
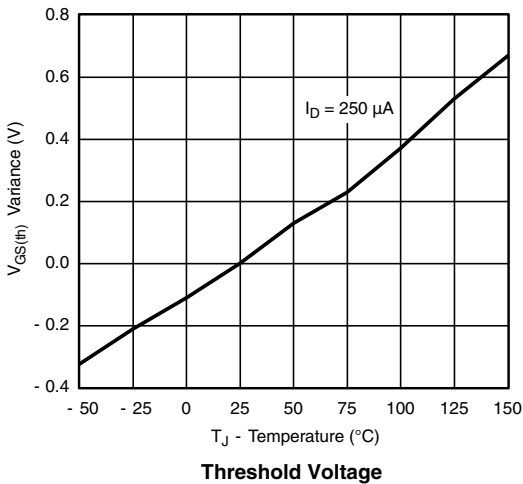
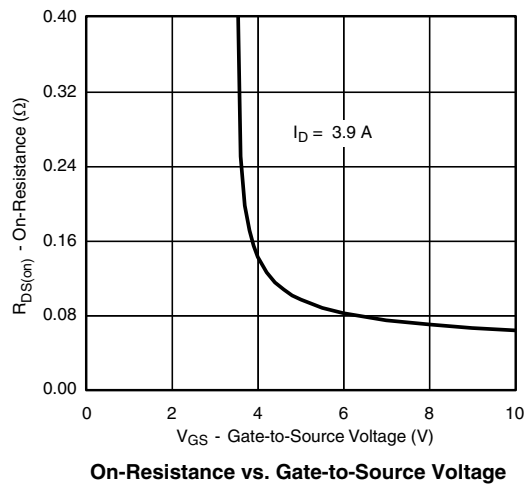
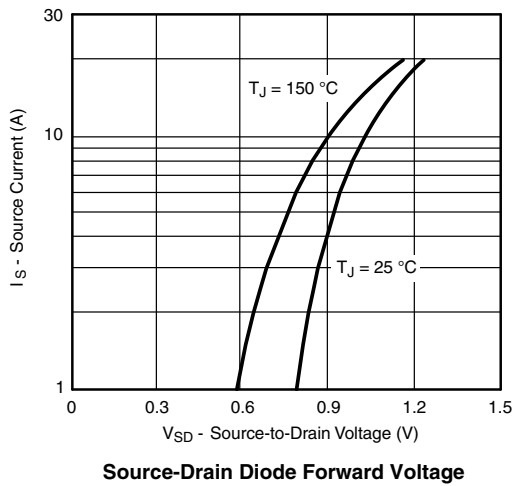
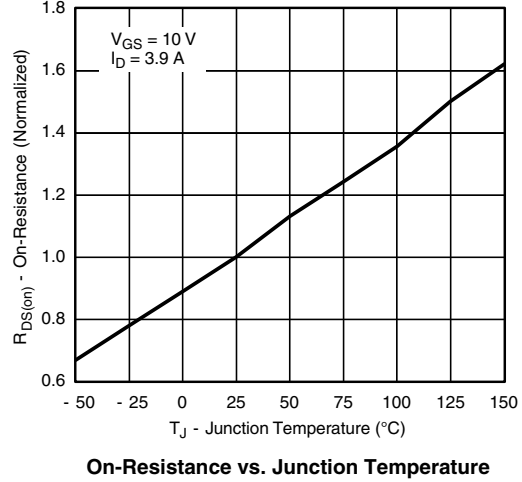
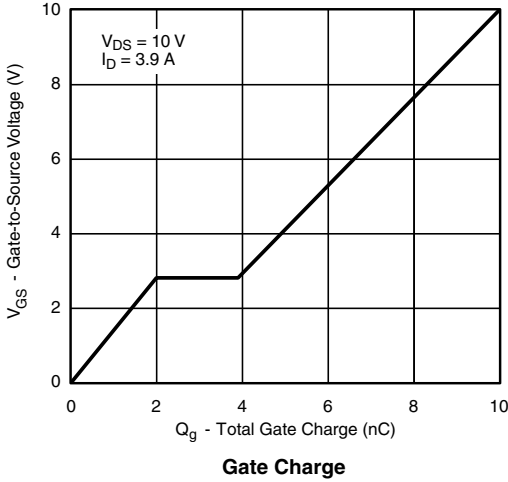
Capacitance

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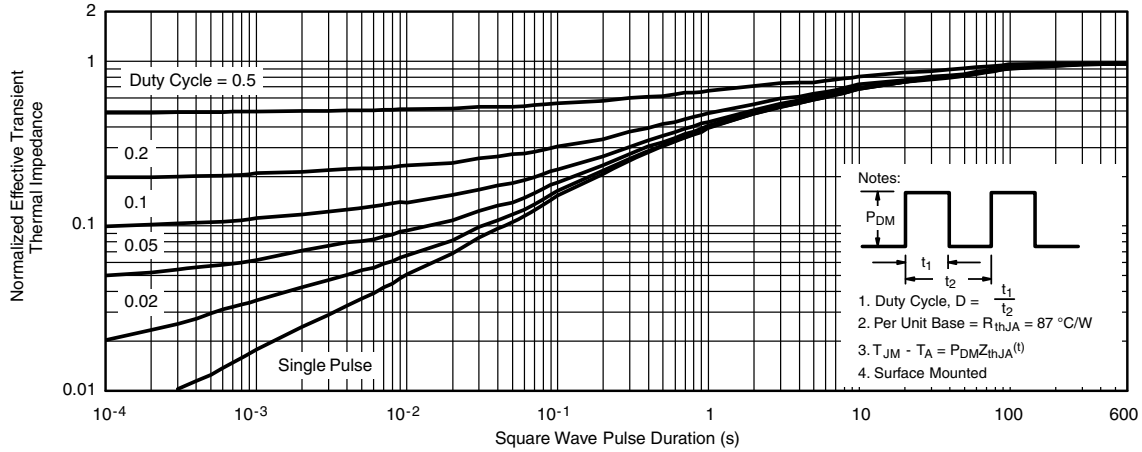
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



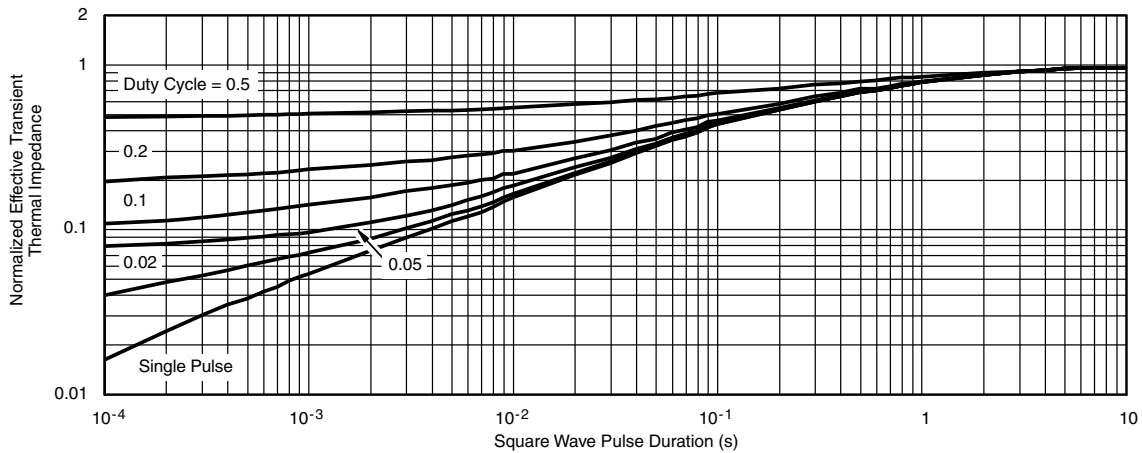


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P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71133.

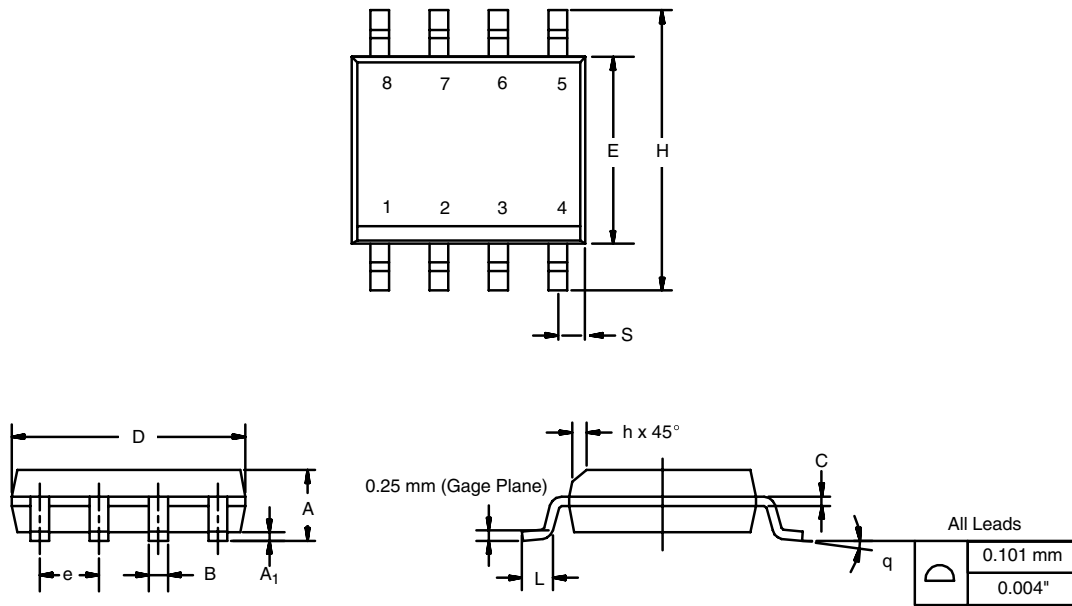


Package Information

Vishay Siliconix

SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026

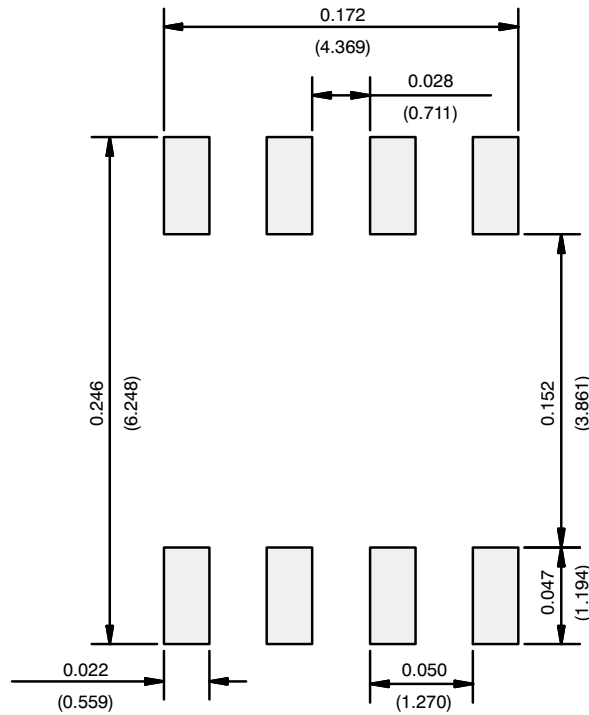
ECN: C-06527-Rev. I, 11-Sep-06
 DWG: 5498

Application Note 826

Vishay Siliconix



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
 Dimensions in Inches/(mm)

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APPLICATION NOTE



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