Excellent Integrated System Limited

Stocking Distributor

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Vishay/Siliconix
SI7392DP-T1-E3

For any questions, you can email us directly:
sales@integrated-circuit.com

N-Channel Reduced Q_g, Fast Switching MOSFET

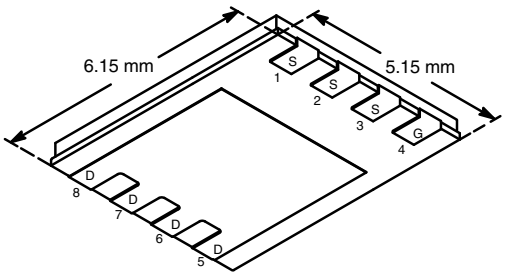
PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
30	0.00975 at V_{GS} = 10 V	15
	0.01375 at V_{GS} = 4.5 V	13

FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- Extremely Low Q_{gd} for Low Switching Losses
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07 mm Profile
- 100 % R_g Tested
- 100 % UIS Tested
- Complaint to RoHS Directive 2002/95/EC

Available
RoHS* COMPLIANT
HALOGEN FREE Available

PowerPAK SO-8

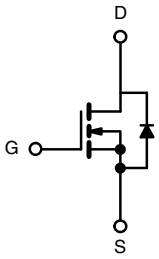


Bottom View

Ordering Information: Si7392DP-T1-E3 (Lead (Pb)-free)
Si7392DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

APPLICATIONS

- High-Side DC/DC Conversion
  - Notebook
  - Server



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)					
Parameter		**Symbol**	**10 s**	**Steady State**	**Unit**
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	15	9	A
	T_A = 70 °C		12	7	
Pulsed Drain Current		I_{DM}	± 50		
Continuous Source Current (Diode Conduction)[a]		I_S	4.1	1.5	
Avalanche Current	L = 0.1 mH	I_{AS}	30		
Single-Pulse Avalanche Energy		E_{AS}	45		mJ
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	5	1.8	W
	T_A = 70 °C		3.2	1.1	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature)[b, c]			260		

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient (MOSFET)[a]	t ≤ 10 s	R_{thJA}	20	25	°C/W
	Steady State		53	70	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	3.5	4.5	

Notes:
a. Surface mounted on 1" x 1" FR4 board.
b. See solder profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

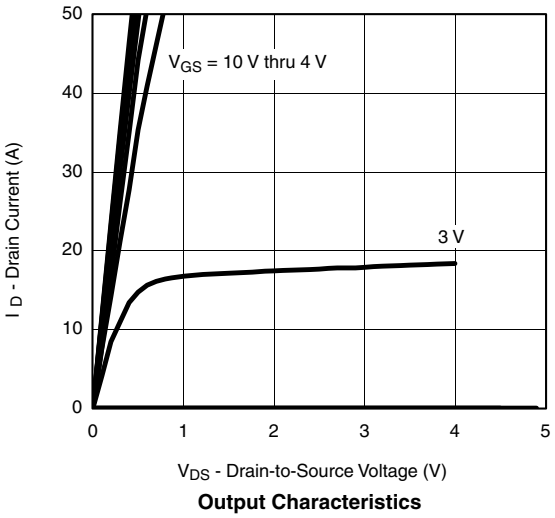
* Pb containing terminations are not RoHS compliant, exemptions may apply.

MOSFET SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.0		3.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			1	µA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 70 °C			5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	40			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 15 A		0.008	0.00975	Ω
		V_{GS} = 4.5 V, I_D = 13 A		0.011	0.01375	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 15 A		40		S
Diode Forward Voltage[a]	V_{SD}	I_S = 4.1 A, V_{GS} = 0 V		0.75	1.1	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 15 A		10	15	nC
Gate-Source Charge	Q_{gs}			3.5		
Gate-Drain Charge	Q_{gd}			2.6		
Gate Resistance	R_g			1.6	2.7	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 15 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_g = 6 Ω		15	25	ns
Rise Time	t_r			7	15	
Turn-Off Delay Time	$t_{d(off)}$			46	70	
Fall Time	t_f			9	17	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2.7 A, dI/dt = 100 A/µs		30	60	

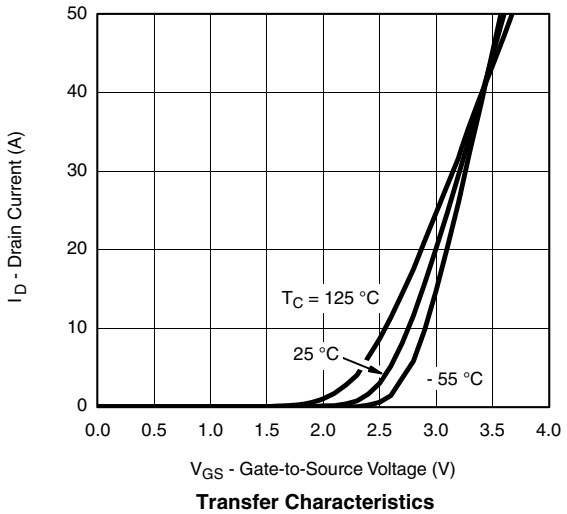
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

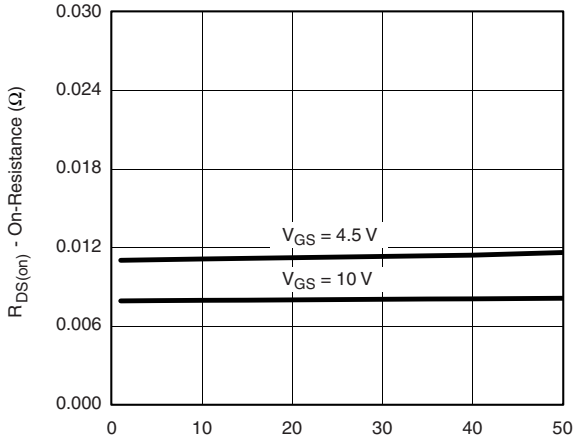


Output Characteristics

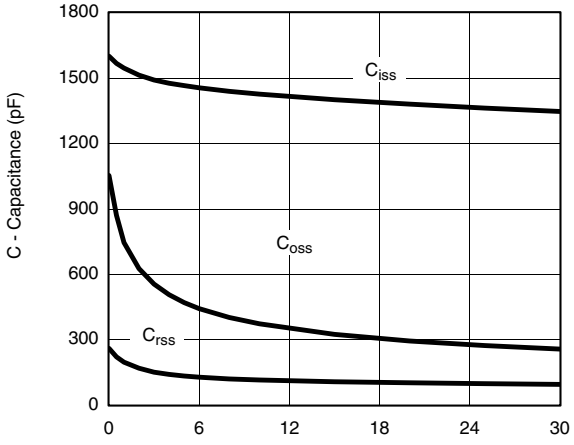


Transfer Characteristics

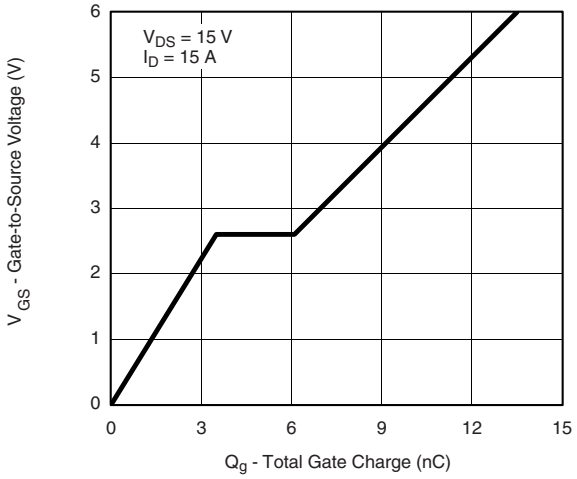
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



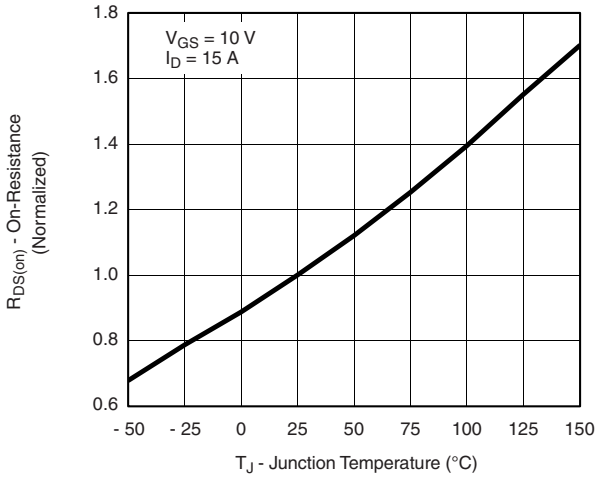
On-Resistance vs. Drain Current



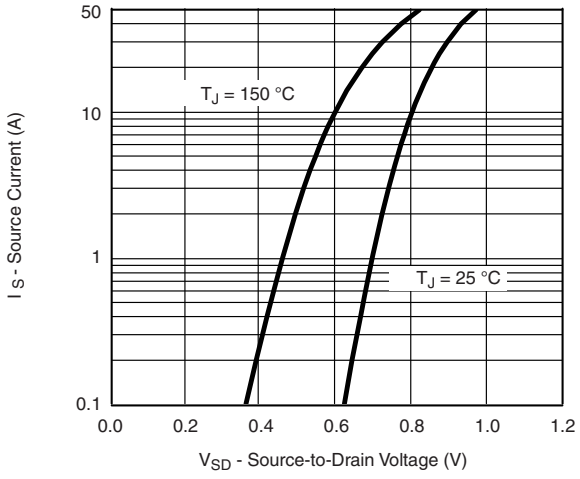
Capacitance



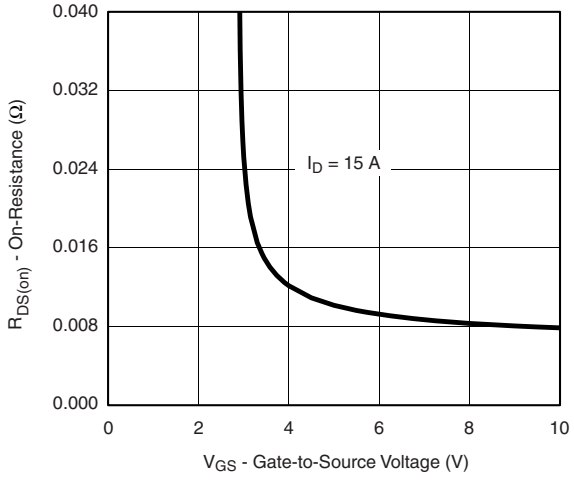
Gate Charge



On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

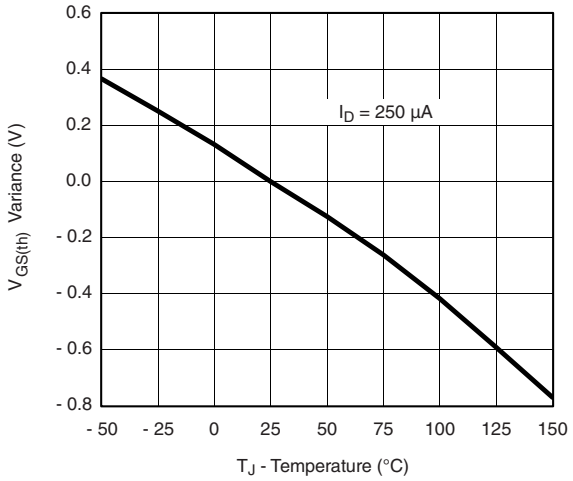


On-Resistance vs. Gate-to-Source Voltage

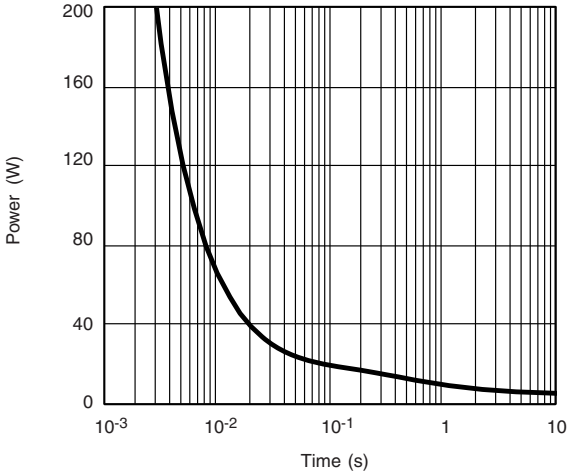
Si7392DP

Vishay Siliconix

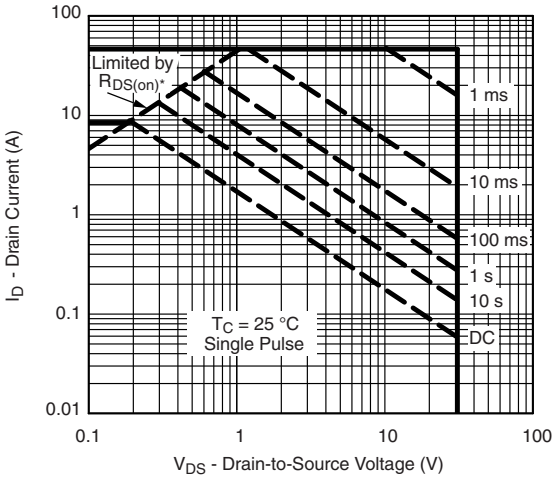
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Threshold Voltage

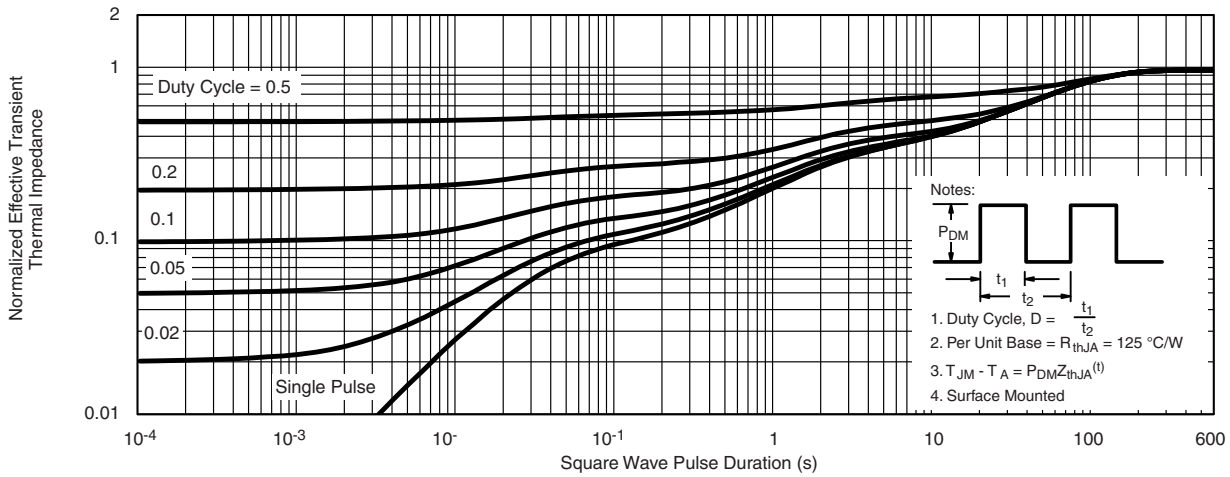


Single Pulse Power



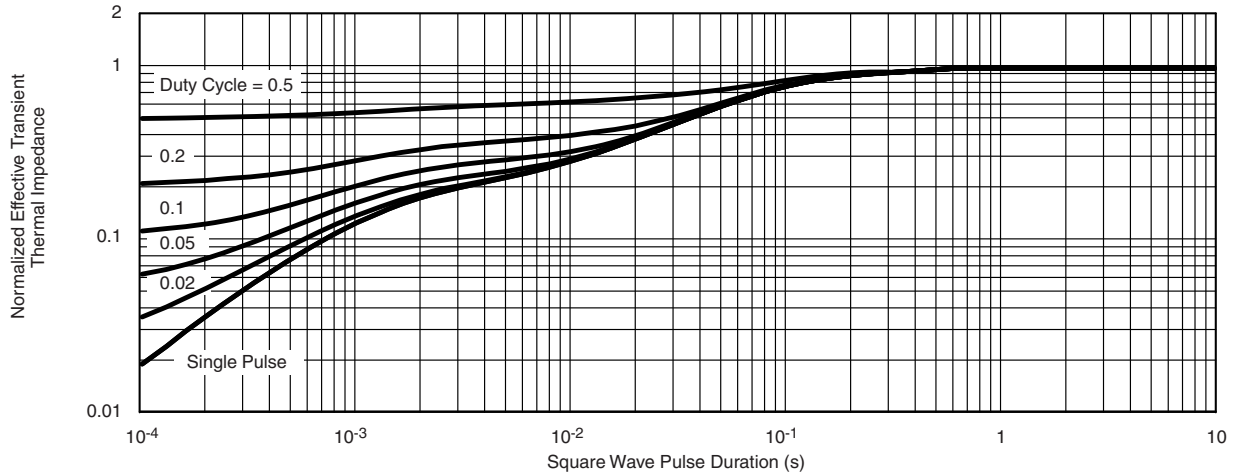
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Foot

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