

# **Excellent Integrated System Limited**

Stocking Distributor

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Vishay/Siliconix SI7404DN-T1-E3

For any questions, you can email us directly: sales@integrated-circuit.com





#### **Si7404DN**

Vishay Siliconix

# N-Channel 30 V (D-S) Fast Switching MOSFET

| PRODUCT SUMMARY     |                                  |                    |  |  |
|---------------------|----------------------------------|--------------------|--|--|
| V <sub>DS</sub> (V) | $R_{DS(on)}(\Omega)$             | I <sub>D</sub> (A) |  |  |
| 30                  | 0.013 at V <sub>GS</sub> = 10 V  | 13.3               |  |  |
|                     | 0.015 at V <sub>GS</sub> = 4.5 V | 12.4               |  |  |
|                     | 0.022 at V <sub>GS</sub> = 2.5 V | 10.2               |  |  |

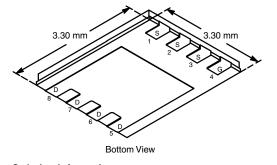
# **FEATURES**

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFET
- Compliant to RoHS Directive 2002/95/EC



#### **APPLICATIONS**

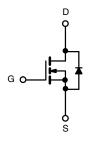
· Li-lon Battery Protection



PowerPAK® 1212-8

Ordering Information: Si7404DN-T1-E3 (Lead (Pb)-free)

Si7404DN-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

| <b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>A</sub> = 25 °C, unless otherwise noted) |                        |                                   |             |              |      |  |
|--|------------------------|-----------------------------------|-------------|--------------|------|--|
| Parameter  |                        | Symbol                            | 10 s        | Steady State | Unit |  |
| Drain-Source Voltage   |                        | V <sub>DS</sub>                   | 30          |              | V    |  |
| Gate-Source Voltage  |                        | $V_{GS}$                          | ± 12        |              |      |  |
| Continuous Drain Current (T <sub>.I</sub> = 150 °C) <sup>a</sup>                 | T <sub>A</sub> = 25 °C |                                   | 13.3        | 8.5          |      |  |
| Continuous Diam Current (1) = 150 °C)  | T <sub>A</sub> = 70 °C |                                   | 10.6        | 6.8          | A    |  |
| Pulsed Drain Current   |                        | I <sub>DM</sub>                   | 40          |              | А    |  |
| Single Avalanche Current   | 0.1 mH                 | I <sub>AS</sub>                   | 15          |              |      |  |
| Single Avalanche Energy (Duty Cycle 1 %)   | 0.11                   | E <sub>AS</sub>                   | 11          |              | mJ   |  |
| Continuous Source Current (Diode Conduction) <sup>a</sup>                        |                        | I <sub>S</sub>                    | 3.2         | 1.3          | Α    |  |
| Maximum Power Dissipation <sup>a</sup>   | T <sub>A</sub> = 25 °C | P <sub>D</sub>                    | 3.8         | 1.5          | W    |  |
| Maximum Fower Dissipation  | T <sub>A</sub> = 70 °C |                                   | 2.0         | 0.8          | ]    |  |
| Operating Junction and Storage Temperature Range                                 |                        | T <sub>J</sub> , T <sub>stg</sub> | - 55 to 150 |              | °C   |  |
| Soldering Recommendations <sup>b,c</sup>   |                        |                                   | 260         |              | C    |  |

| THERMAL RESISTANCE RATINGS               |              |                     |         |         |      |
|--|--------------|---------------------|---------|---------|------|
| Parameter                                |              | Symbol              | Typical | Maximum | Unit |
| Maximum Junction-to-Ambient <sup>a</sup> | t ≤ 10 s     | - R <sub>thJA</sub> | 26      | 33      | °C/W |
|  | Steady State |                     | 65      | 81      |      |
| Maximum Junction-to-Case (Drain)         | Steady State | R <sub>thJC</sub>   | 1.9     | 2.4     | 1    |

#### Notes:

- a. Surface Mounted on 1" x 1" FR4 board.
- b. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

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Datasheet of SI7404DN-T1-E3 - MOSFET N-CH 30V 8.5A PPAK 1212-8

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#### **Si7404DN**

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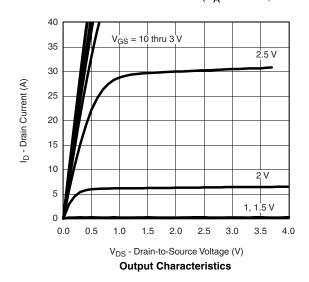
| MOSFET SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted) |                     |  |      |        |       |      |  |
|--|---------------------|--|------|--------|-------|------|--|
| Parameter  | Symbol              | Test Conditions  | Min. | Тур.   | Max.  | Unit |  |
| Static   |                     |  |      |        |       |      |  |
| Gate Threshold Voltage   | $V_{GS(th)}$        | $V_{DS} = V_{GS}$ , $I_D = 250 \mu A$                                      | 0.6  |        | 1.5   | V    |  |
| Gate-Body Leakage  | I <sub>GSS</sub>    | $V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$                          |      |        | ± 100 | nA   |  |
| Zero Gate Voltage Drain Current  | I <sub>DSS</sub>    | $V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$                              |      |        | 1     |      |  |
|  |                     | $V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$ |      |        | 5     | μΑ   |  |
| On-State Drain Current <sup>a</sup>                                    | I <sub>D(on)</sub>  | $V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$                            | 40   |        |       | Α    |  |
|  |                     | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 13.3 A                            |      | 0.010  | 0.013 | Ω    |  |
| Drain-Source On-State Resistance <sup>a</sup>                          | R <sub>DS(on)</sub> | $V_{GS} = 4.5 \text{ V}, I_D = 12.4 \text{ A}$                             |      | 0.0125 | 0.015 |      |  |
|  | ` ′                 | $V_{GS} = 2.5 \text{ V}, I_D = 5 \text{ A}$                                |      | 0.019  | 0.022 |      |  |
| Forward Transconductance <sup>a</sup>                                  | 9 <sub>fs</sub>     | V <sub>DS</sub> = 5 V, I <sub>D</sub> = 13.3 A                             |      | 50     |       | S    |  |
| Diode Forward Voltage <sup>a</sup>                                     | $V_{SD}$            | $I_S = 3.2 \text{ A}, V_{GS} = 0 \text{ V}$                                |      | 0.75   | 1.2   | V    |  |
| Dynamic <sup>b</sup>   |                     |  |      |        |       |      |  |
| Total Gate Charge  | $Q_g$               |  |      | 20     | 30    |      |  |
| Gate-Source Charge   | Q <sub>gs</sub>     | $V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 13.3 \text{ A}$      |      | 5.8    |       | nC   |  |
| Gate-Drain Charge  | $Q_{gd}$            |  |      | 7.1    |       | 1    |  |
| Turn-On Delay Time   | t <sub>d(on)</sub>  |  |      | 27     | 40    |      |  |
| Rise Time  | t <sub>r</sub>      | $V_{DD}$ = 15 V, $R_L$ = 15 $\Omega$                                       |      | 39     | 60    | ns   |  |
| Turn-Off DelayTime   | t <sub>d(off)</sub> | $I_D\cong$ 1 A, $V_{GEN}$ = 4.5 V, $R_G$ = 6 $\Omega$                      |      | 64     | 100   |      |  |
| Fall Time  | t <sub>f</sub>      |  |      | 33     | 50    |      |  |
| Source-Drain Reverse Recovery<br>Time                                  | t <sub>rr</sub>     | r I <sub>F</sub> = 3.2 A, dl/dt = 100 A/μs                                 |      | 45     | 90    |      |  |

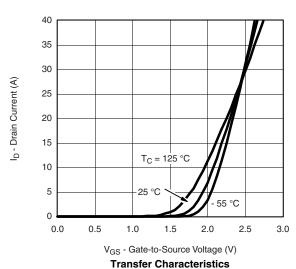
#### Notes:

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)





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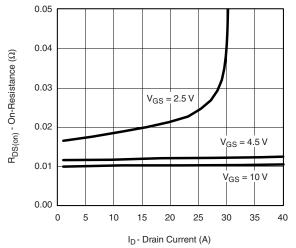




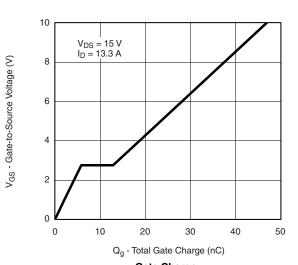
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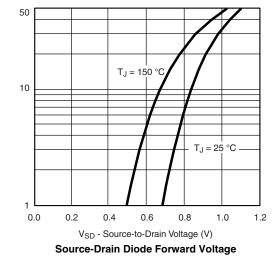
### TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



#### On-Resistance vs. Drain Current

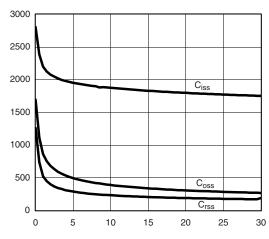


**Gate Charge** 



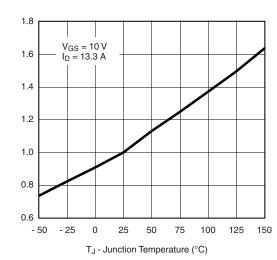
C - Capacitance (pF)

R<sub>DS(on)</sub> - On-Resistance (Normalized)

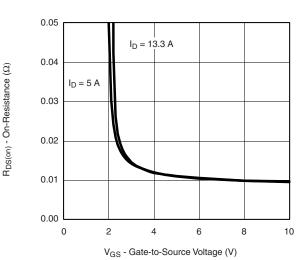


V<sub>DS</sub> - Drain-to-Source Voltage (V)

#### Capacitance



On-Resistance vs. Junction Temperature



On-Resistance vs. Gate-to-Source Voltage

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Is- Source Current (A)

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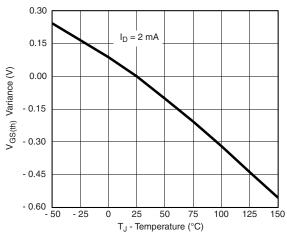


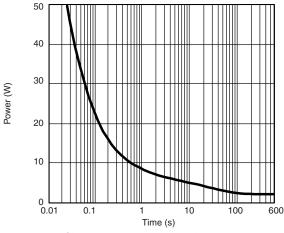
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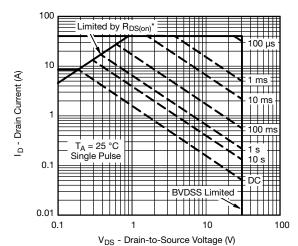
#### **TYPICAL CHARACTERISTICS** ( $T_A = 25$ °C, unless otherwise noted)





**Threshold Voltage** 

Single Pulse Power, Junction-to-Ambient



\*  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area, Junction-to-Ambient

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Datasheet of SI7404DN-T1-E3 - MOSFET N-CH 30V 8.5A PPAK 1212-8

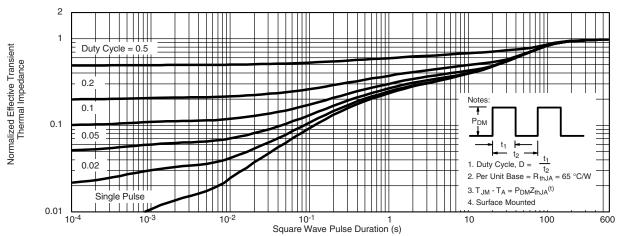
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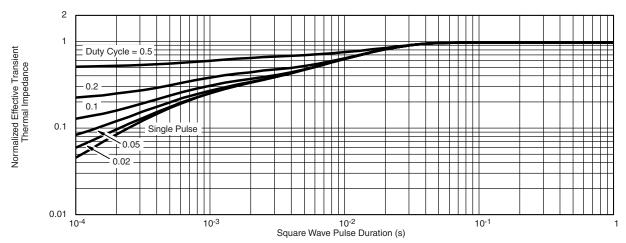
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#### TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?71658">www.vishay.com/ppg?71658</a>.

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