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Vishay/Siliconix SIE726DF-T1-E3

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SiE726DF

RoHS

COMPLIANT

HALOGEN

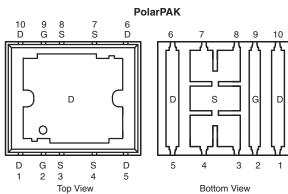
FREE

Vishay Siliconix

N-Channel 30-V (D-S) MOSFET with Schottky Diode

PRODUCT SUMMARY					
		I _D (A) ^a			
V _{DS} (V)	R _{DS(on)} (Ω) ^e	Silicon Limit	Package Limit	Q _g (Typ.)	
30	0.0024 at V _{GS} = 10 V	175	60	50 nC	
30	0.0033 at $V_{GS}\!=\!4.5V$	149	60	50 110	

Package Drawing www.vishay.com/doc?72945



Top surface is connected to pins 1, 5, 6, and 10 Ordering Information: SiE726DF-T1-E3 (Lead (Pb)-free)

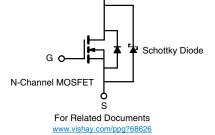
SiE726DF-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- Halogen-free According to IEC 61249-2-21
 Definition
- SkyFET[™] Monolithic TrenchFET[®] Power MOSFET and Schottky Diode
- Ultra Low Thermal Resistance Using Top-Exposed PolarPAK[®] Package for Double-Sided Cooling
- Leadframe-Based New Encapsulated Package
- Die Not Exposed
- Same Layout Regardless of Die Size
- Low Q_{gd}/Q_{gs} Ratio Helps Prevent Shoot-Through
- 100 % R_g and UIS Tested
- Compliant to RoHS directive 2002/95/EC

APPLICATIONS

- · Synchronous Rectification
- DC/DC
- · Low-Side Switch



D

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	30	V	
Gate-Source Voltage		V _{GS}	± 20	v	
	T _C = 25 °C		175 (Silicon Limit)		
	$1_{\rm C} = 25$ C		60 ^a (Package Limit)		
Continuous Drain Current (T _J = 150 °C)	T _C = 70 °C	I _D	60 ^a		
	T _A = 25 °C		35 ^{b, c}		
	T _A = 70 °C		28 ^{b, c}	A	
Pulsed Drain Current		I _{DM}	80		
Continuous Source-Drain Diode Current	T _C = 25 °C		60 ^a		
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	4.3 ^{b, c}		
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	50		
Avalanche Energy		E _{AS}	125	mJ	
	T _C = 25 °C		125		
Maximum Power Dissipation	T _C = 70 °C	P _D	80	w	
	T _A = 25 °C		5.2 ^{b, c}	•••	
	T _A = 70 °C		3.3 ^{b, c}		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{d, e}			260		

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. See Solder Profile (<u>www.vishay.com/ppg?73257</u>). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.



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THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{a, b}	t ≤ 10 s	R _{thJA}	20	24		
Maximum Junction-to-Case (Drain Top)	Steady State	R _{thJC} (Drain)	0.8	1	°C/W	
Maximum Junction-to-Case (Source) ^{a, c}	Sleady State	R _{thJC} (Source)	2.2	2.7		

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. Maximum under Steady State conditions is 68 °C/W.

c. Measured at source pin (on the side of the package).

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 V$, $I_D = 1 mA$	30			V	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	1		3	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$		0.120	0.5	mA	
		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$		1.0	10		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, \text{ V}_{GS} = 10 \text{ V}$	25			А	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 25 A		0.0020	0.0024	Ω	
		$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 25 \text{ A}$		0.0026	0.0033		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 25 A		90		S	
Dynamic ^b							
Input Capacitance	C _{iss}			7400		pF	
Output Capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		1100			
Reverse Transfer Capacitance	C _{rss}			400			
Table Oats Observe		V _{DS} = 15 V, V _{GS} = 10 V, I _D = 20 A		105	160		
Total Gate Charge	Qg			50	75		
Gate-Source Charge	Q _{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 20 \text{ A}$		22		nC	
Gate-Drain Charge	Q _{gd}			12			
Gate Resistance	R _g	f = 1 MHz		1	2	Ω	
Turn-On Delay Time	t _{d(on)}			60	90	ns	
Rise Time	ťr	V_{DD} = 15 V, R_L = 1.5 Ω		35	55		
Turn-Off Delay Time	t _{d(off)}	${ m I}_{ m D}\cong$ 10 A, ${ m V}_{ m GEN}$ = 4.5 V, ${ m R}_{ m q}$ = 1 Ω		55	85		
Fall Time	t _f	с С		30	45		
Turn-On Delay Time	t _{d(on)}			20	30		
Rise Time	t _r	V_{DD} = 15 V, R_L = 1.5 Ω		10	15		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 10 \text{ A}, \text{ V}_{\text{GEN}} = 10 \text{ V}, \text{ R}_{\text{g}} = 1 \Omega$		55	85		
Fall Time	t _f	- v		10	15		
Drain-Source Body Diode and Schottky	Characteristi	cs					
Continuous Source-Drain Diode Current	۱ _S	T _C = 25 °C			60	A	
Pulse Diode Forward Current ^a	I _{SM}	~	1	1	80		
Body Diode Voltage	V _{SD}	I _S = 2 A	1	0.37	0.45	V	
Body Diode Reverse Recovery Time	t _{rr}	5	1	40	60	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			30	45	nC	
Reverse Recovery Fall Time	t _a	$I_F = 10 \text{ A}, \text{ dl/dt} = 100 \text{ A/}\mu\text{s}, \text{ T}_J = 25 \text{ °C}$		19	-		
Reverse Recovery Rise Time	t _b			21		ns	

Notes:

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

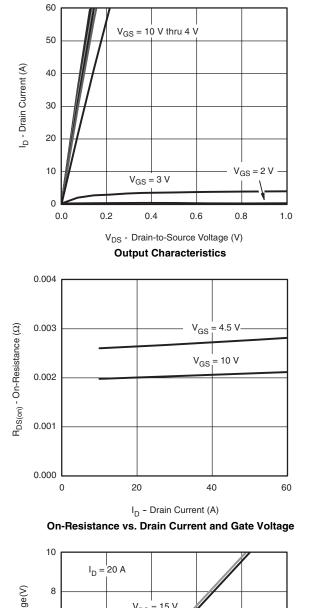


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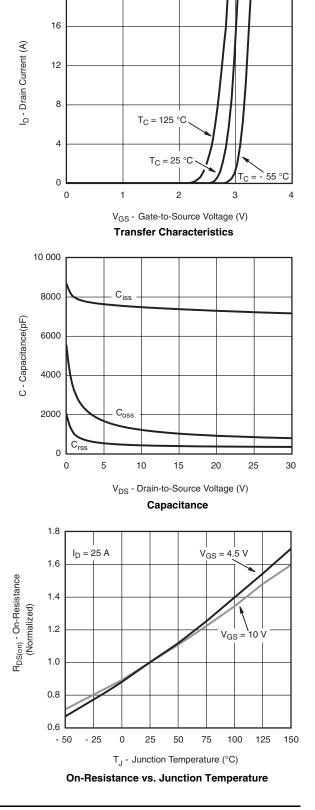


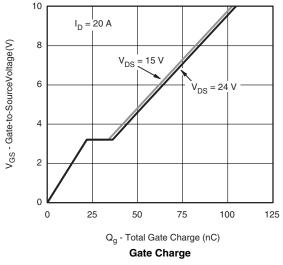
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





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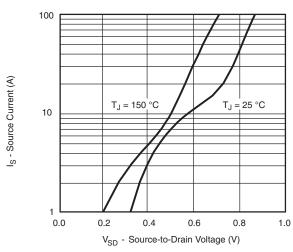


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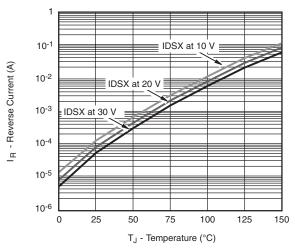




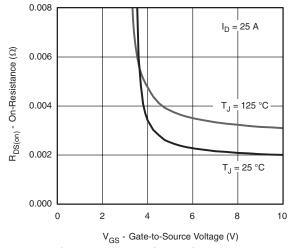
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



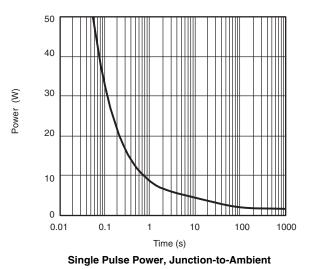
Source-Drain Diode Forward Voltage

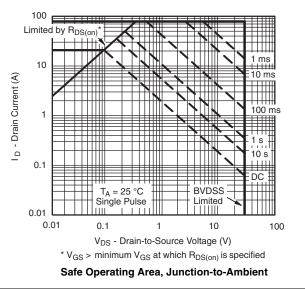


Reverse Current vs. Junction Temperature



On-Resistance vs. Gate-to-Source Voltage





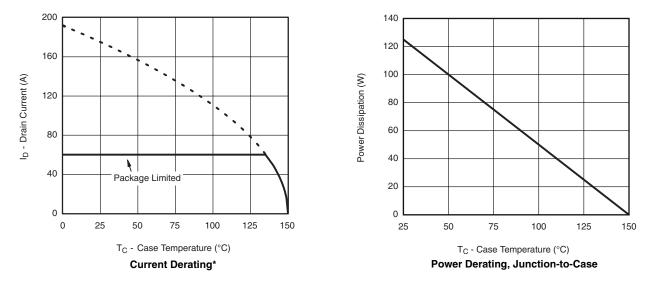
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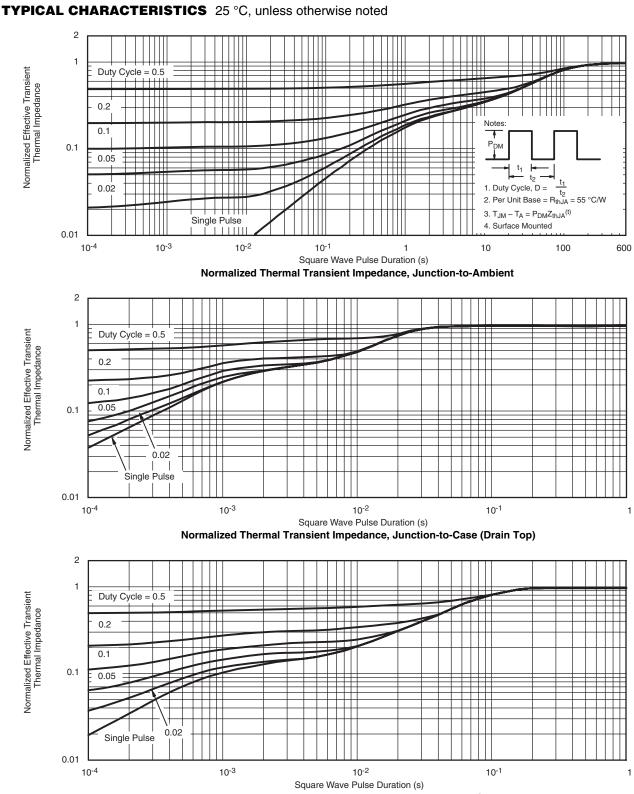
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



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Normalized Thermal Transient Impedance, Junction-to-Source

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68626.

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