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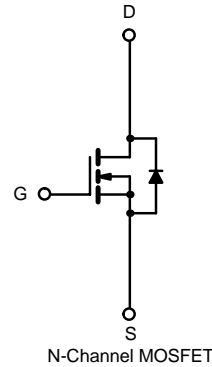
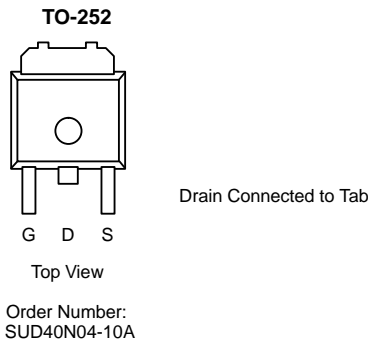
New Product

**SUD40N04-10A**  
Vishay Siliconix

**N-Channel 40-V (D-S), 175 °C MOSFET**

PRODUCT SUMMARY		
V <sub>(BR)DSS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>
40	0.010 @ V <sub>GS</sub> = 10 V	40
	0.014 @ V <sub>GS</sub> = 4.5 V	40

**175 °C Rated**  
Maximum Junction Temperature



ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V <sub>DS</sub>	40	V
Gate-Source Voltage		V <sub>GS</sub>	±20	
Continuous Drain Current (T <sub>J</sub> = 175 °C)	T <sub>C</sub> = 25 °C	I <sub>D</sub>	40 <sup>a</sup>	A
	T <sub>C</sub> = 100 °C		40 <sup>a</sup>	
Pulsed Drain Current		I <sub>DM</sub>	100	
Avalanche Current		I <sub>AR</sub>	30	
Repetitive Avalanche Energy <sup>b</sup>	L = 0.1 mH	E <sub>AR</sub>	45	mJ
Power Dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	71 <sup>c</sup>	W
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to 175	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient <sup>d</sup>	t ≤ 10 sec.	R <sub>thJA</sub>	15	18	°C/W
	Steady State		40	50	
Junction-to-Case		R <sub>thJC</sub>	1.75	2.1	

- Notes:
- Package limited.
  - Duty cycle ≤ 1%.
  - See SOA curve for voltage derating.
  - Surface mounted on 1" FR4 board.



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SPECIFICATIONS (T <sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	40			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>DS</sub> = 250 μA	1		3	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 32 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 32 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			50	
		V <sub>DS</sub> = 32 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C			150	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	40			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 40 A		0.0075	0.010	Ω
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 40 A, T <sub>J</sub> = 125 °C		0.012	0.016	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 40 A, T <sub>J</sub> = 175 °C		0.015	0.020	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A		0.011	0.014	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A, T <sub>J</sub> = 125 °C		0.018	0.022	
V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A, T <sub>J</sub> = 175 °C		0.022	0.028			
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 40 A	20	40		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	C <sub>iSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz		1700		pF
Output Capacitance	C <sub>oSS</sub>			370		
Reverse Transfer Capacitance	C <sub>rSS</sub>			145		
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 40 A		35		nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			6		
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			8		
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 20 V, R <sub>L</sub> = 0.5 Ω I <sub>D</sub> = 40 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 2.5 Ω		14	30	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			7.5	15	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			30	60	
Fall Time <sup>c</sup>	t <sub>f</sub>			14	30	
<b>Source-Drain Ciode Ratings and Characteristics (T<sub>C</sub> = 25 °C)<sup>b</sup></b>						
Continuous Current	I <sub>S</sub>				40	A
Pulsed Current	I <sub>SM</sub>				100	
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = 40 A, V <sub>GS</sub> = 0 V		1.0	1.50	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 40 A, di/dt = 100 A/μs		30	60	ns

Notes:

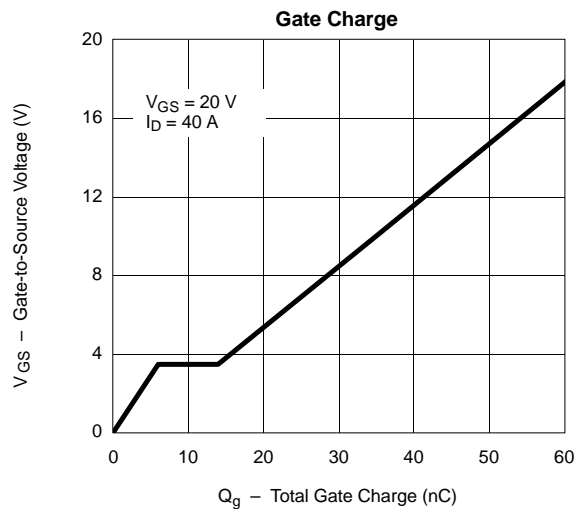
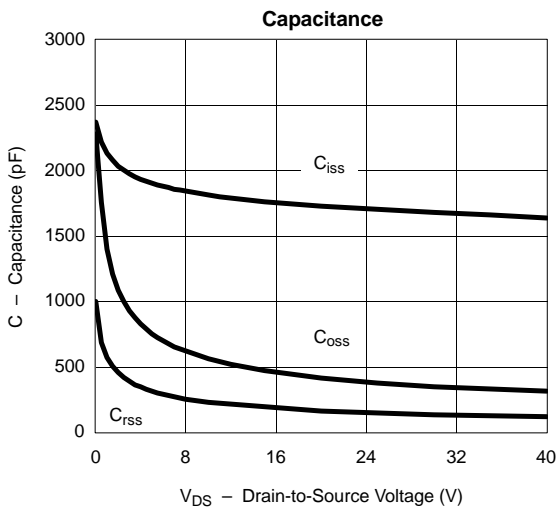
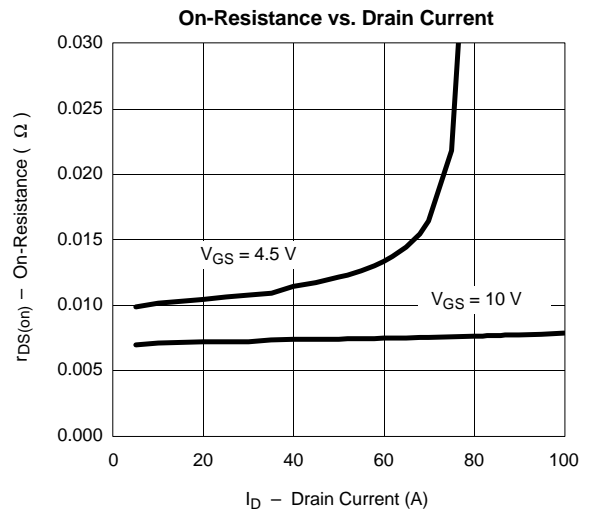
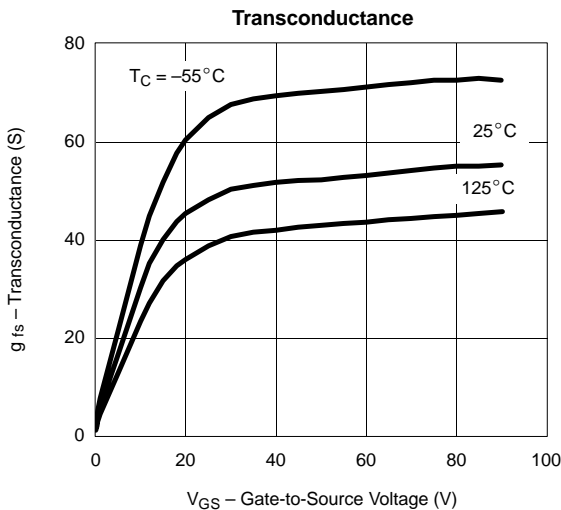
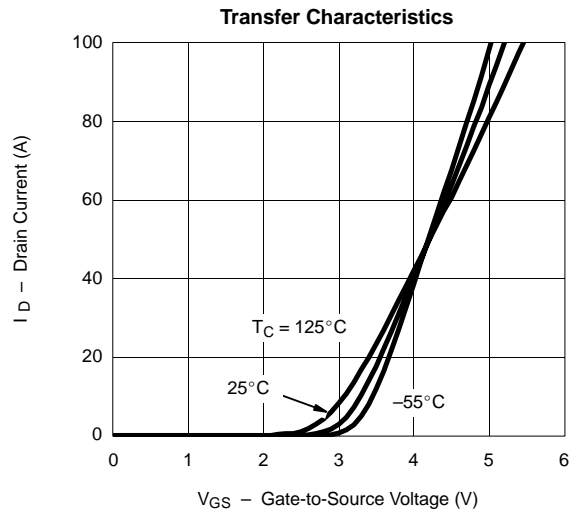
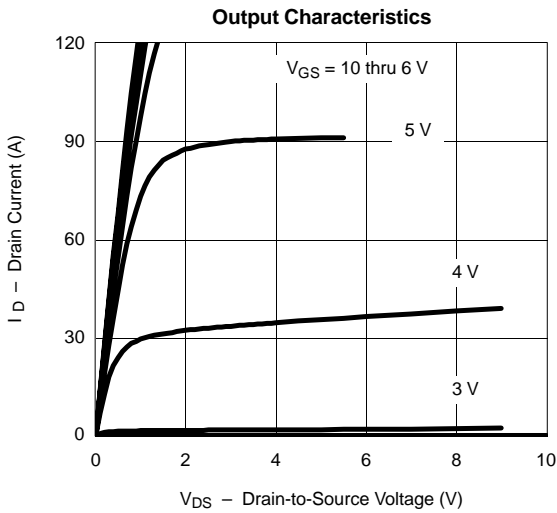
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.



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**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**



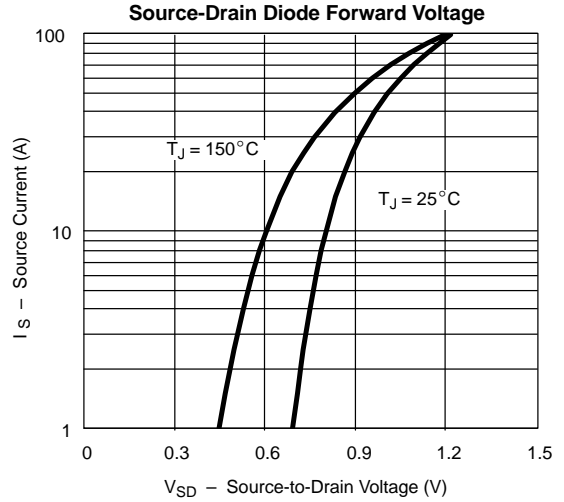
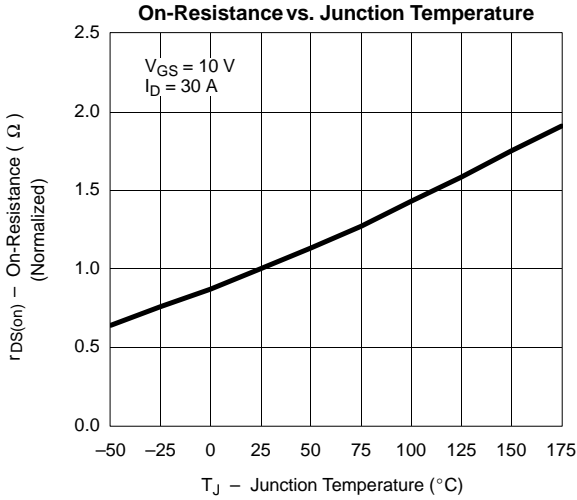


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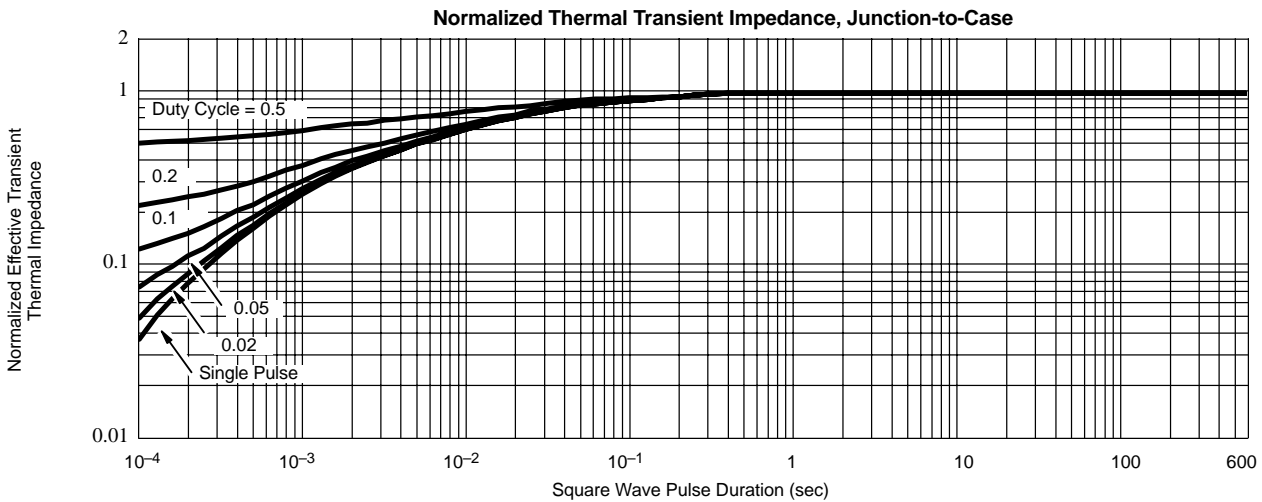
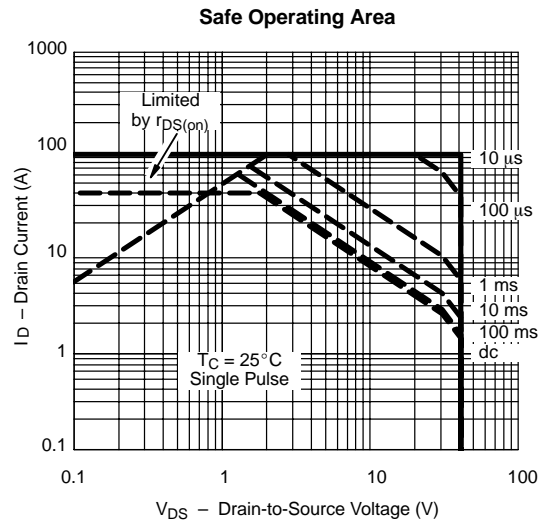
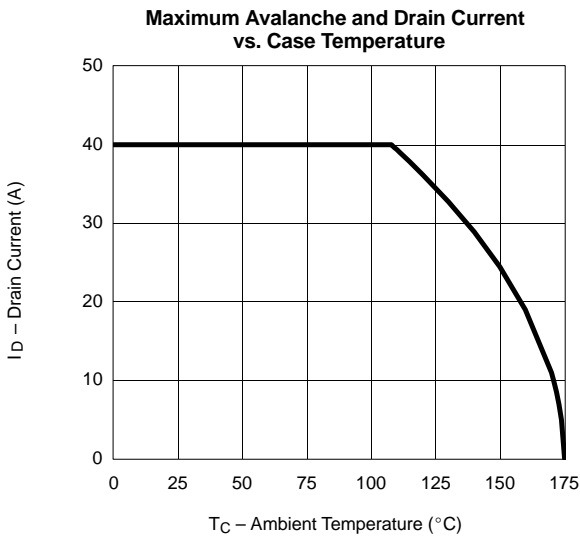
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## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



## THERMAL RATINGS





## Legal Disclaimer Notice

Vishay

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