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STMicroelectronics
ESDAVLC8-1BU2

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ESDAVLC8-1BU2

Single-line low capacitance Transil™, transient surge voltage suppressor (TVS) for bidirectional ESD protection

Datasheet – production data

Features

- Bidirectional device
- Withstands multiple ESD strikes
- Very low diode capacitance: 5 pF typ. at 0 V
- Low leakage current
- 0201 SMD package size compatible
- Ultra small PCB area: 0.18 mm^2
- RoHS compliant

Benefits

- High ESD protection level
- High integration
- Suitable for high density boards
- MSL1

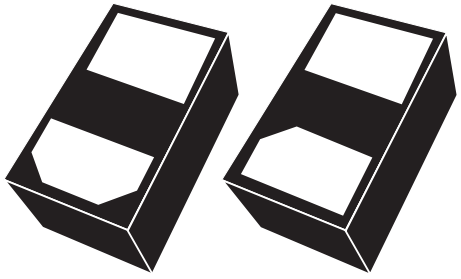
Complies with the following standards:

- IEC 61000-4-2 level 4
  - 15 kV (air discharge)
  - 8 kV (contact discharge)

Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

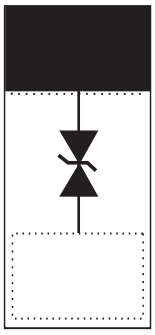
- Portable multimedia players and accessories
- Notebooks
- Digital cameras and camcorders
- Communication systems
- Cellular phone handsets and accessories



Pin 2 available in different forms

ST0201 package

Figure 1. Functional diagram (top view)



Description

The ESDAVLC8-1BU2 is a bidirectional single line TVS diode designed to protect the data lines or other I/O ports against ESD transients.

The device is ideal for applications where both reduced line capacitance and board space saving are required.

TM: Transil is a trademark of STMicroelectronics

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter	Value	Unit
V_{PP}	Peak pulse voltage: IEC 61000-4-2 contact discharge EC 61000-4-2 air discharge	 ± 15 ± 16	kV
I_{PP}	Peak pulse current (8/20 µs)	1.5	A
T_j	Junction temperature	125	°C
T_{stg}	Storage temperature range	- 55 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s	260	°C
T_{op}	Operating junction temperature range	-40 to +125	°C

Figure 2. Electrical characteristics (definitions)

Symbol		Parameter
V_{BR}	=	Breakdown voltage
V_{CL}	=	Clamping voltage
I_{RM}	=	Leakage current @ V_{RM}
V_{RM}	=	Stand-off voltage
I_F	=	Forward current
I_{PP}	=	Peak pulse current
I_R	=	Breakdown current
V_F	=	Forward voltage drop
R_d	=	Dynamic impedance
aT	=	Voltage temperature

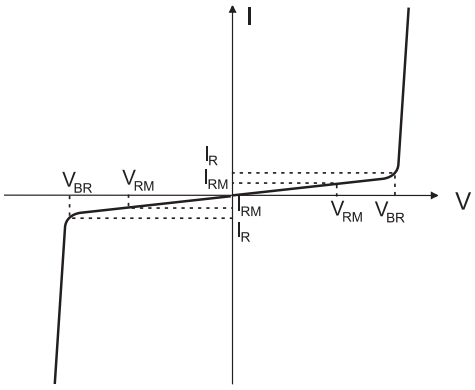


Table 2. Electrical characteristics (values, T_{amb} = 25 °C)

Symbol	Test Condition	Min.	Typ.	Max.	Unit
V_{BR}	From pin1 to pin 2, I_R = 1 mA	8.5	11		V
	From pin 2 to pin1, I_R = 1 mA	14.5	17		
I_{RM}	V_{RM} = 3 V			100	nA
R_d	Square pulse, I_{PP} = 1 A t_p = 2.5 µs		2.5		Ω
αT	$\Delta V_{BR} = \alpha T(T_{amb}$ - 25 °C) x V_{BR} (25 °C)			6	10^{-4}/°C
C_{line}	V_R = 0 V, F_{osc} = 1 MHz, V_{osc} = 30 mV		5	7	pF

Figure 3. Relative variation of peak pulse power versus initial junction temperature

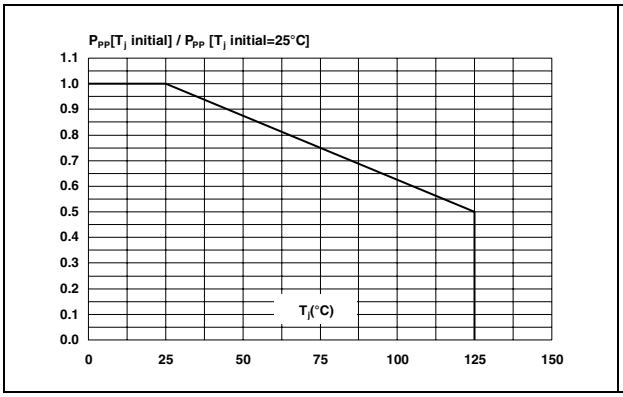


Figure 4. Peak pulse power versus exponential pulse duration

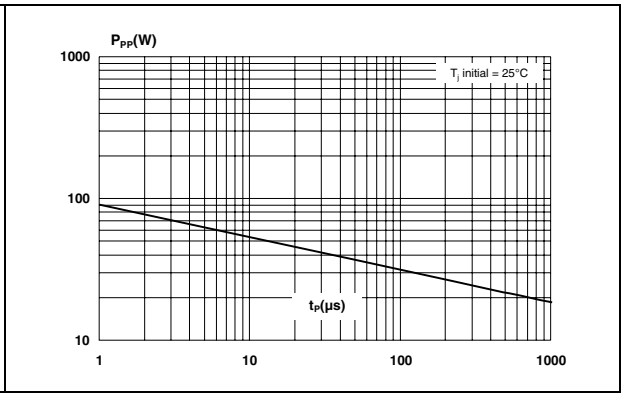


Figure 5. Junction capacitance versus reverse applied voltage (typical values)

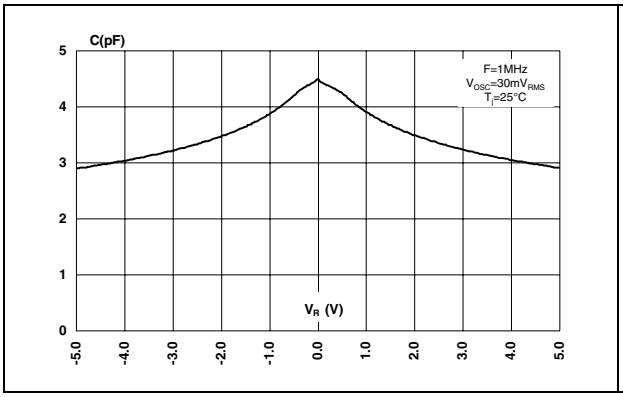


Figure 6. Relative variation of leakage current versus junction temperature (typical values)

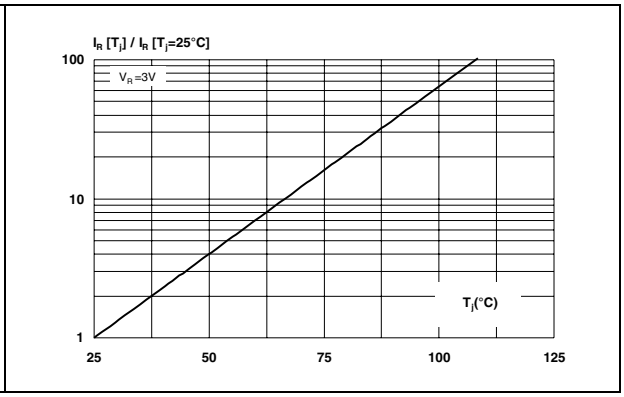


Figure 7. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

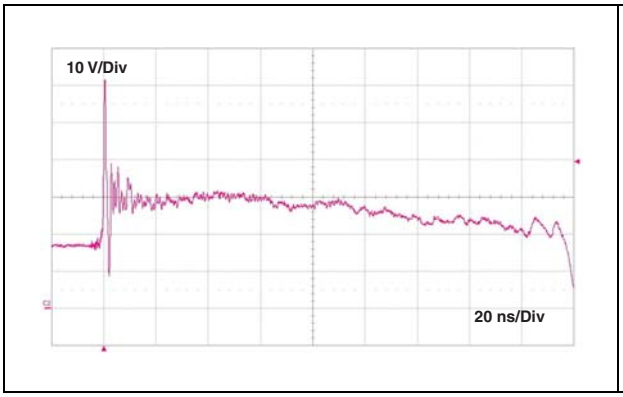


Figure 8. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

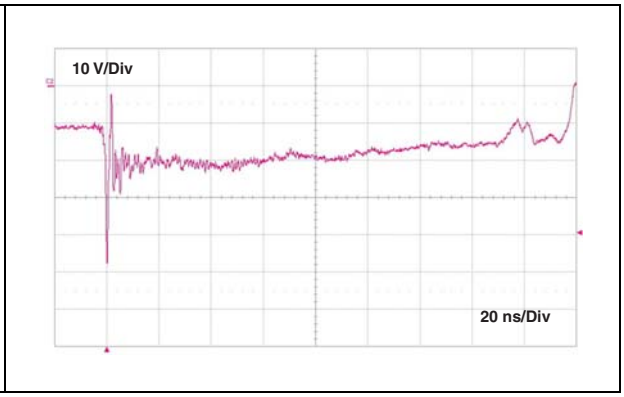


Figure 9. S21 attenuation measurement results

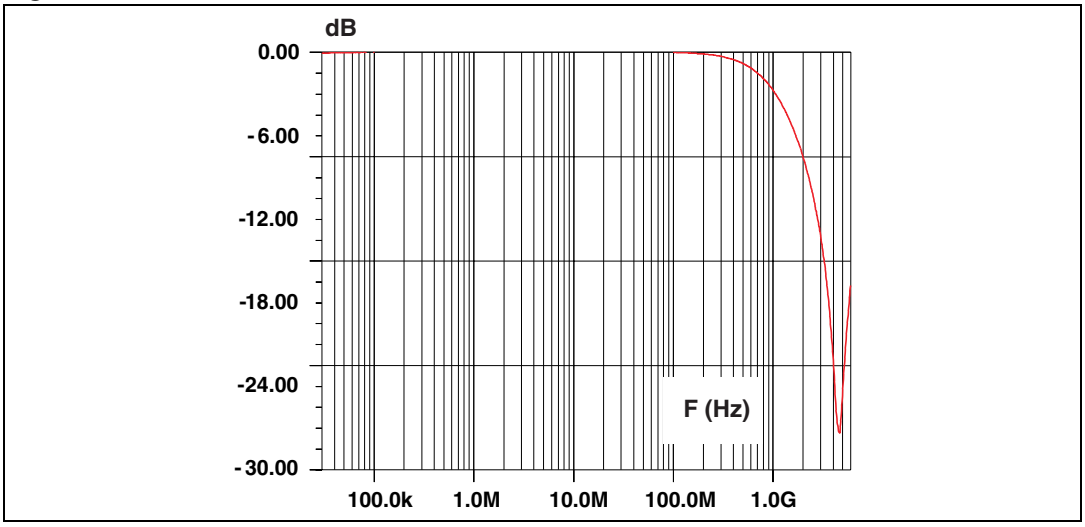
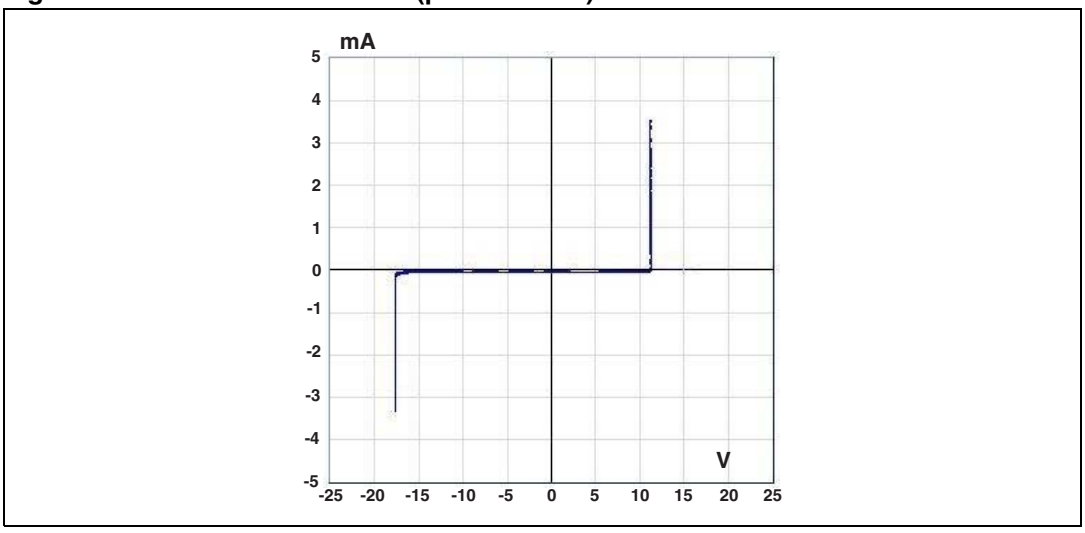
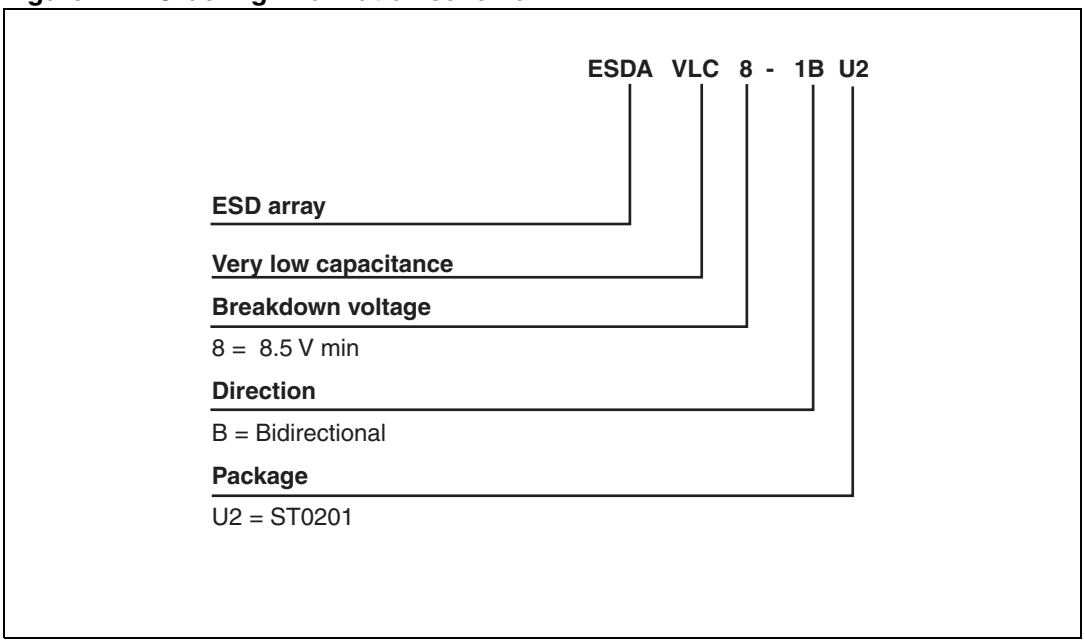


Figure 10. Static characteristic (pin 2 to GND)



2 Ordering information scheme

Figure 11. Ordering information scheme

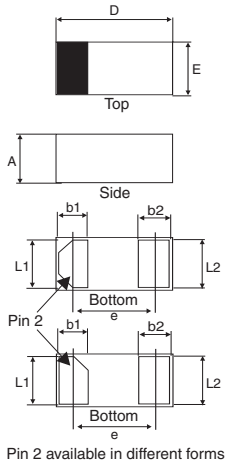


3 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 3. ST0201 dimensions



Pin 2 available in different forms

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.23	0.28	0.33	0.009	0.011	0.013
b1	0.13	0.18	0.23	0.005	0.007	0.009
b2	0.14	0.19	0.24	0.006	0.007	0.009
D	0.55	0.60	0.65	0.022	0.024	0.026
E	0.25	0.30	0.35	0.010	0.012	0.014
e	-	0.35	-	-	0.014	-
L1	0.20	0.25	0.30	0.008	0.010	0.012
L2	0.20	0.25	0.30	0.008	0.010	0.012

Figure 12. Footprint (dimensions in mm)

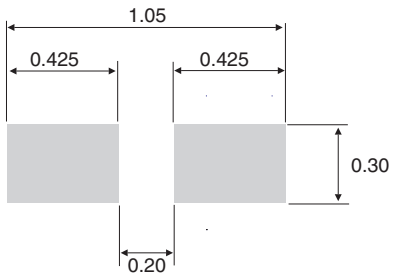
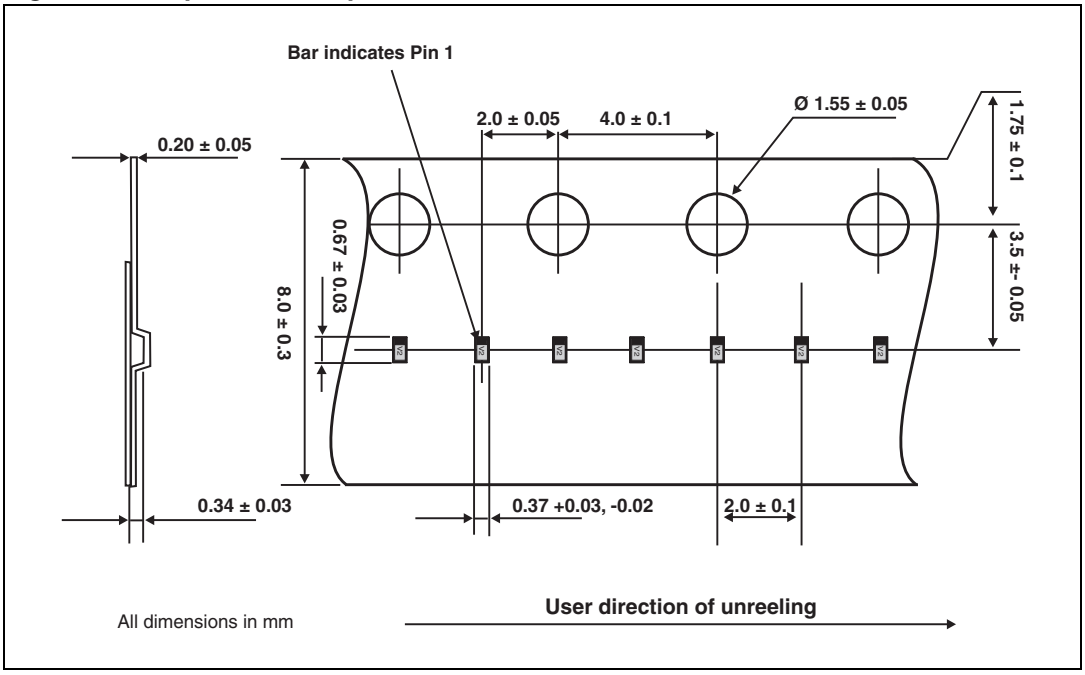


Figure 13. Marking

Note: Product marking may be rotated by multiples of 180° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

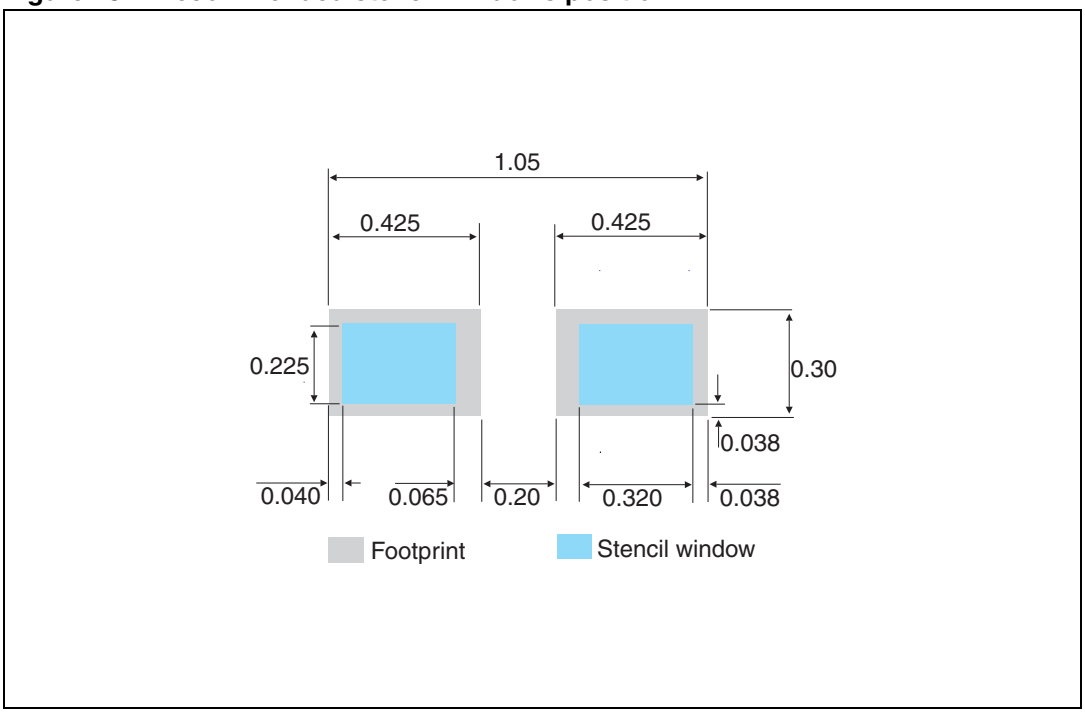
Figure 14. Tape and reel specifications



4 Recommendation on PCB assembly

4.1 Stencil opening design

Figure 15. Recommended stencil windows position



4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed
4. Solder paste with fine particles: powder particle size is 20-45 µm.

4.3 Placement

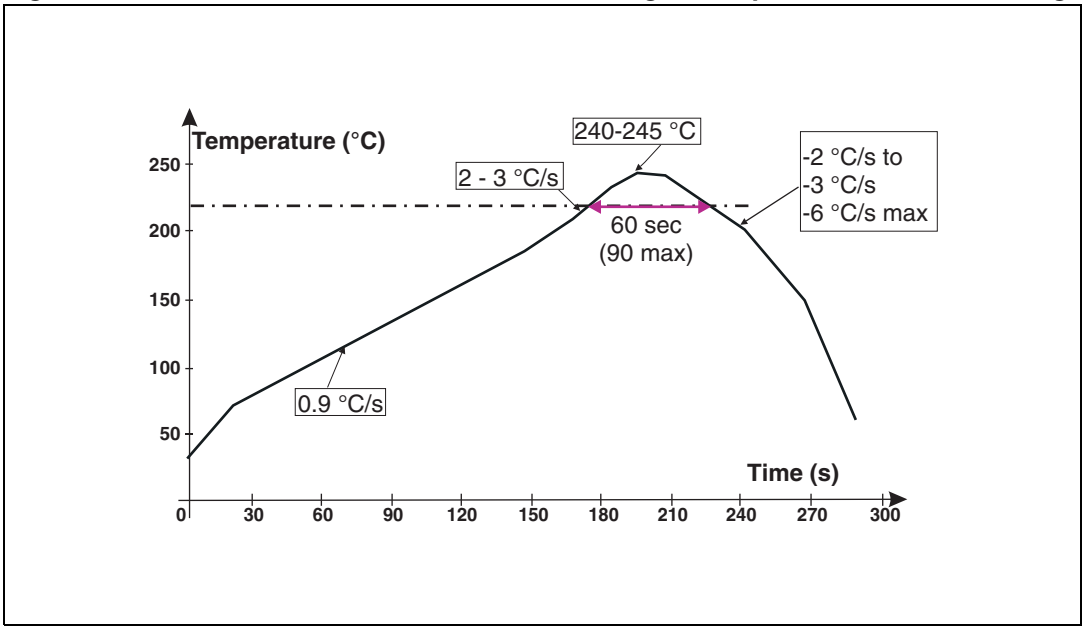
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile

Figure 16. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

5 Ordering information

Table 4. Ordering information

Order code	Marking	Weight	Base qty	Delivery mode
ESDAVLC8-1BU2	V2(1)	0.124 mg	15000	Tape and reel

1. The marking can be rotated by multiples of 180° to differentiate assembly location

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
03-Mar-2011	1	Initial release.
15-May-2012	2	Updated *Figure 10* for flow polarity. Updated graphic in *Table 3* for pin 2 form. Updated note under *Figure 13* and *Table 4* for marking rotation. Updated *Figure 16* for recommended soldering reflow. Updated marking in *Table 4*.

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