NANOPOWER 1.8-V COMPARATOR WITH VOLTAGE REFERENCE

Check for Samples: TLV3012A-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Low Quiescent Current = 5 μA (Max)**
- **Integrated Voltage Reference = 1.242 V**
- **Input Common-Mode Range = 200 mV Beyond Rails**
- **Voltage Reference Initial Accuracy = 1%**
- **Open-Drain Logic Compatible Output (TLV3011-Q1)**
- **Push-Pull Output (TLV3012A-Q1)**
- **Low Supply Voltage = 1.8 V to 5.5 V**
- **Fast Response Time = 6-μs Propagation Delay With 100-mV Overdrive (TLV3011-Q1: $R_{PULL-UP}$ = 10 kΩ)**

APPLICATIONS

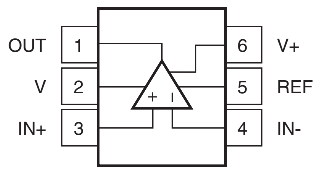
- **Battery-Powered Level Detection**
- **Data Acquisition**
- **System Monitoring**
- **Oscillators**

DESCRIPTION

The TLV3011-Q1 is a low-power, open-drain output comparator. The TLV3012A-Q1 is a push-pull output comparator. Both feature an uncommitted on-chip voltage reference, have 5-μA (max) quiescent current, input common-mode range 200 mV beyond the supply rails, and single-supply operation from 1.8 V to 5.5 V. The integrated 1.242-V series voltage reference offers low 100-ppm/°C (max) drift, is stable with up to 10-nF capacitive load, and can provide up to 0.5 mA (typ) of output current.

The TLV3012A-Q1 is available in the SC-70 package. The devices are specified for the temperature range of –40°C to 125°C.

DCK PACKAGE
(TOP VIEW)



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE ORDERING INFORMATION

Table 1.

T_A	PACKAGE(1)	ORDERABLE PART NUMBER	TOP SIDE MARKING
-40°C TO 125°C	SOT (SC-70), DCK	TLV3011AQDCKRQ1(2)	TBD
	SOT (SC-70), DCK	TLV3012AQDCKRQ1	BPF

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) Product preview device.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

			MIN	MAX	UNIT
	Supply voltage			7	V
	Signal input terminals	Voltage(2)	–0.5	(V+) +0.5	V
		Current(2)		±10	mA
	Output short circuit(3)			Continous	
	Operating temperature range		–40	125	°C
T_{stg}	Storage temperature range		–65	150	°C
T_J	Junction temperature			150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.
(3) Short circuit to ground

ELECTRICAL CHARACTERISTICS: V_S = +1.8 V to +5.5 V

Boldface limits apply over the specified temperature range, T_A = –40°C to +125°C.
At T_A = +25°C, V_{OUT} = V_S, unless otherwise noted; for TLV3011-Q1, $R_{PULL-UP}$ = 10 kΩ connected to V_S.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Offset Voltage							
V_{OS}	Input offset voltage		V_{CM} = 0 V, I_O = 0 V		0.5	15	mV
dV_{OS}/dT	**Input offset voltage vs temperature**		**T_A = –40°C to 125°C**		**±12**		**μV/°C**
PSRR	Power supply rejection ratio		V_S = 1.8 V to 5.5 V		100	1000	μV/V
Input Bias Current							
I_B	Input bias current		V_{CM} = V_S/2		±10		pA
I_{OS}	Input offset current		V_{CM} = V_S/2		±10		pA
Input Voltage Range							
V_{CM}	Common-mode voltage range			(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio		V_{CM} = –0.2 V to (V+) – 1.5 V	60	74		dB
			V_{CM} = –0.2 V to (V+) + 0.2 V	54	62		
Input Impedance							
	Common mode				10^{13} ∥ 2		Ω ∥ pF
	Differential				10^{13} ∥ 4		Ω ∥ pF
Switching Characteristics							
	Propagation delay time	Low to high	f = 10 kHz, V_{STEP} = 1 V, input overdrive = 10 mV		12		μs
			f = 10 kHz, V_{STEP} = 1 V, input overdrive = 100 mV		6		
		High to low	f = 10 kHz, V_{STEP} = 1 V, input overdrive = 10 mV		13.5		
			f = 10 kHz, V_{STEP} = 1 V, input overdrive = 100 mV		6.5		
t_r	Rise time	TLV3011-Q1 (1)			See (2)		
		TLV3012A-Q1	C_L = 10 pF		100		ns
t_f	Fall time		C_L = 10 pF		100		ns
Output							
V_{OL}	Voltage output low from rail		V_S = 5 V, I_{OUT} = –5 mA		160	200	mV
	Voltage output high from rail	TLV3012A-Q1	V_S = 5 V, I_{OUT} = 5 mA		90	200	mV
	Short-circuit current	TLV3012A-Q1			See Typical Characteristics		
Voltage Reference							
V_{OUT}	Output voltage			1.208	1.242	1.276	V
	Initial accuracy					±1%	
dV_{OUT}/d_T	Temperature drift		–40°C ≤ T_A ≤ 125°C		40	100	ppm/°C
dV_{OUT}/dI_{LOAD}	Load regulation	Sourcing	0 mA < I_{SOURCE} ≤ 0.5 mA		0.36	1	mV/mA
		Sinking	0 mA < I_{SINK} ≤ 0.5 mA		6.6		
I_{LOAD}	Output current				0.5		mA
dV_{OUT}/dV_{IN}	Line regulation		1.8 V ≤ V_{IN} ≤ 5.5 V		10	100	μV/V
Noise							
	Reference voltage noise		f = 0.1 Hz to 10 Hz		0.2		mV_{PP}
Power Supply							
V_S	Specified voltage			1.8		5.5	V
	Operating voltage range			1.8		5.5	V
I_Q	Quiescent current		V_S = 5 V, V_O = High		2.8	5	μA
Temperature							
	Operating range			–40		125	°C
	Storage range			–65		150	°C
	Thermal resistance	DCK package			259		°C/W

(1) Product preview device.
(2) t_r depends on $R_{PULL-UP}$ and C_{LOAD}.

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +1.8 V to +5.5 V, $R_{PULL-UP}$ = 10 kΩ, and Input Overdrive = 100 mV, unless otherwise noted.

QUIESCENT CURRENT vs TEMPERATURE

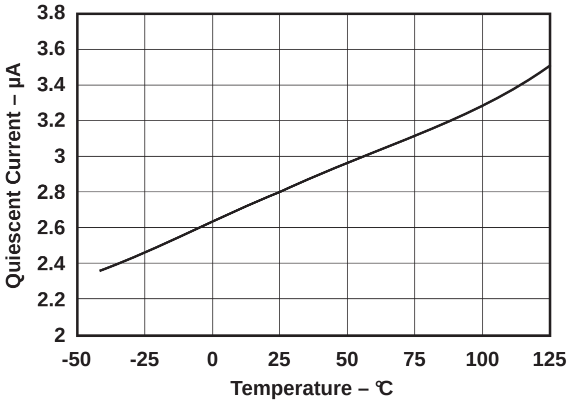


Figure 1.

QUIESCENT CURRENT vs OUTPUT SWITCHING FREQUENCY

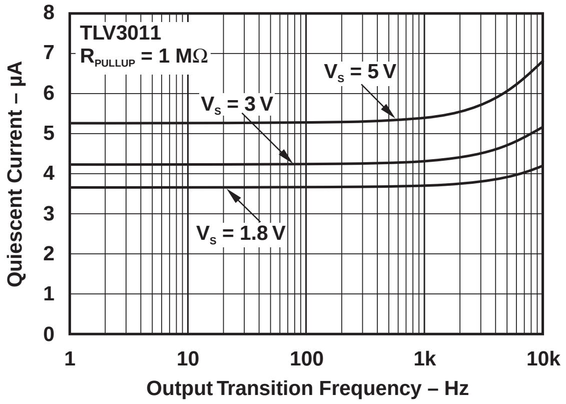


Figure 2.

QUIESCENT CURRENT vs OUTPUT SWITCHING FREQUENCY

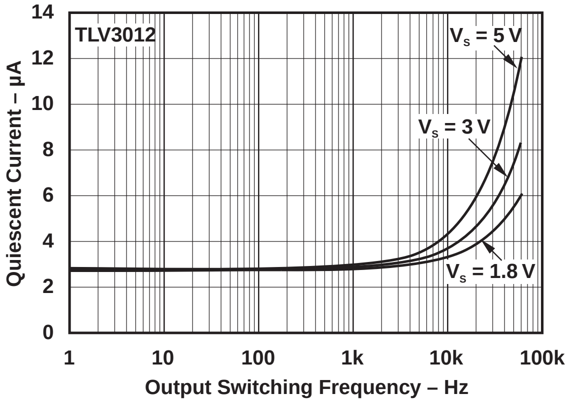


Figure 3.

INPUT BIAS CURRENT vs TEMPERATURE

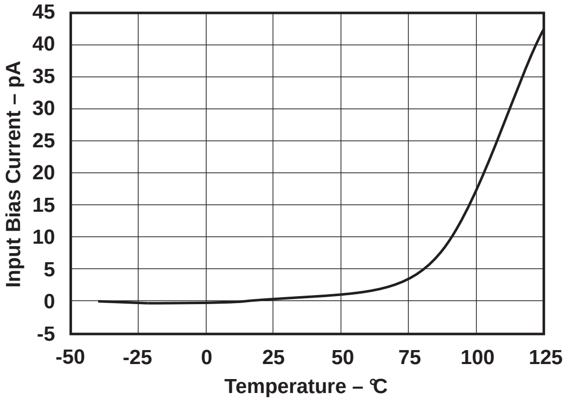


Figure 4.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +1.8 V to +5.5 V, $R_{PULL-UP}$ = 10 kΩ, and Input Overdrive = 100 mV, unless otherwise noted.

OUTPUT LOW vs OUTPUT CURRENT

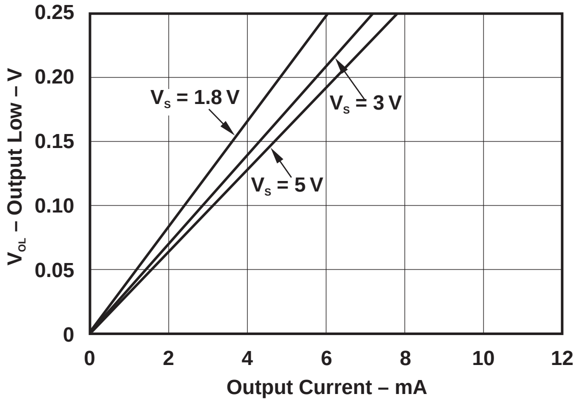


Figure 5.

OUTPUT HIGH vs OUTPUT CURRENT

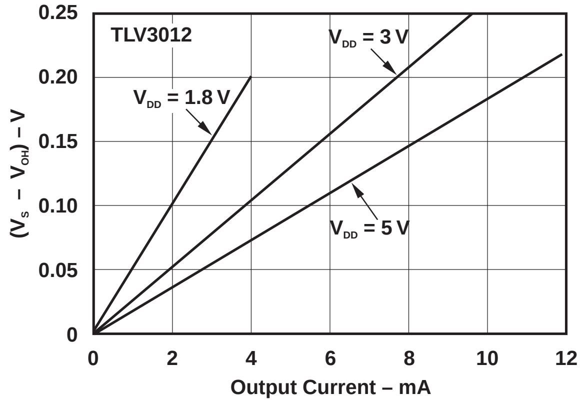


Figure 6.

PROPAGATION DELAY (t_{PLH}) vs CAPACITIVE LOAD

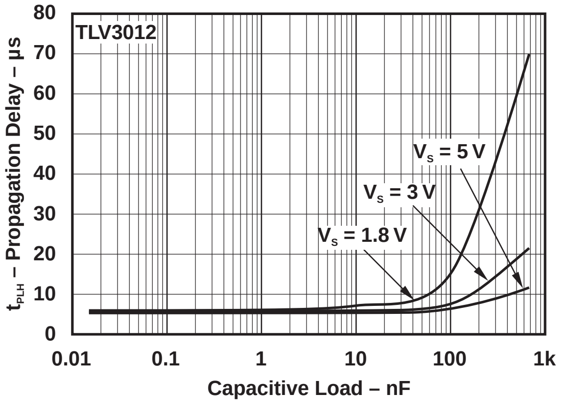


Figure 7.

PROPAGATION DELAY (t_{PHL}) vs CAPACITIVE LOAD

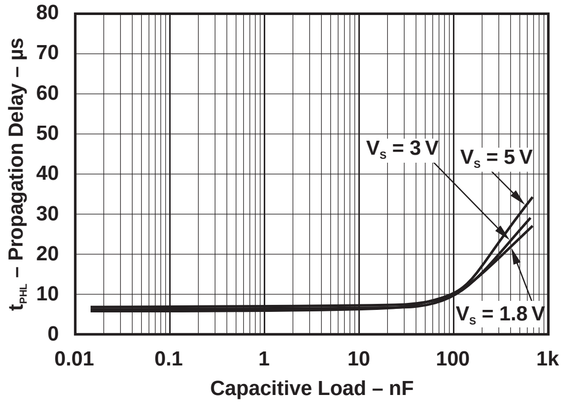


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +1.8 V to +5.5 V, $R_{PULL\text{-}UP}$ = 10 kΩ, and Input Overdrive = 100 mV, unless otherwise noted.

PROPAGATION DELAY (t_{PLH}) vs INPUT OVERDRIVE

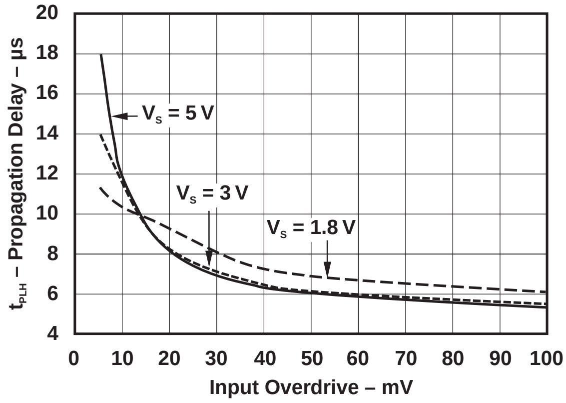


Figure 9.

PROPAGATION DELAY (t_{PHL}) vs INPUT OVERDRIVE

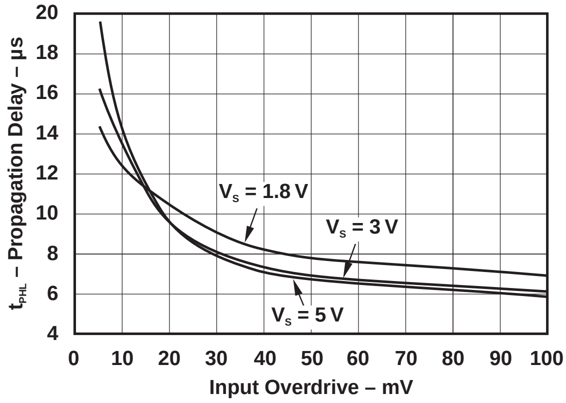


Figure 10.

PROPAGATION DELAY (t_{PLH}) vs TEMPERATURE

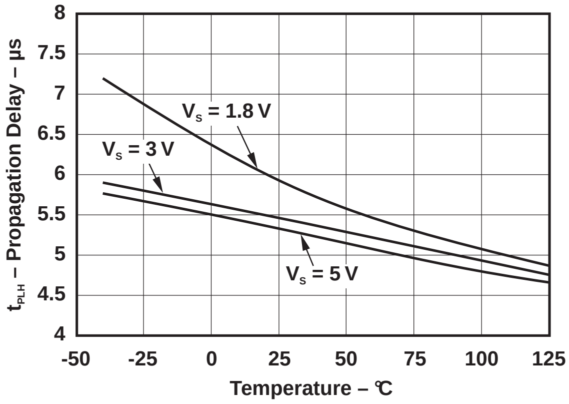


Figure 11.

PROPAGATION DELAY (t_{PHL}) vs TEMPERATURE

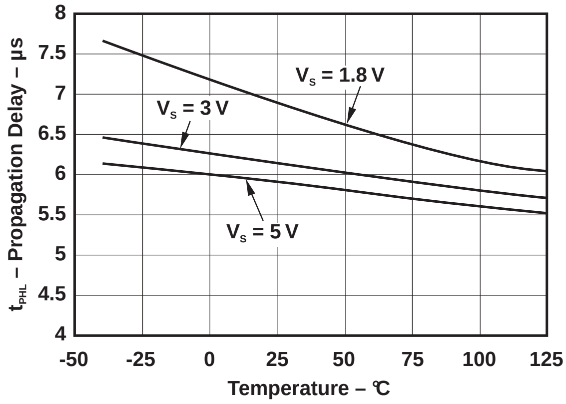


Figure 12.

PROPAGATION DELAY (t_{PLH})

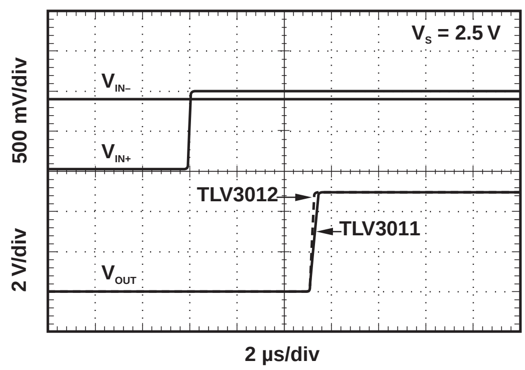


Figure 13.

PROPAGATION DELAY (t_{PHL})

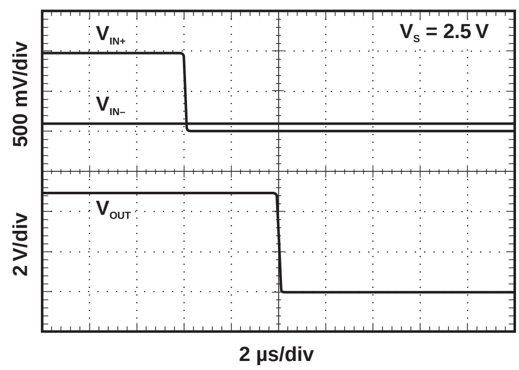


Figure 14.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +1.8 V to +5.5 V, $R_{PULL-UP}$ = 10 kΩ, and Input Overdrive = 100 mV, unless otherwise noted.

PROPAGATION DELAY (t_{PLH})

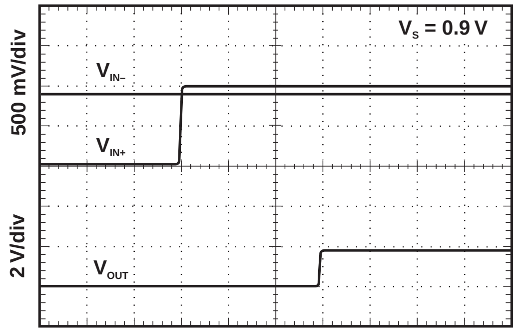


Figure 15.

PROPAGATION DELAY (t_{PHL})

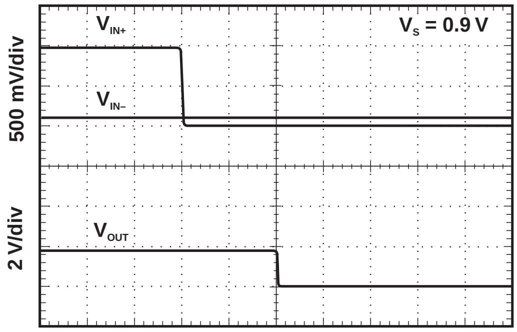


Figure 16.

REFERENCE VOLTAGE
vs
OUTPUT LOAD CURRENT (SOURCING)

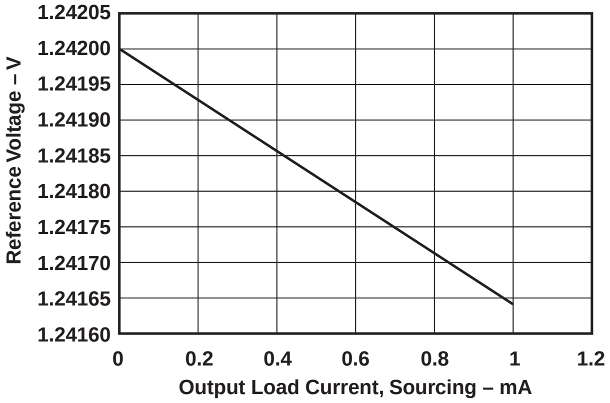


Figure 17.

REFERENCE VOLTAGE
vs
OUTPUT LOAD CURRENT (SINKING)

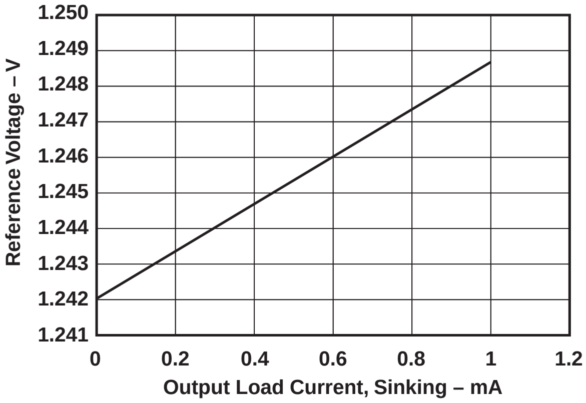


Figure 18.

REFERENCE VOLTAGE
vs
TEMPERATURE

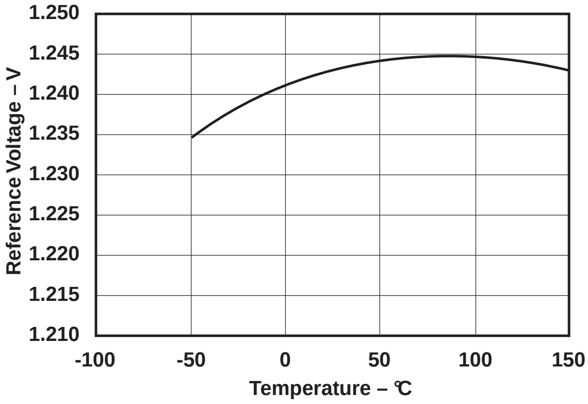


Figure 19.

SHORT-CIRCUIT CURRENT
vs
SUPPLY VOLTAGE

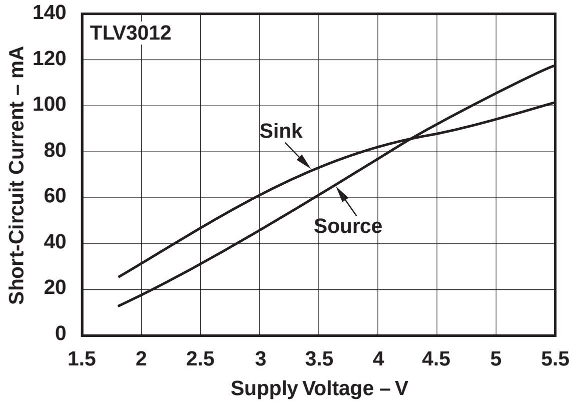


Figure 20.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +1.8 V to +5.5 V, $R_{PULL\text{-}UP}$ = 10 kΩ, and Input Overdrive = 100 mV, unless otherwise noted.

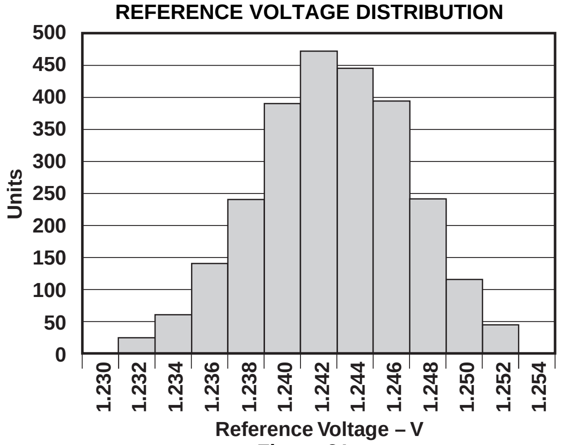


Figure 21.

APPLICATION INFORMATION

The TLV3011-Q1is a low-power, open-drain comparator with on-chip 1.242-V series reference. The open-drain output allows multiple devices to be driven by a single pullup resistor to accomplish an OR function, making the TLV3011-Q1useful for logic applications.

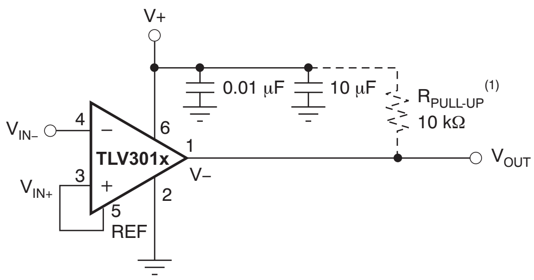
The TLV3012A-Q1 comparator with on-chip 1.242-V series reference has a push-pull output stage optimal for reduced power budget applications and features no shoot-through current.

A typical supply current of 2.8 μA and small packaging combine with 1.8-V supply requirements to make the TLV3011-Q1and TLV3012A-Q1 optimal for battery and portable designs.

Board Layout

Typical connections for the TLV3011-Q1and TLV3012A-Q1 are shown in Figure 22. The TLV3011-Q1is an open-drain output device. A pull-up resistor must be connected between the comparator output and supply to enable operation.

To minimize supply noise, power supplies should be capacitively decoupled by a 0.01-μF ceramic capacitor in parallel with a 1-μF electrolytic capacitor. Comparators are sensitive to input noise and precautions such as proper grounding (use of ground plane), supply bypassing, and guarding of high-impedance nodes minimize the effects of noise and help to ensure specified performance.



(1) Use $R_{PULL-UP}$ with TLV3011-Q1 only.

Figure 22. Basic Connections of the TLV3011-Q1 and TLV3012A-Q1

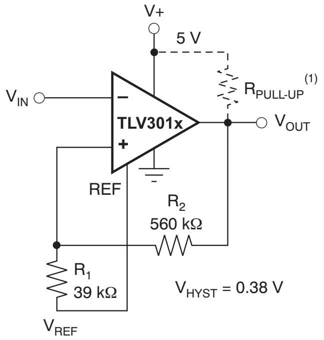
Open-Drain Output (TLV3011-Q1)

The open-drain output of the TLV3011-Q1is useful in logic applications. The value of the pull-up resistor and supply voltage used affects current consumption because of the additional current drawn when the output is in a low state. This effect can be seen in Figure 3.

External Hysteresis

Comparator inputs have no noise immunity within the range of specified offset voltage (±12 mV). For noisy input signals, the comparator output may display multiple switching as input signals move through the switching threshold. The typical comparator threshold of the TLV3011-Q1and TLV3012A-Q1 is ±0.5 mV. To prevent multiple switching within the comparator threshold of the TLV3011-Q1or TLV3012A-Q1, external hysteresis may be added by connecting a small amount of feedback to the positive input. Figure 23 shows a typical topology used to introduce hysteresis, described by this equation:

$$V_{HYST} = \frac{V+ \times R_1}{R_1 + R_2}$$



(1) Use $R_{PULL-UP}$ with TLV3011-Q1 only.

Figure 23. Adding Hysteresis

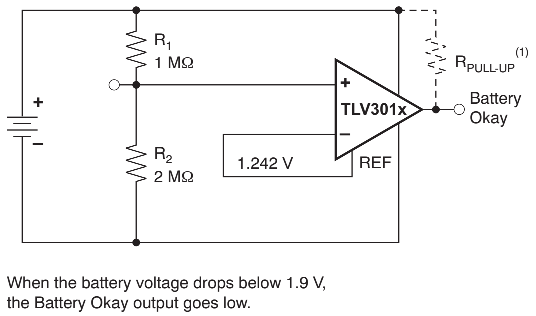
V_{HYST} sets the value of the transition voltage required to switch the comparator output by increasing the threshold region, thereby reducing sensitivity to noise.

Applications

Battery-Level Detect

The low power consumption and 1.8-V supply voltage of the TLV3011-Q1make it an excellent candidate for battery-powered applications. Figure 24 shows the TLV3011-Q1configured as a low battery level detector for a 3-V battery.

$$\text{Battery Okay trip voltage} = 1.242 \frac{R_1 + R_2}{R_2}$$

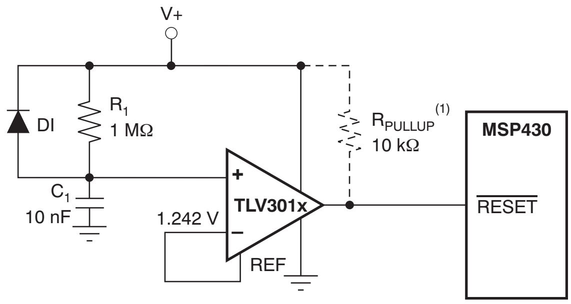


(1) Use $R_{PULL-UP}$ with TLV3011-Q1 only.

Figure 24. TLV3011-Q1 Configured as Low Battery Level Detector

Power-On Reset

The reset circuit shown in Figure 25 provides a time-delayed release of reset to the MSP430 microcontroller. Operation of the circuit is based on a stabilization time constant of the supply voltage, rather than on a predetermined voltage value. The negative input is a reference voltage created by the internal voltage reference. The positive input is an RC circuit that provides a power-up delay. When power is applied, the output of the comparator is low, holding the processor in the reset condition. Only after allowing time for the supply voltage to stabilize does the positive input of the comparator become higher than the negative input, resulting in a high output state, releasing the processor for operation. The stabilization time required for the supply voltage is adjustable by the selection of the RC component values. Use of a lower-valued resistor in this portion of the circuit does not increase current consumption, because no current flows through the RC circuit after the supply has stabilized.



(1) Use $R_{PULL\text{-}UP}$ with TLV3011-Q1 only.

Figure 25. TLV3011-Q1 or TLV3012A-Q1 Configured as Power-Up Reset Circuit for the MSP430

The reset delay needed depends on the power-up characteristics of the system power supply. R_1 and C_1 are selected to allow enough time for the power supply to stabilize. D_1 provides rapid reset if power is lost. In this example, the $R_1 \times C_1$ time constant is 10 ms.

Relaxation Oscillator

The TLV3012A-Q1 can be configured as a relaxation oscillator to provide a simple and inexpensive clock output (see Figure 26). The capacitor is charged at a rate of T = 0.69RC and discharges at a rate of 0.69RC. Therefore, the period is T = 1.38RC. R_1 may be a different value than R_2.

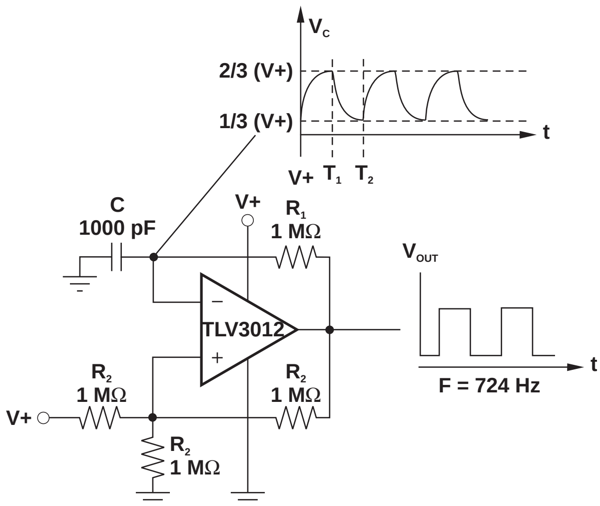


Figure 26. TLV3012A-Q1 Configured as Relaxation Oscillator

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
TLV3012AQDCKRQ1	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV3012-Q1 :

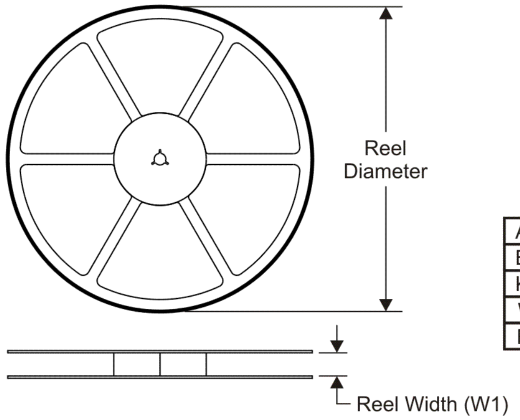
- Catalog: TLV3012

NOTE: Qualified Version Definitions:

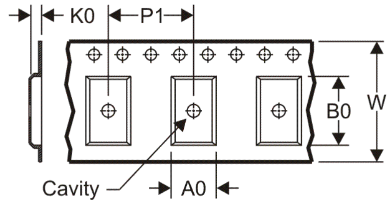
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

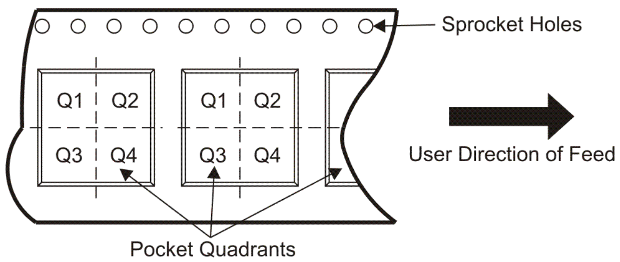


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

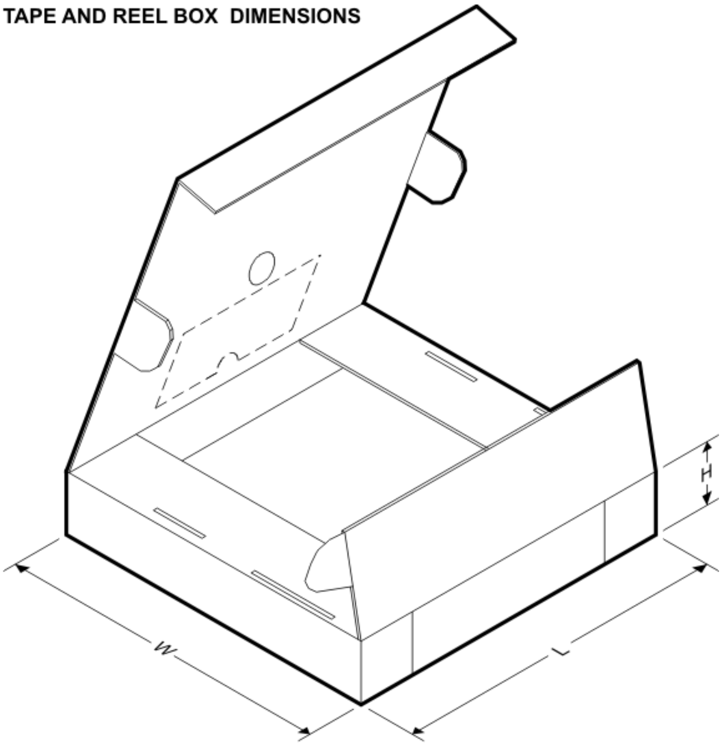


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3012AQDCKRQ1	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3

PACKAGE MATERIALS INFORMATION

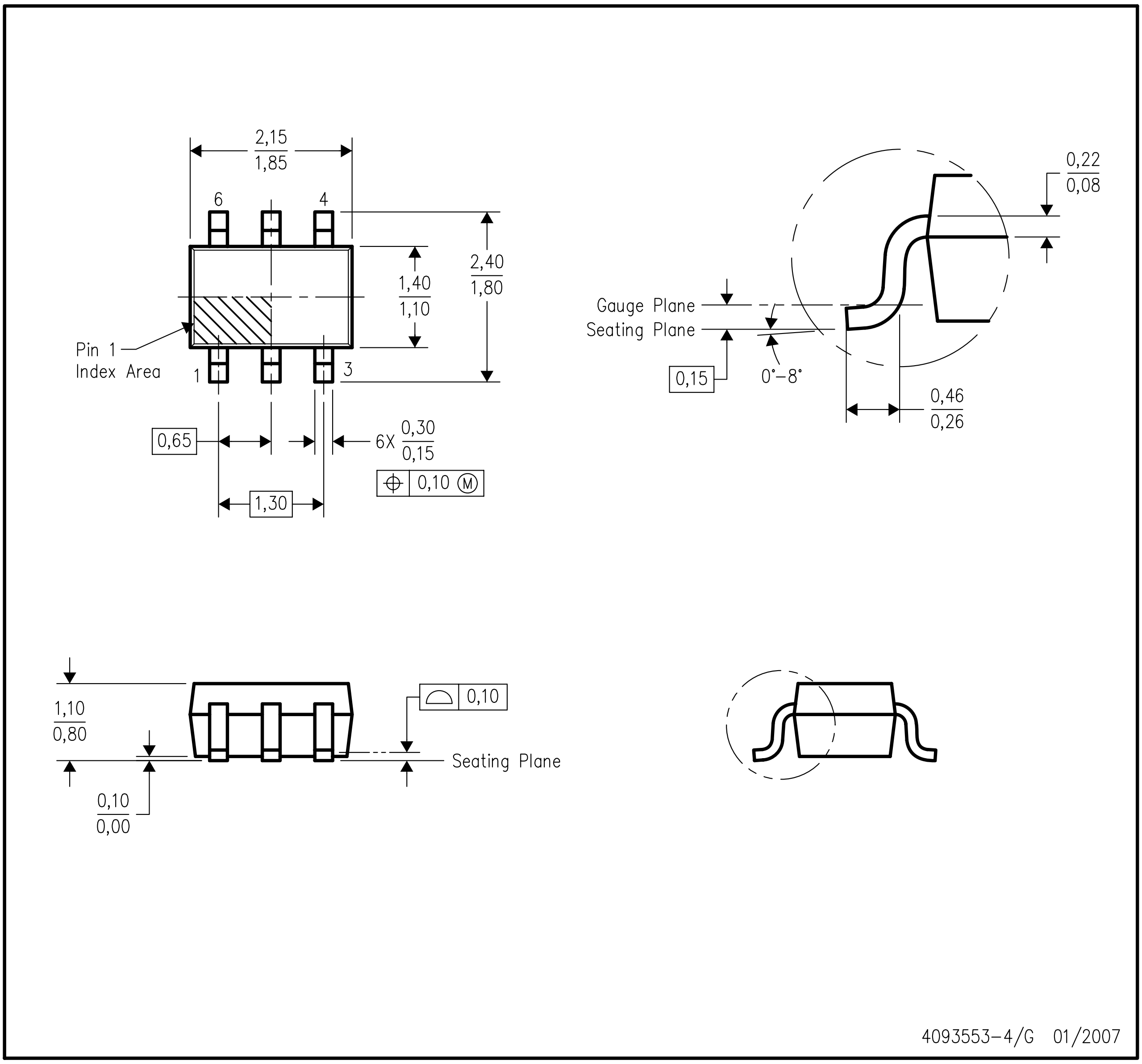
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3012AQDCKRQ1	SC70	DCK	6	3000	203.0	203.0	35.0

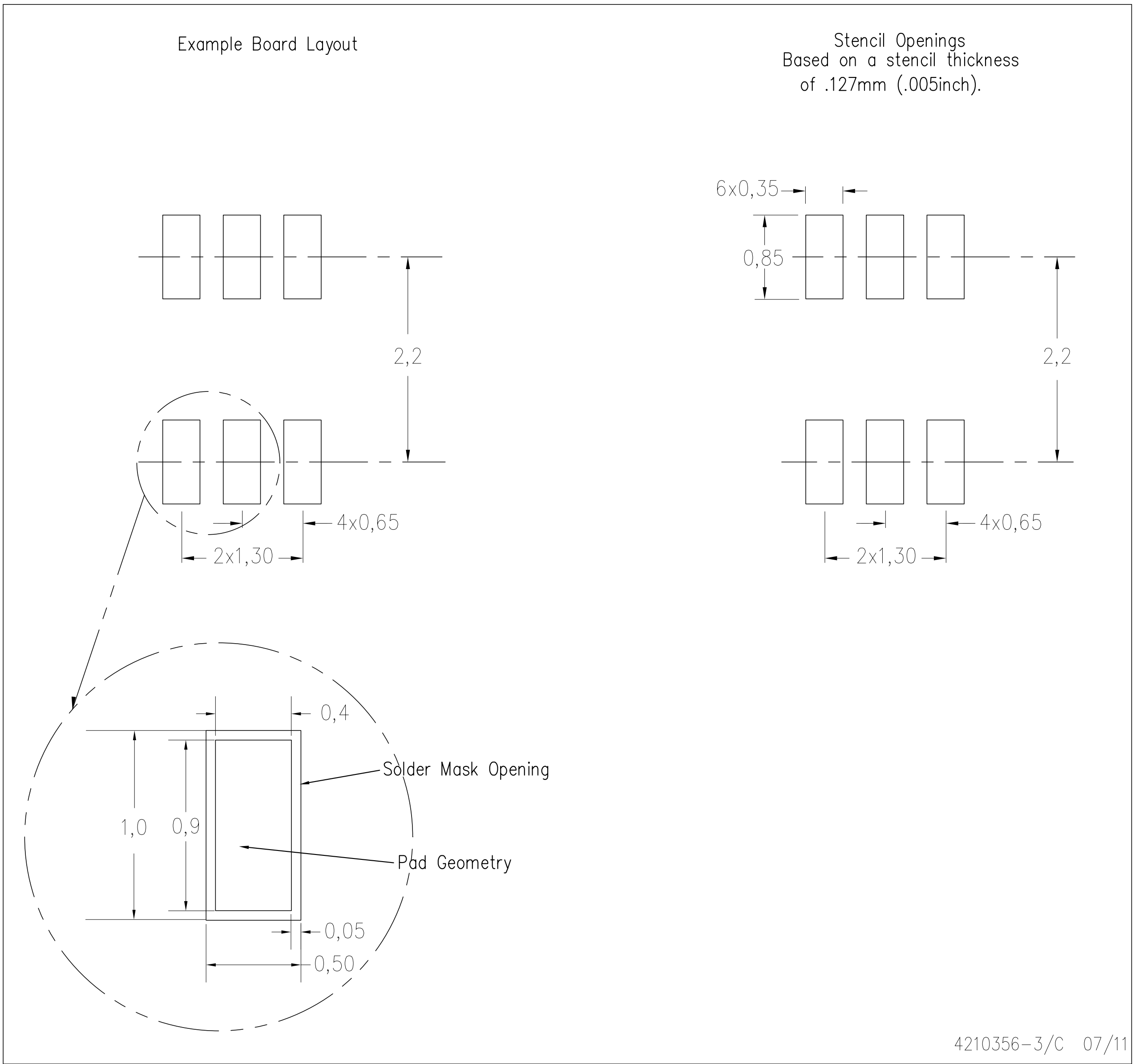
DCK (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AB.

LAND PATTERN DATA

DCK (R-PDSO-G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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