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Texas Instruments
ADS8634SRGET

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12-Bit, 1MSPS, 4-/8-Channel, Bipolar-Input, SAR Analog-to-Digital Converter with Software-Selectable Ranges

Check for Samples: ADS8634, ADS8638

FEATURES

- **Selectable Input Range:**
  ±10V, ±5V, ±2.5V, 0V to 10V, or
  0V to 5V
  Up to ±12V with External Reference
- **No Latent Conversions Up to 1MSPS**
- **Outstanding Performance:**
  12 Bits No Missing Codes
  INL: ±0.9LSB
  SNR: 71.8dB
- **Highly Integrated:**
  4- or 8-Channel Input Mux
  Temperature Sensor
  Internal Voltage Reference
  Alarm Thresholds for Each Channel
- **Low Power:**
  14.45mW at 1MSPS
  5.85mW at 0.1MSPS
  Flexible Power-Down Mode
- **SPI™-Compatible Serial Interface**
- **Extended Temperature Range:**
  –40°C to +125°C
- **Small Footprint: 4mm × 4mm QFN Package**

APPLICATIONS

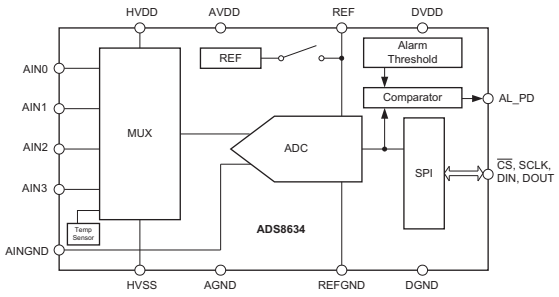
- **Industrial Process Controls (PLC)**
- **Data Acquisition Systems**
- **High-Speed, Closed-Loop Systems**
- **Digital Power Supplies**

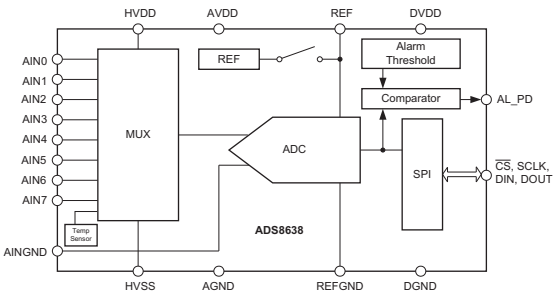
DESCRIPTION

The ADS8634 and ADS8638 (ADS8634/8) are 12-bit analog-to-digital converters (ADCs) capable of measuring inputs up to ±10V at 1MSPS. Using a successive approximation register (SAR) core, these ADCs provide a sample-and-hold front-end with no latency in conversions. The ADS8634 includes an input multiplexer (mux) for measuring up to four inputs. The ADS8638 can measure up to eight inputs.

In addition to the input multiplexer, the ADS8634/8 feature an internal temperature sensor, voltage reference, and a digital comparator for setting alarm thresholds on each input; therefore, a minimal amount of external components are required. A simple SPI-compatible interface provides for communication and control. The digital supply operates from 5V all the way down to 1.8V for direct connection to a wide range of processors and controllers.

Ideal for demanding industrial measurement applications, the ADS8634/8 are fully specified over the extended industrial temperature range of –40°C to +125°C and are available in a small form-factor QFN-24 package.





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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DEVICE COMPARISON(1)

PRODUCT	RESOLUTION	CHANNELS	SAMPLE RATE
ADS8634	12-Bit	4	1MSPS
ADS8638		8	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range, unless otherwise noted.(1)

		VALUE	UNIT
AINn to AGND or AINGND to AGND		HVSS – 0.3 to HVDD + 0.3	V
AVDD to AGND or DVDD to DGND		–0.3 to 7	V
HVDD to AGND		–0.3 to 18	V
HVSS to AGND		–18 to 0.3	V
HVDD to HVSS		–0.3 to 33	V
Digital input voltage to DGND		–0.3 to DVDD + 0.3	V
Digital output to DGND		–0.3 to DVDD + 0.3	V
Operating temperature range		–40 to +125	°C
Storage temperature range		–65 to +150	°C
ESD ratings, all pins	Human body model (HBM)	±2000	V
	Charged device model (CDM)	±500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified in the Electrical Characteristics table is not implied.

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ELECTRICAL CHARACTERISTICS: ADS8634, ADS8638

Minimum/maximum specifications at T_A = –40°C to +125°C, f_{SAMPLE} = 1MSPS, HVDD = 10V to 15V, HVSS = –10V to –15V, AVDD = 4.75V to 5.25V, DVDD = 2.7V to 3.6V, and V_{REF} = 2.5V, unless otherwise noted. Typical specifications at +25°C, f_{SAMPLE} = 1MHz, HVDD = 10V, HVSS = –10V, AVDD = 3.3V, DVDD = 3.3V, and V_{REF} = 2.5V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8634, ADS8638 MIN	TYP	MAX	UNIT
ANALOG INPUT						
Full-scale input span(1)		Bipolar ranges, V_{REF} = 2.5V		±2.5		V
				±5		V
				±10		V
		Unipolar ranges, V_{REF} = 2.5V		0 to 5		V
				0 to 10		V
AINx absolute input range			HVSS		HVDD	V
AINGND absolute input range			–0.2		0.2	V
Input capacitance				8		pF
Input leakage current		At +125°C		200		nA
SYSTEM PERFORMANCE						
Resolution				12		Bits
No missing codes			12			Bits
Integral linearity			–1.5	+0.9/–0.9	1.5	LSB(2)
Differential linearity			–1.0	+0.9/–0.5	1.6	LSB
Offset error(3)			–3	±0.8	3	LSB
Offset error drift				0.75		ppmFS/°C(4)
Gain error(5)			–8	±2	8	LSB
Gain error drift				1.2		ppm/°C
Noise				0.33		LSB
Power-supply rejection		At FFCh output code with 250mV_{PP} and 480Hz ripple on AVDD		–87		dB
Crosstalk	Isolation crosstalk	Crosstalk on channel 0 with channel 0 permanently selected, 2kHz full-scale sine wave on channel 1, all other channels grounded		–110		dB
	Memory crosstalk	Crosstalk on channel 0, 2kHz full-scale sine wave on channel 1, all other channels grounded, device scans channel 0 and channel 1 alternately		–81		dB
SAMPLING DYNAMICS						
Conversion time		At 20MHz SCLK, DVDD = 2.7V to 5.25V			750	ns
Acquisition time		AVDD = 2.7V to 5.25V	250			ns
Maximum throughput rate		At 20MHz SCLK, DVDD = 2.7V to 5.25V		1	1	MSPS
Aperture delay				13		ns
Step response				250		ns

(1) Ideal input span; does not include gain or offset error.
(2) LSB means least significant bit.
(3) Measured relative to an ideal full-scale input.
(4) ppmFS/°C is drift measured in parts per million of full-scale range per degree centigrade.
(5) Does not include reference drift.

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ELECTRICAL CHARACTERISTICS: ADS8634, ADS8638 (continued)

Minimum/maximum specifications at T_A = –40°C to +125°C, f_{SAMPLE} = 1MSPS, HVDD = 10V to 15V, HVSS = –10V to –15V, AVDD = 4.75V to 5.25V, DVDD = 2.7V to 3.6V, and V_{REF} = 2.5V, unless otherwise noted. Typical specifications at +25°C, f_{SAMPLE} = 1MHz, HVDD = 10V, HVSS = –10V, AVDD = 3.3V, DVDD = 3.3V, and V_{REF} = 2.5V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8634, ADS8638			UNIT
			MIN	TYP	MAX	
DYNAMIC CHARACTERISTICS						
Total harmonic distortion(6) (THD)		At 1kHz		–81		dB
		At 100kHz		–80		dB
Signal-to-noise ratio (SNR)		At 1kHz	71	71.8		dB
		At 100kHz		71.1		dB
Signal-to-noise and distortion ratio (SINAD)		At 1kHz	70.1	71.3		dB
		At 100kHz		70.5		dB
Spurious-free dynamic range (SFDR)		At 1kHz		–83		dB
		At 100kHz		–80		dB
Full-power bandwidth		At –3dB		1		MHz
DIGITAL INPUT/OUTPUT						
Logic family				CMOS		V
Logic level	V_{IH}		0.7 DVDD			V
	V_{IL}				0.3 DVDD	V
	V_{OH}	With 20pF load on SDO	0.8 DVDD			V
	V_{OL}	With 20pF load on SDO			0.2 DVDD	V
EXTERNAL VOLTAGE REFERENCE						
Reference input voltage range	V_{REF}		2.0		3.0 or AVDD, whichever is less	V
INTERNAL VOLTAGE REFERENCE						
Reference output voltage				2.5		V
Initial accuracy			–1.2		1.2	%
Temperature drift				20		ppm/°C
Drive current, source(7)					750	µA
Drive current, sink					20	µA
Driver output impedance				1		Ω
Turn-on settling time		With 10µF decoupling capacitor from REF to REFGND		9		ms
INTERNAL TEMPERATURE SENSOR						
Absolute accuracy				5		% of FSR

(6) Calculated on the first nine harmonics of the input frequency.
(7) Internal reference output is short-circuit protected. In case of short-circuit to ground, the drive current is limited to this value.

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ELECTRICAL CHARACTERISTICS: ADS8634, ADS8638 (continued)

Minimum/maximum specifications at T_A = –40°C to +125°C, f_{SAMPLE} = 1MSPS, HVDD = 10V to 15V, HVSS = –10V to –15V, AVDD = 4.75V to 5.25V, DVDD = 2.7V to 3.6V, and V_{REF} = 2.5V, unless otherwise noted. Typical specifications at +25°C, f_{SAMPLE} = 1MHz, HVDD = 10V, HVSS = –10V, AVDD = 3.3V, DVDD = 3.3V, and V_{REF} = 2.5V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8634, ADS8638 MIN	TYP	MAX	UNIT
POWER-SUPPLY REQUIREMENTS						
Supply voltage	V_{AVDD}		2.7	3.3	5.25	V
	V_{DVDD}		1.65	3.3	5.25	V
	V_{HVDD}	10V < V_{HVDD} – V_{HVSS} < 30V	5	10	15	V
	V_{HVSS}	10V < V_{HVDD} – V_{HVSS} < 30V	–15	–10	0	V
AVDD supply current	$I_{AVDD(dynamic)}$	At V_{AVDD} = 2.7V to 3.6V and 1MHz throughput, normal mode with internal reference and temperature sensor off		2.5		mA
		At V_{AVDD} = 4.75V to 5.25V and 1MHz throughput, normal mode with internal reference and temperature sensor off		3.1	3.6	mA
	$I_{AVDD(static)}$	At V_{AVDD} = 2.7V to 3.6V and SCLK off, normal mode with internal reference and temperature sensor off		1.45		mA
		At V_{AVDD} = 4.75V to 5.25V and SCLK off, normal mode with internal reference and temperature sensor off		1.5	1.9	mA
	$I_{AVDD(ref)}$ (8)	At V_{AVDD} = 2.7V to 5.25V, additional AVDD current with internal reference on and temperature sensor off		180		µA
	$I_{AVDD(temp)}$ (9)	At V_{AVDD} = 2.7V to 5.25V, additional AVDD current with internal temperature sensor on and internal reference off		400		µA
HVDD supply current	$I_{HVDD(dynamic)}$	HVDD = 15V and 1MSPS throughput		270	350	µA
	$I_{HVDD(static)}$	HVDD = 15V and device static with SCLK off		5		µA
HVSS supply current	$I_{HVSS(dynamic)}$	HVSS = –15 V and 1MSPS throughput			520	µA
	$I_{HVSS(static)}$	HVSS = –15V and device static with SCLK off		5		µA
DVDD supply current (10)	I_{DVDD}	DVDD = 3.3V, f_{SAMPLE} = 1MSPS, DOUT load = 20pF		2.5		mA
Power-down state	AVDD current	SCLK off, internal reference and temperature sensor off		10		µA
		SCLK on, internal reference and temperature sensor off		160		µA
	HVDD current			5		µA
	HVSS current			5		µA
TEMPERATURE RANGE						
Specified performance			–40		+125	°C

(8) Add $I_{AVDD(ref)}$ to $I_{AVDD(dynamic)}$ or $I_{AVDD(static)}$(as applicable), if internal reference is selected.
(9) Add $I_{AVDD(temp)}$ to $I_{AVDD(dynamic)}$ or $I_{AVDD(static)}$(as applicable), if internal temperature sensor is enabled.
(10) I_{DVDD} consumes only dynamic current. I_{DVDD} = C_{LOAD} × V_{DVDD} × number of 0 → 1 transitions in DOUT × f_{SAMPLE}. I_{DVDD} is a load-dependent current; there is no current when the output is not toggling.

THERMAL INFORMATION

THERMAL METRIC (1)		ADS8634/8RGE RGE 24 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	32.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	30.5	
θ_{JB}	Junction-to-board thermal resistance	3.3	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	9.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	2.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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PARAMETER MEASUREMENT INFORMATION

TIMING DIAGRAM

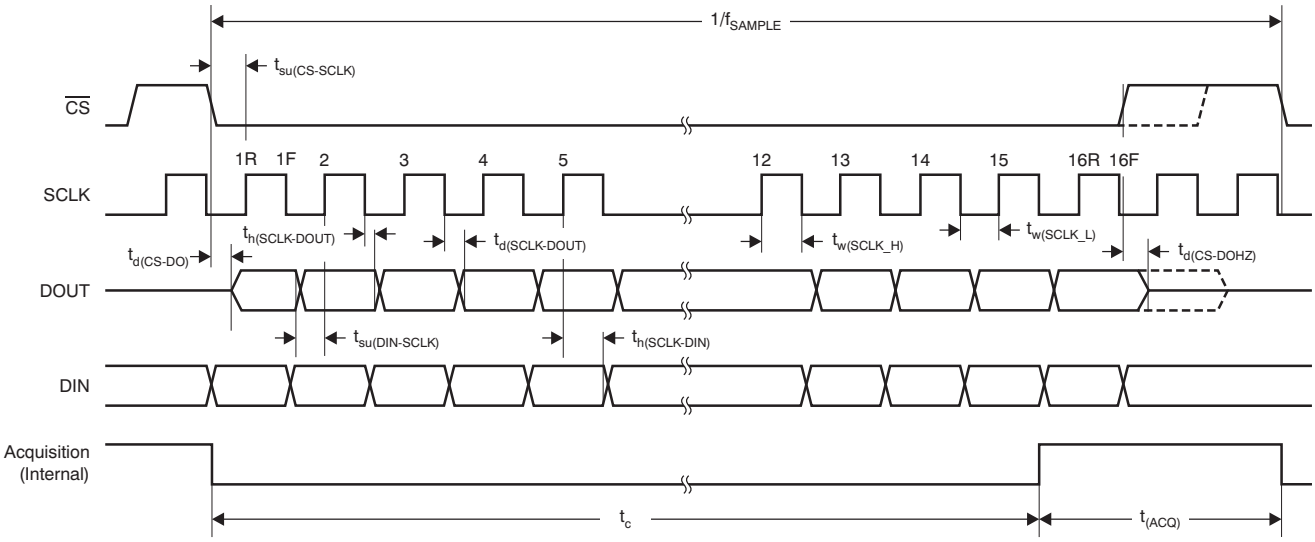

Table 1. Timing Requirements(1)(2)(3)

PARAMETER		TEST CONDITIONS	ADS8634, ADS8638 MIN	TYP	MAX	UNIT
t_c	Conversion time	DVDD = 1.8V			15	SCLK
		DVDD = 3V			15	SCLK
		DVDD = 5V			15	SCLK
$t_{(ACQ)}$	Acquisition time	DVDD = 1.8V	250			ns
		DVDD = 3V	250			ns
		DVDD = 5V	250			ns
$t_{d(CS-DO)}$	Delay time, $\overline{CS}$ low to first data (D0 to D15) out	DVDD = 1.8V			52.5	ns
		DVDD = 3V			40.0	ns
		DVDD = 5V			30.5	ns
$t_{su(CS-SCLK)}$	Setup time, $\overline{CS}$ low to first SCLK rising edge	DVDD = 1.8V	26.0			ns
		DVDD = 3V	18.5			ns
		DVDD = 5V	15.5			ns
$t_{d(SCLK-DOUT)}$	Delay time, SCLK falling to DOUT	DVDD = 1.8V			51.5	ns
		DVDD = 3V			33.0	ns
		DVDD = 5V			25.3	ns
$t_{h(SCLK-DOUT)}$	Hold time, SCLK falling to DOUT valid	DVDD = 1.8V	5.5			ns
		DVDD = 3V	5.0			ns
		DVDD = 5V	4.7			ns
$t_{d(CS-DOHZ)}$	Delay time $\overline{CS}$ high to DOUT high-z	DVDD = 1.8V	7.3		31.0	ns
		DVDD = 3V	6.4		22.0	ns
		DVDD = 5V	5.9		16.4	ns

(1) All specifications at –40°C to +125°C, unless otherwise noted.
(2) 1.8V specifications apply from 1.65V to 1.95V; 3V specifications apply from 2.7V to 3.6V; and 5V specifications apply from 4.75V to 5.25V.
(3) With 20pF load on DOUT.

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PARAMETER MEASUREMENT INFORMATION (continued)

Table 1. Timing Requirements(1)(2)(3) (continued)

PARAMETER		TEST CONDITIONS	ADS8634, ADS8638 MIN	TYP	MAX	UNIT
$t_{su(DIN-SCLK)}$	Setup time, DIN valid to SCLK rising edge	DVDD = 1.8V	7.0			ns
		DVDD = 3V	6.0			ns
		DVDD = 5V	5.0			ns
$t_{h(SCLK-DIN)}$	Hold time, SCLK rising to DIN valid	DVDD = 1.8V	9.0			ns
		DVDD = 3V	8.0			ns
		DVDD = 5V	7.0			ns
$t_{W(SCLK_H)}$	Pulse duration, SCLK high	DVDD = 1.8V	25			ns
		DVDD = 3V	20			ns
		DVDD = 5V	20			ns
$t_{W(SCLK_L)}$	Pulse duration, SCLK low	DVDD = 1.8V	25			ns
		DVDD = 3V	20			ns
		DVDD = 5V	20			ns
f_{SCLK}	SCLK frequency	DVDD = 1.8V			16	MHz
		DVDD = 3V			20	MHz
		DVDD = 5V			20	MHz
f_{SAMPLE}	Sampling frequency	DVDD = 1.8V			0.84	MSPS
		DVDD = 3V			1	MSPS
		DVDD = 5V			1	MSPS

POWER-UP TIMING REQUIREMENTS

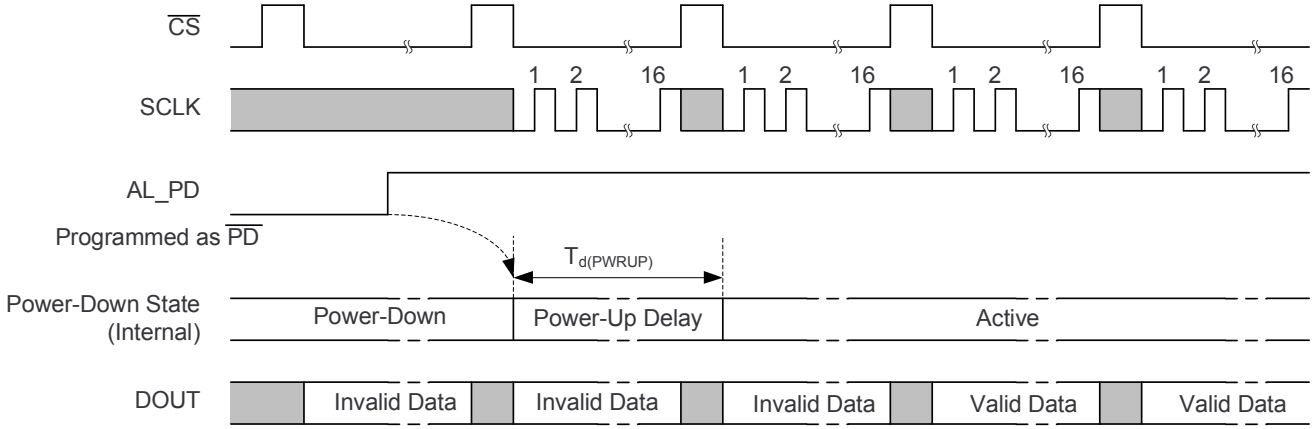

Table 2. TIMING REQUIREMENTS(1)

PARAMETER		ADS8634, ADS8638 MIN	TYP	MAX	UNIT
$t_{d(PWRUP)}$(2)	Power-up delay from first $\overline{CS}$ after power-up command			1	µs
	Invalid conversions after device is active (powered up)			1	Conversion

(1) All specifications at –40°C to +125°C, unless otherwise noted.
(2) Power-up time excludes internal reference and temperature sensor.

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PIN CONFIGURATIONS

RGE PACKAGE
4mm × 4mm QFN-24
(TOP VIEW)

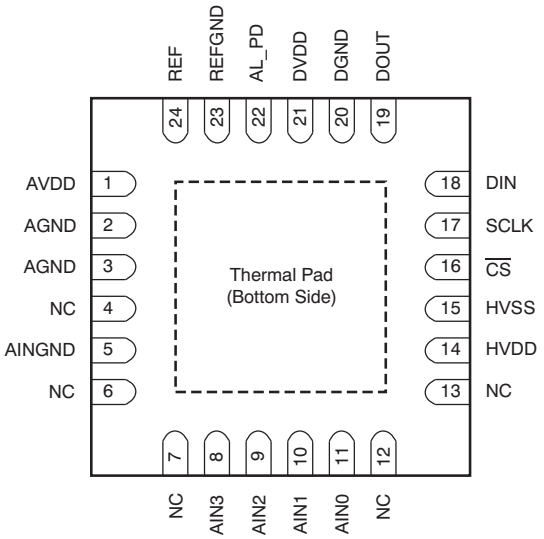

Figure 1. ADS8634 Pin Configuration

ADS8634 PIN ASSIGNMENTS

PIN NUMBER	NAME	FUNCTION	DESCRIPTION
1	AVDD	Analog power supply	Analog power supply
2, 3	AGND	Analog power supply	Analog ground
4, 6, 7, 12, 13	NC	—	These pins are not internally connected; do not float these pins. It is recommended to connect these pins to AGND.
5	AINGND	Input	Common for all analog input channels; acts as ground sense terminal
8	AIN3	Analog input	Analog input channel 3
9	AIN2	Analog input	Analog input channel 2
10	AIN1	Analog input	Analog input channel 1
11	AIN0	Analog input	Analog input channel 0
14	HVDD	High-voltage power supply	High-voltage positive supply for multiplexer channels
15	HVSS	High-voltage power supply	High-voltage negative supply for multiplexer channels
16	$\overline{CS}$	Digital input	Chip select input
17	SCLK	Digital input	Serial clock input
18	DIN	Digital input	Serial data input
19	DOUT	Digital output	Serial data output
20	DGND	Digital power supply	Digital ground
21	DVDD	Digital power supply	Digital I/O supply
22	AL_PD	Digital output	Active high, output indicates alarm (programmed as an output pin)
		Digital input	Active low, asynchronous power-down. The device features an internal, weak pull-up resistor from the AL_PD pin to DVDD. The AL_PD pin can also be floated when programmed as a power-down input. (The default condition for this pin is programmed as a power-down input pin.)
23	REFGND	Analog input	Reference ground input to device when an external reference is selected. This pin acts as a reference decoupling ground terminal when an internal reference is selected.
24	REF	Analog input	Reference input to device when an external reference is selected. This pin acts as a reference decoupling terminal when an internal reference is selected.

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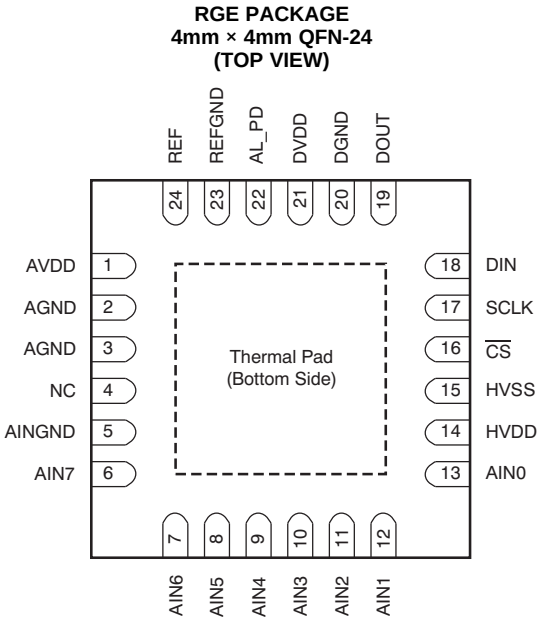

Figure 2. ADS8638 Pin Configuration

ADS8638 PIN ASSIGNMENTS

PIN NUMBER	NAME	FUNCTION	DESCRIPTION
1	AVDD	Analog power supply	Analog power supply
2, 3	AGND	Analog power supply	Analog ground
4	NC	—	This pin is not internally connected; do not float this pin. It is recommended to connect this pin to AGND.
5	AINGND	Input	Common for all analog input channels; acts as ground sense terminal
6	AIN7	Analog input	Analog input channel 7
7	AIN6	Analog input	Analog input channel 6
8	AIN5	Analog input	Analog input channel 5
9	AIN4	Analog input	Analog input channel 4
10	AIN3	Analog input	Analog input channel 3
11	AIN2	Analog input	Analog input channel 2
12	AIN1	Analog input	Analog input channel 1
13	AIN0	Analog input	Analog input channel 0
14	HVDD	High-voltage power supply	High-voltage positive supply for multiplexer channels
15	HVSS	High-voltage power supply	High-voltage negative supply for multiplexer channels
16	$\overline{CS}$	Digital input	Chip select input
17	SCLK	Digital input	Serial clock input
18	DIN	Digital input	Serial data input
19	DOUT	Digital output	Serial data output
20	DGND	Digital power supply	Digital ground
21	DVDD	Digital power supply	Digital I/O supply
22	AL_PD	Digital output	Active high, output indicating alarm (programmed as an output pin)
		Digital input	Active low, asynchronous power-down (programmed as an input pin, default condition)
23	REFGND	Analog input	Reference ground input to device when an external reference is selected. This pin acts as reference decoupling ground terminal when an internal reference is selected.
24	REF	Analog input	Reference input to device when an external reference is selected. This pin acts as reference decoupling terminal when an internal reference is selected.

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TYPICAL CHARACTERISTICS

At T_A = +25°C, internal reference = 2.5V, channel 0, range = ±2.5V, AVDD = 2.7V, DVDD = 1.8V, HVDD = 10V, HVSS = –10V, and f_{SAMPLE} = 1MSPS, unless otherwise noted.

DNL vs ANALOG SUPPLY VOLTAGE

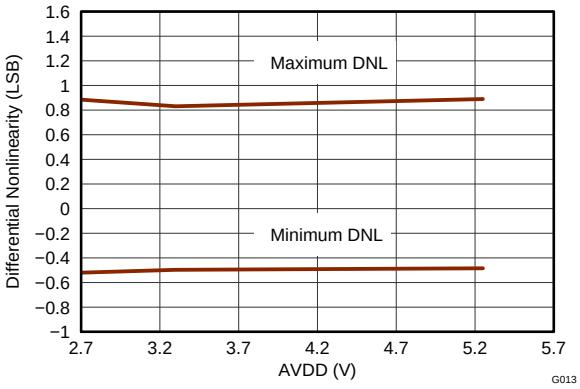

Figure 3.

DNL vs SIGNAL RANGE

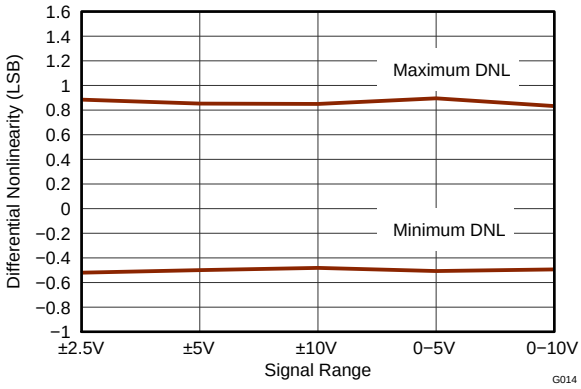

Figure 4.

DNL vs REFERENCE VOLTAGE

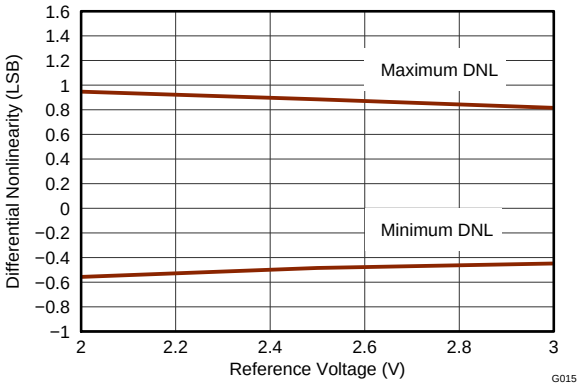

Figure 5.

DNL vs CHANNEL NUMBER

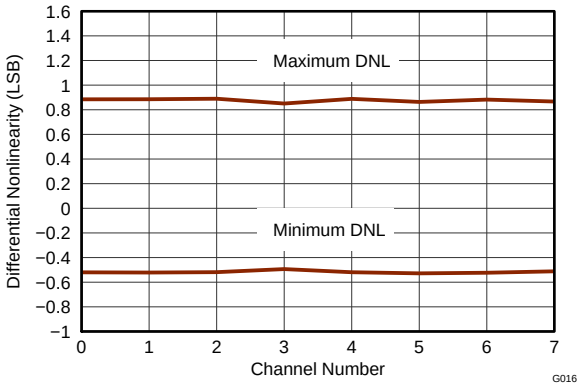

Figure 6.

DNL vs FREE-AIR TEMPERATURE

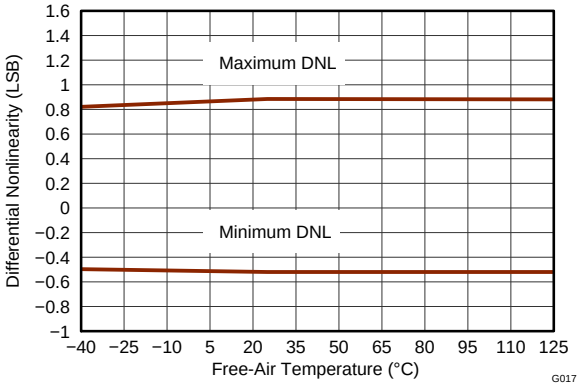

Figure 7.

DNL vs POSITIVE HIGH-VOLTAGE SUPPLY

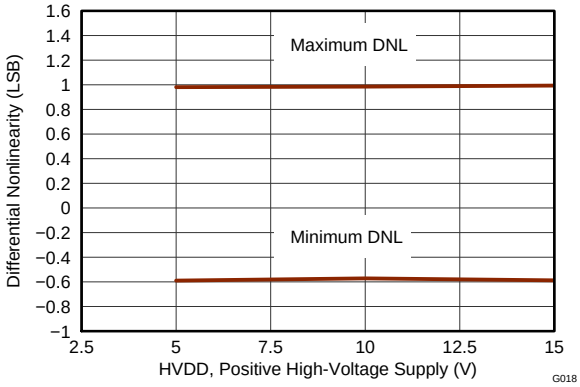

Figure 8.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, internal reference = 2.5V, channel 0, range = ±2.5V, AVDD = 2.7V, DVDD = 1.8V, HVDD = 10V, HVSS = –10V, and f_{SAMPLE} = 1MSPS, unless otherwise noted.

INL vs ANALOG SUPPLY VOLTAGE

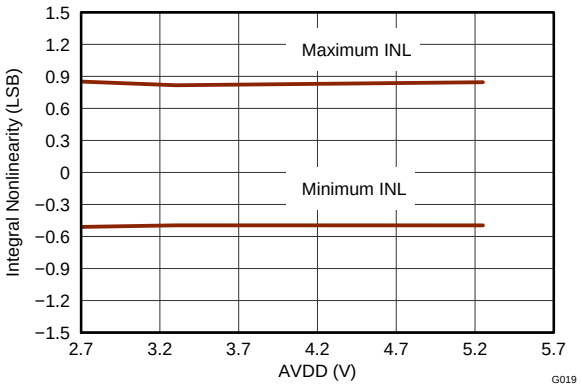

Figure 9.

INL vs SIGNAL RANGE

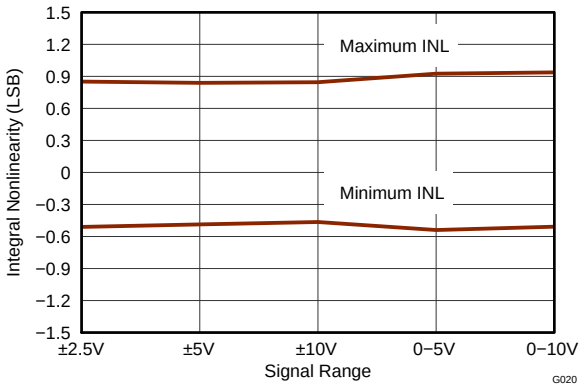

Figure 10.

INL vs REFERENCE VOLTAGE

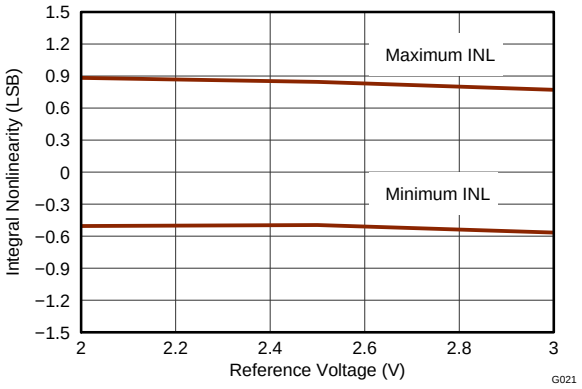

Figure 11.

INL vs CHANNEL NUMBER

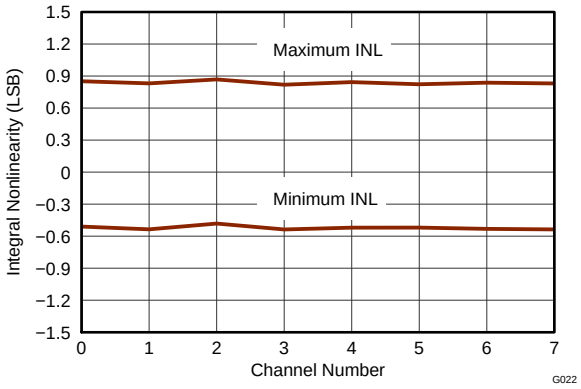

Figure 12.

INL vs FREE-AIR TEMPERATURE

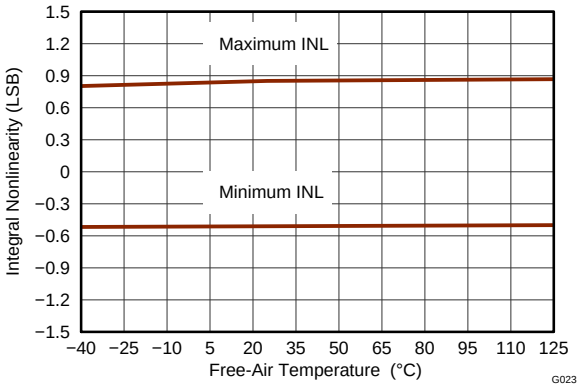

Figure 13.

INL vs POSITIVE HIGH-VOLTAGE SUPPLY

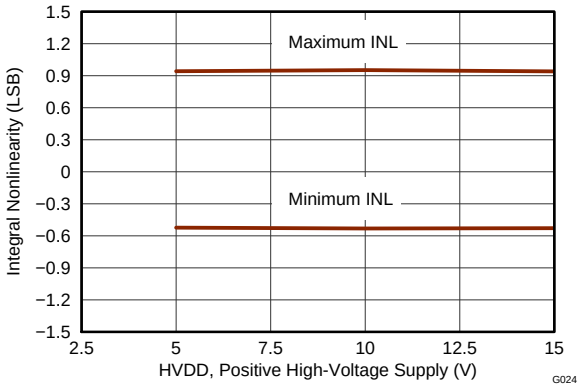

Figure 14.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, internal reference = 2.5V, channel 0, range = ±2.5V, AVDD = 2.7V, DVDD = 1.8V, HVDD = 10V, HVSS = –10V, and f_{SAMPLE} = 1MSPS, unless otherwise noted.

OFFSET ERROR vs ANALOG SUPPLY VOLTAGE

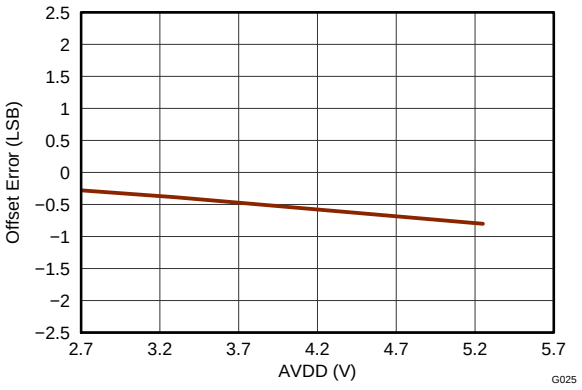

Figure 15.

OFFSET ERROR vs SIGNAL RANGE

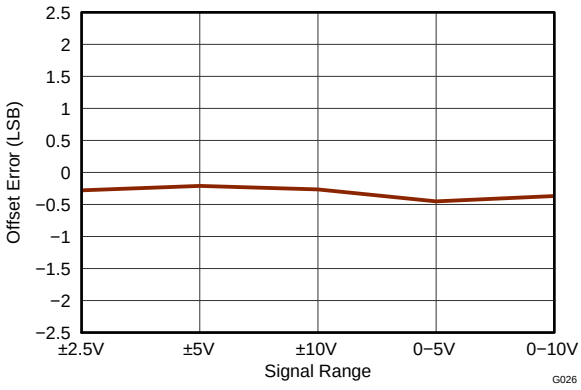

Figure 16.

OFFSET ERROR vs REFERENCE VOLTAGE

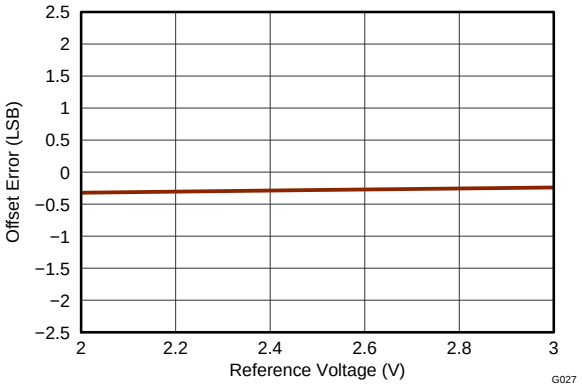

Figure 17.

OFFSET ERROR vs CHANNEL NUMBER

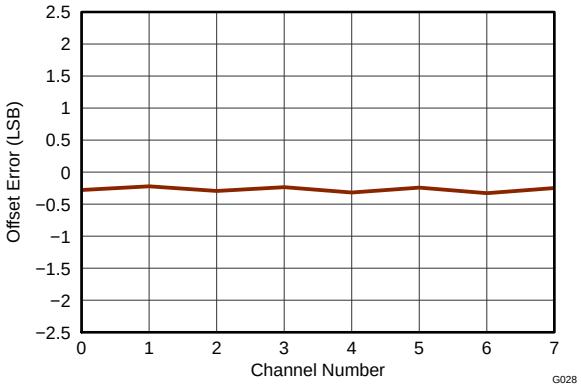

Figure 18.

OFFSET ERROR vs FREE-AIR TEMPERATURE

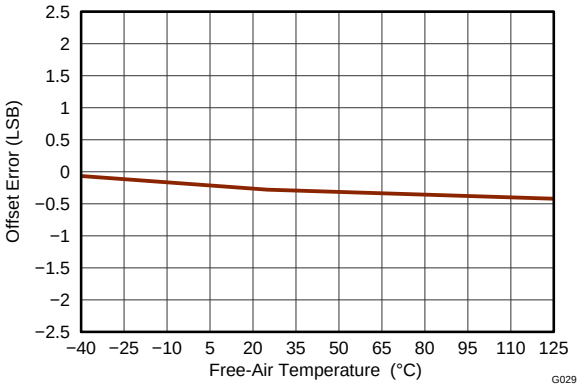

Figure 19.

OFFSET ERROR vs POSITIVE HIGH-VOLTAGE SUPPLY

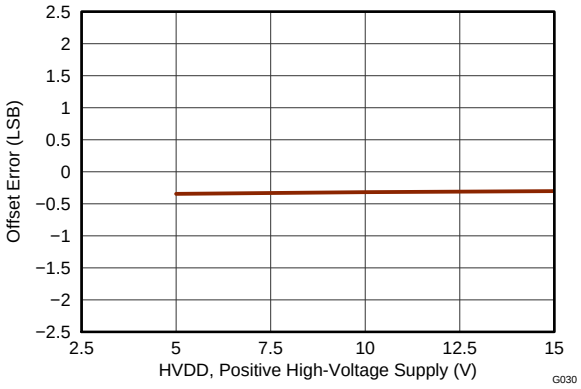

Figure 20.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, internal reference = 2.5V, channel 0, range = ±2.5V, AVDD = 2.7V, DVDD = 1.8V, HVDD = 10V, HVSS = –10V, and f_{SAMPLE} = 1MSPS, unless otherwise noted.

GAIN ERROR vs ANALOG SUPPLY VOLTAGE

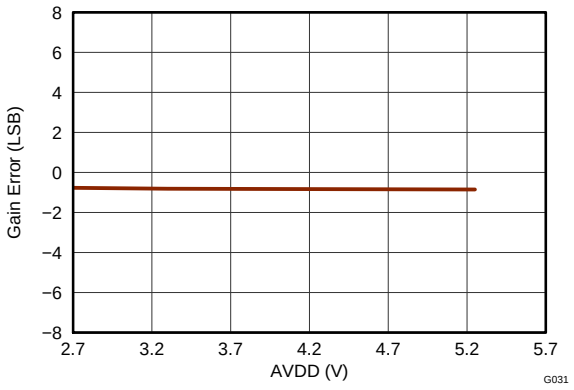

Figure 21.

GAIN ERROR vs SIGNAL RANGE

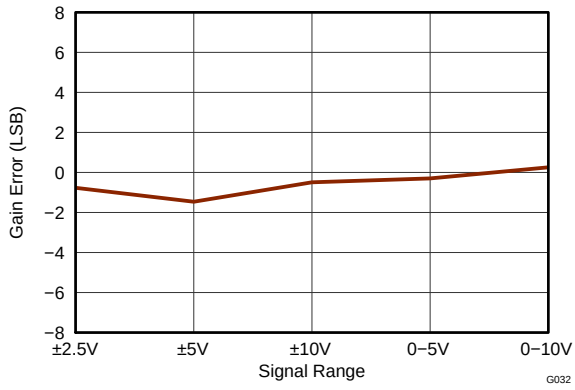

Figure 22.

GAIN ERROR vs REFERENCE VOLTAGE

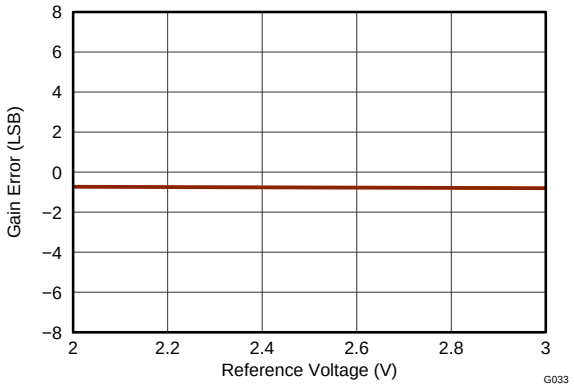

Figure 23.

GAIN ERROR vs CHANNEL NUMBER

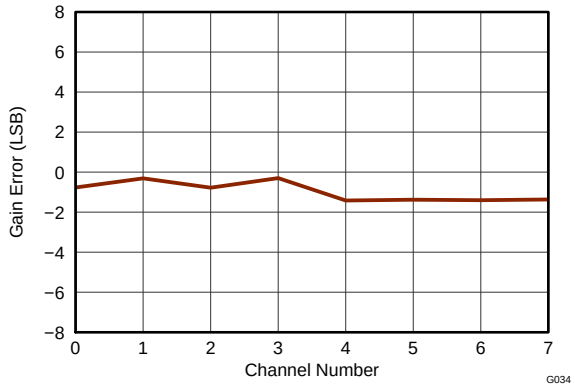

Figure 24.

GAIN ERROR vs FREE-AIR TEMPERATURE

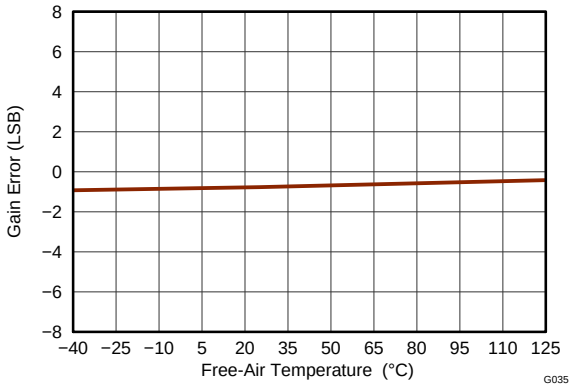

Figure 25.

GAIN ERROR vs POSITIVE HIGH-VOLTAGE SUPPLY

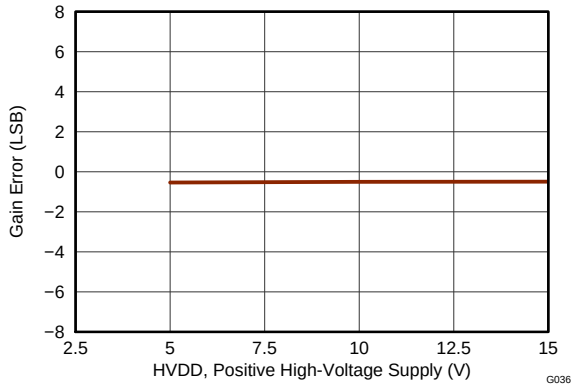

Figure 26.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, internal reference = 2.5V, channel 0, range = ±2.5V, AVDD = 2.7V, DVDD = 1.8V, HVDD = 10V, HVSS = –10V, and f_{SAMPLE} = 1MSPS, unless otherwise noted.

SNR vs ANALOG SUPPLY VOLTAGE

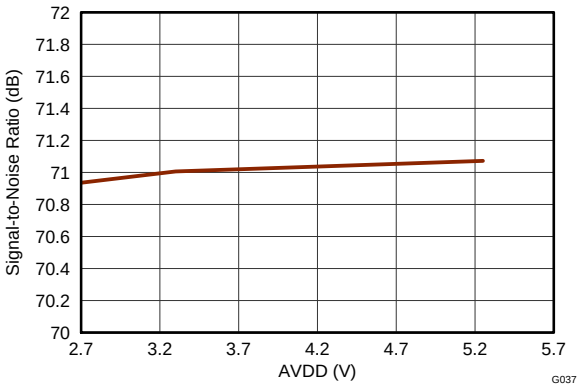


Figure 27.

SNR vs SIGNAL RANGE

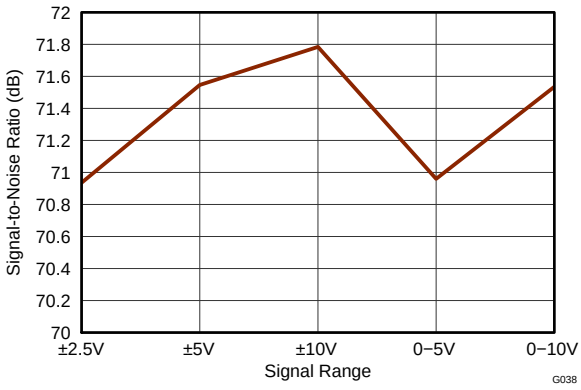


Figure 28.

SNR vs REFERENCE VOLTAGE

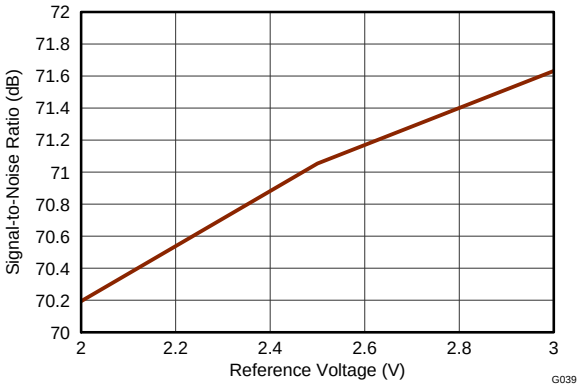


Figure 29.

SNR vs CHANNEL NUMBER

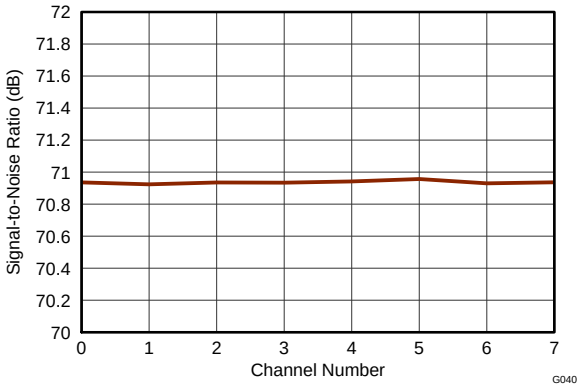


Figure 30.

SNR vs FREE-AIR TEMPERATURE

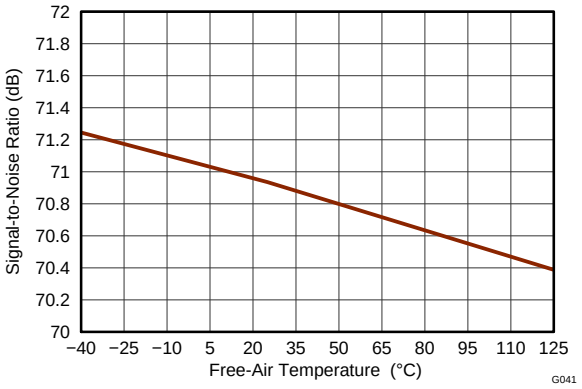
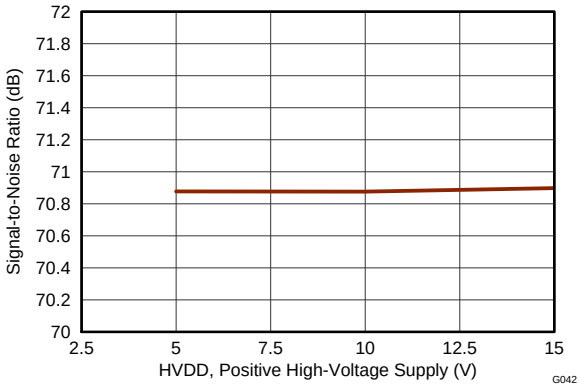


Figure 31.

SNR vs POSITIVE HIGH-VOLTAGE SUPPLY



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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, internal reference = 2.5V, channel 0, range = ±2.5V, AVDD = 2.7V, DVDD = 1.8V, HVDD = 10V, HVSS = –10V, and f_{SAMPLE} = 1MSPS, unless otherwise noted.

SNR vs INPUT FREQUENCY

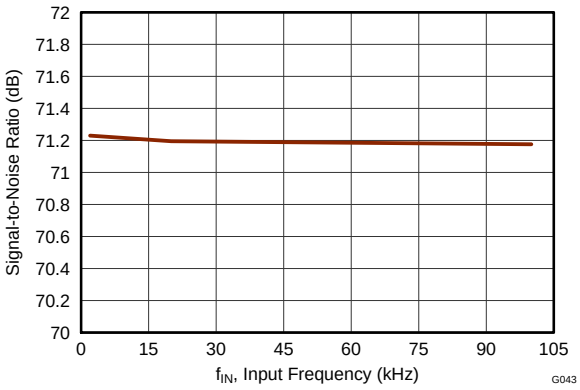

Figure 33.

SINAD vs ANALOG SUPPLY VOLTAGE

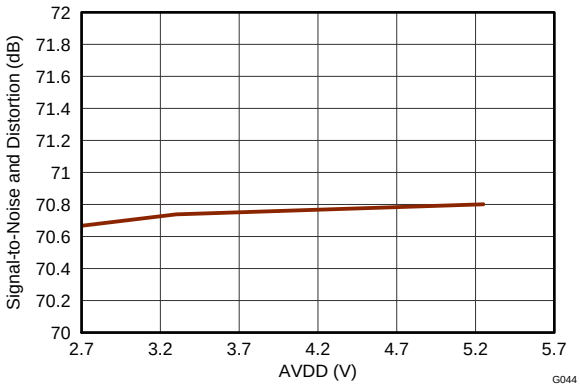

Figure 34.

SINAD vs SIGNAL RANGE

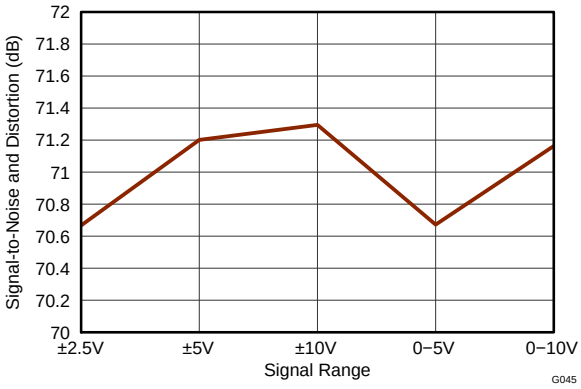

Figure 35.

SINAD vs REFERENCE VOLTAGE

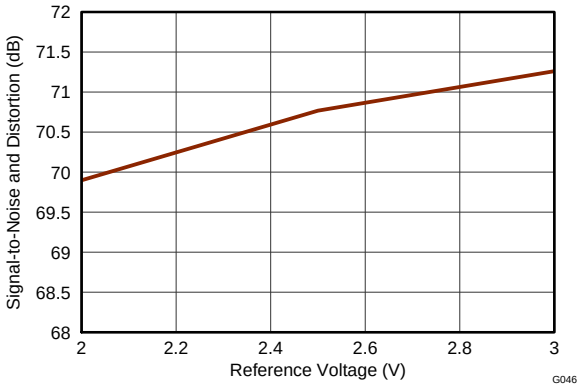

Figure 36.

SINAD vs CHANNEL NUMBER

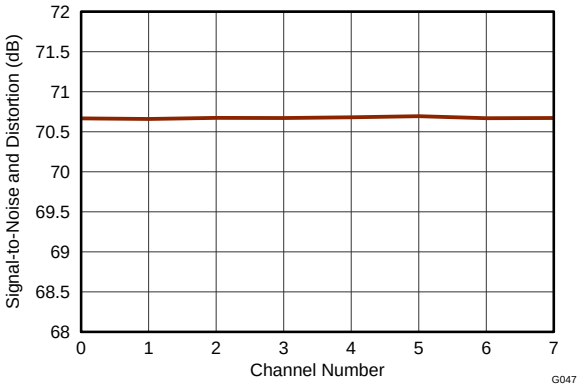

Figure 37.

SINAD vs FREE-AIR TEMPERATURE

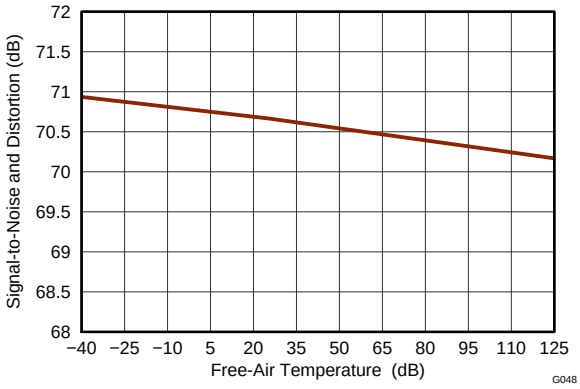

Figure 38.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, internal reference = 2.5V, channel 0, range = ±2.5V, AVDD = 2.7V, DVDD = 1.8V, HVDD = 10V, HVSS = –10V, and f_{SAMPLE} = 1MSPS, unless otherwise noted.

SINAD vs POSITIVE HIGH-VOLTAGE SUPPLY

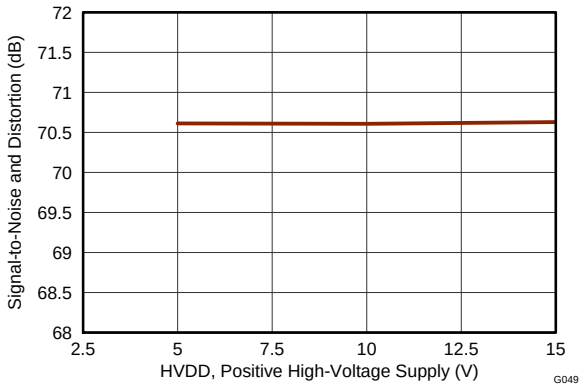


Figure 39.

SINAD vs INPUT FREQUENCY

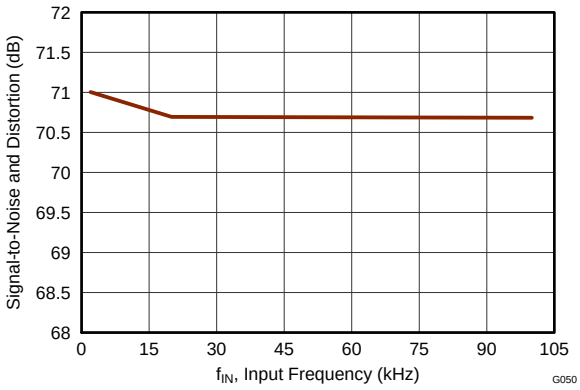


Figure 40.

THD vs ANALOG SUPPLY VOLTAGE

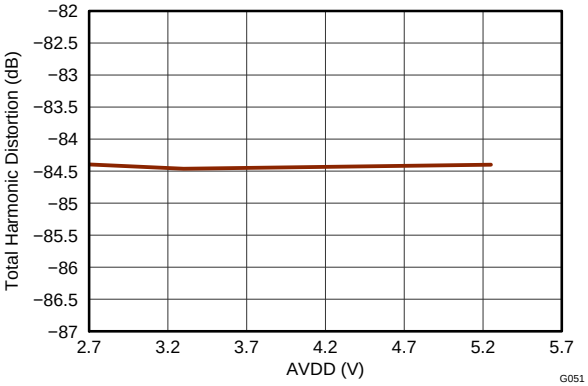


Figure 41.

THD vs SIGNAL RANGE

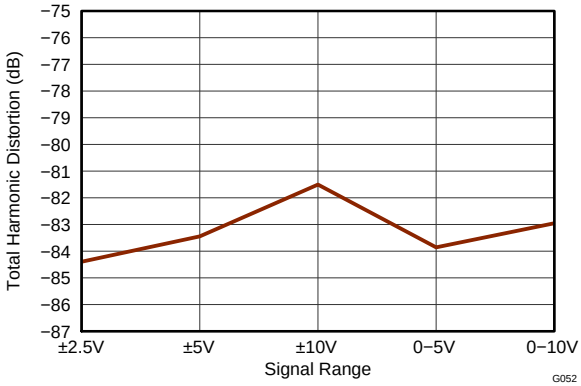


Figure 42.

THD vs REFERENCE VOLTAGE

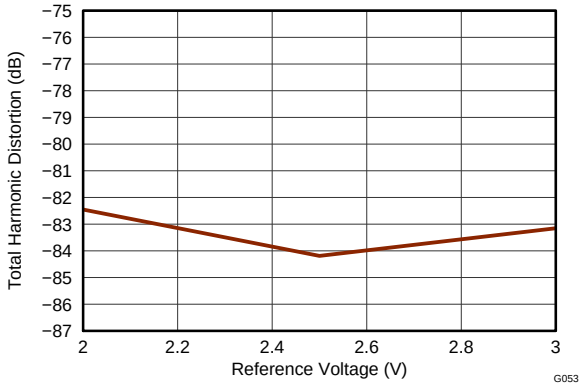
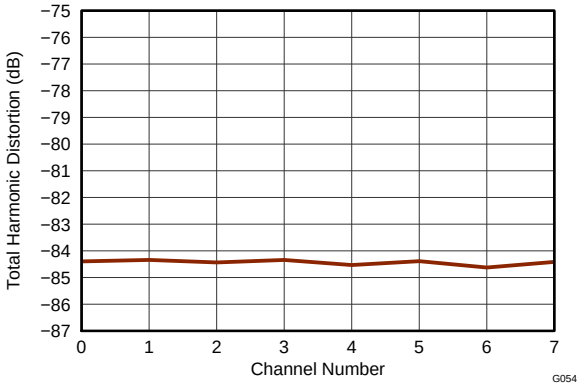


Figure 43.

THD vs CHANNEL NUMBER



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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, internal reference = 2.5V, channel 0, range = ±2.5V, AVDD = 2.7V, DVDD = 1.8V, HVDD = 10V, HVSS = –10V, and f_{SAMPLE} = 1MSPS, unless otherwise noted.

THD vs FREE-AIR TEMPERATURE

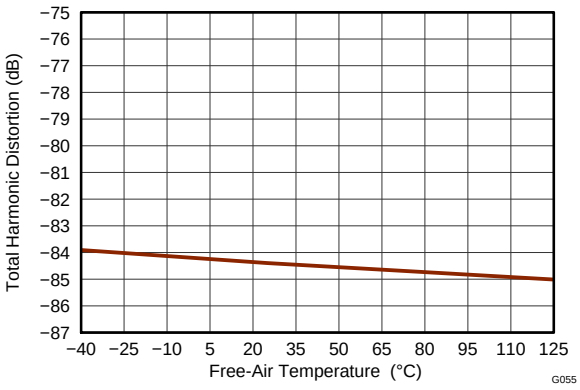

Figure 45.

THD vs POSITIVE HIGH-VOLTAGE SUPPLY

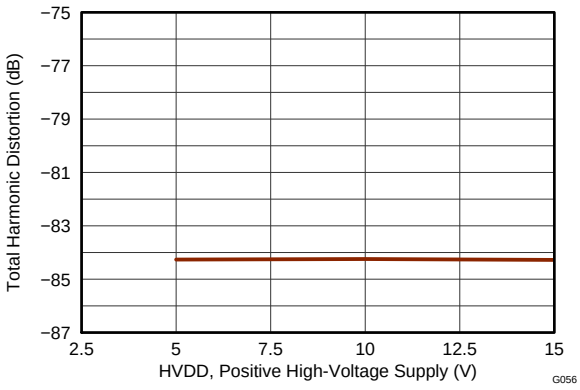

Figure 46.

THD vs INPUT FREQUENCY

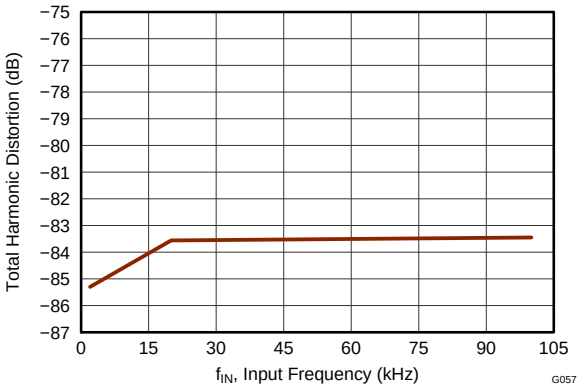

Figure 47.

SFDR vs ANALOG SUPPLY VOLTAGE

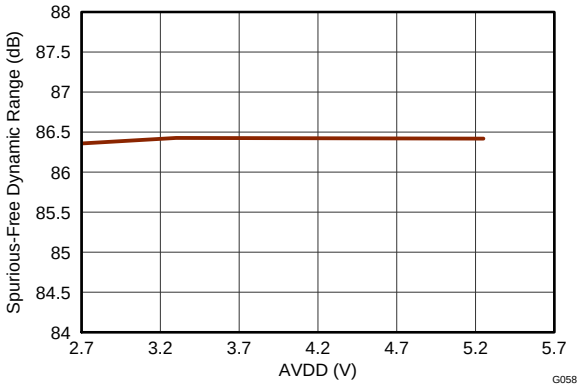

Figure 48.

SFDR vs SIGNAL RANGE

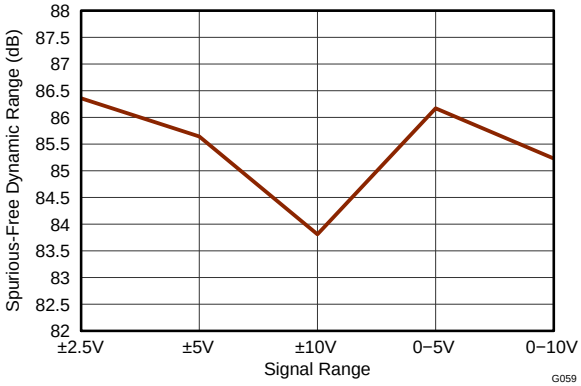

Figure 49.

SFDR vs REFERENCE VOLTAGE

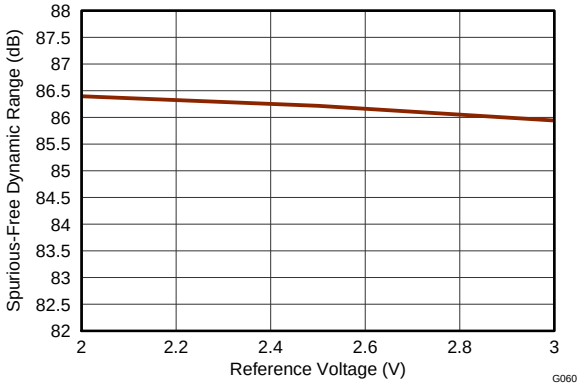

Figure 50.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, internal reference = 2.5V, channel 0, range = ±2.5V, AVDD = 2.7V, DVDD = 1.8V, HVDD = 10V, HVSS = –10V, and f_{SAMPLE} = 1MSPS, unless otherwise noted.

SFDR vs CHANNEL NUMBER

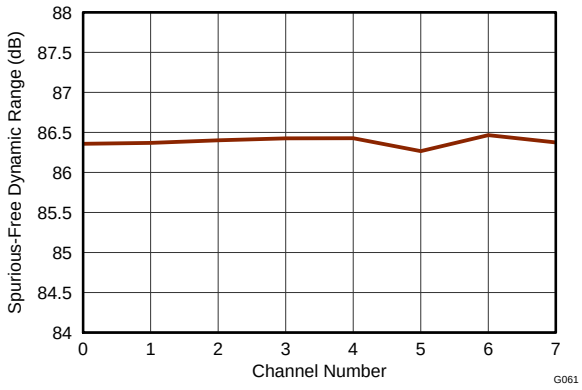

Figure 51.

SFDR vs FREE-AIR TEMPERATURE

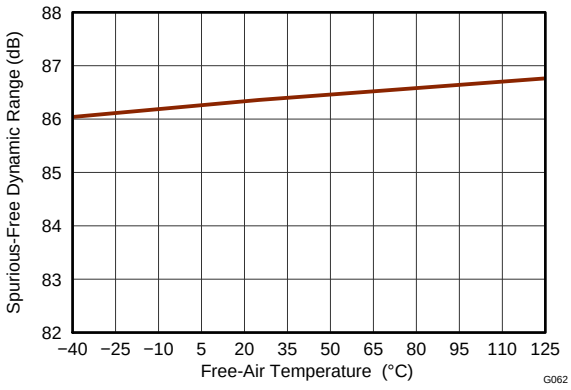

Figure 52.

SFDR vs POSITIVE HIGH-VOLTAGE SUPPLY

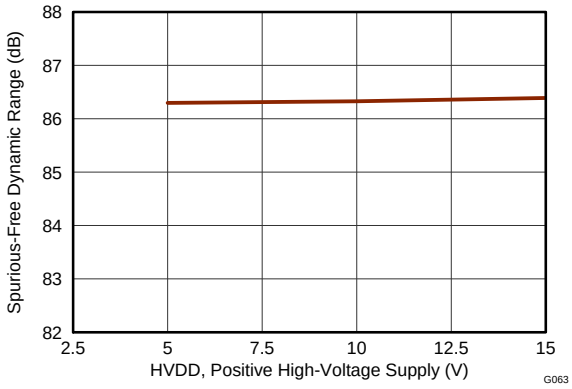

Figure 53.

SFDR vs INPUT FREQUENCY

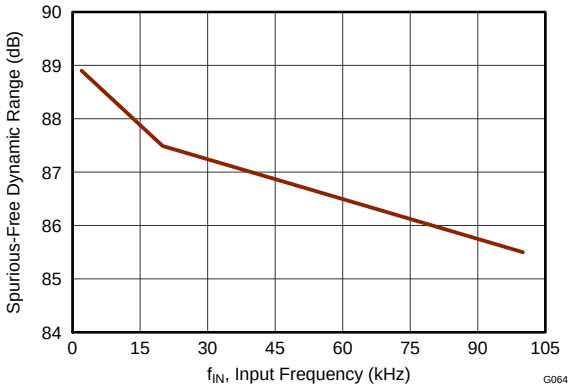

Figure 54.

CROSSTALK vs INPUT FREQUENCY

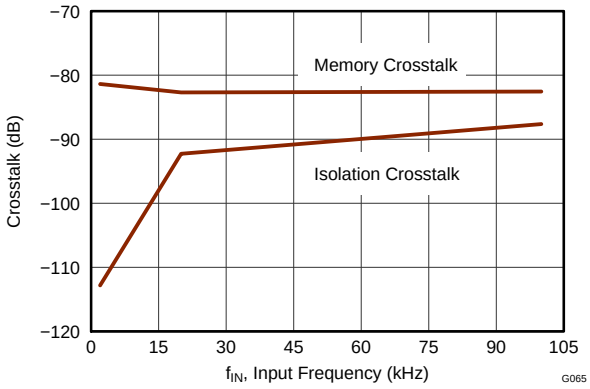

Figure 55.

ANALOG SUPPLY CURRENT (Dynamic) vs ANALOG SUPPLY VOLTAGE

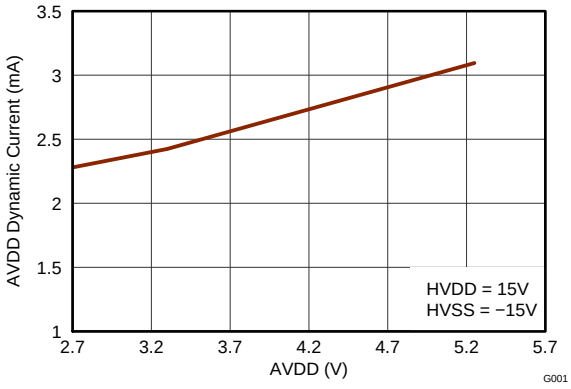

Figure 56.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, internal reference = 2.5V, channel 0, range = ±2.5V, AVDD = 2.7V, DVDD = 1.8V, HVDD = 10V, HVSS = –10V, and f_{SAMPLE} = 1MSPS, unless otherwise noted.

ANALOG SUPPLY CURRENT (Dynamic) vs FREE-AIR TEMPERATURE

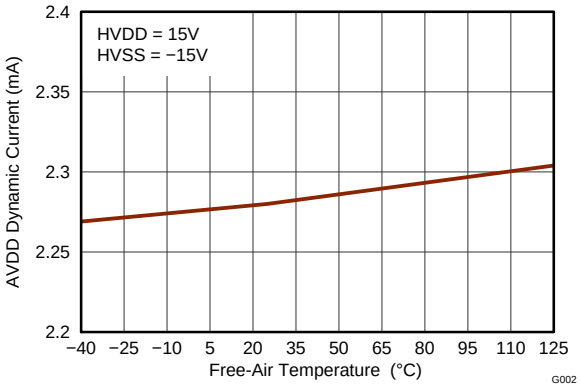

Figure 57.

ANALOG SUPPLY CURRENT (Dynamic) vs SAMPLE RATE

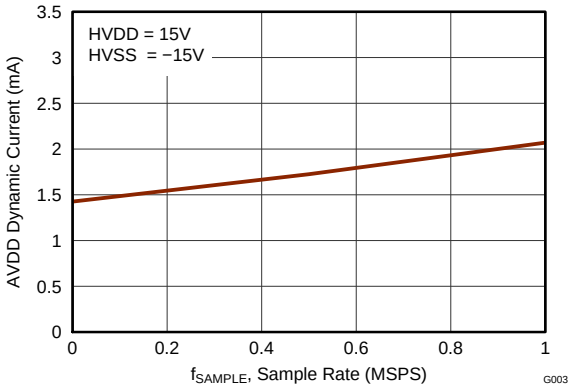

Figure 58.

ANALOG SUPPLY CURRENT (Static) vs ANALOG SUPPLY VOLTAGE

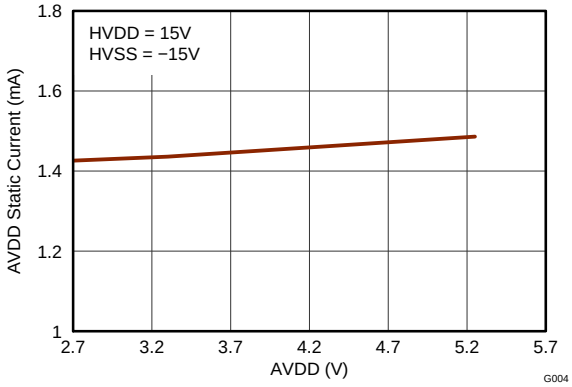

Figure 59.

POSITIVE HIGH-VOLTAGE SUPPLY CURRENT (Dynamic) vs ANALOG SUPPLY VOLTAGE

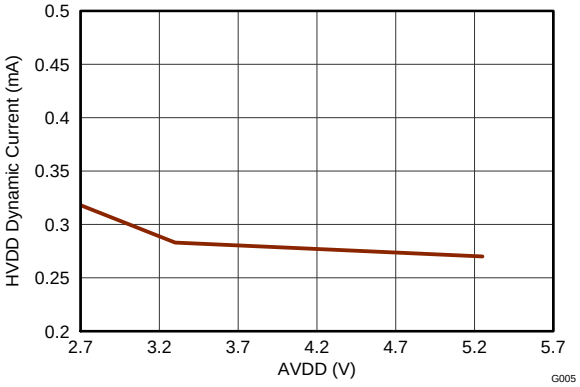

Figure 60.

POSITIVE HIGH-VOLTAGE SUPPLY CURRENT (Dynamic) vs FREE-AIR TEMPERATURE

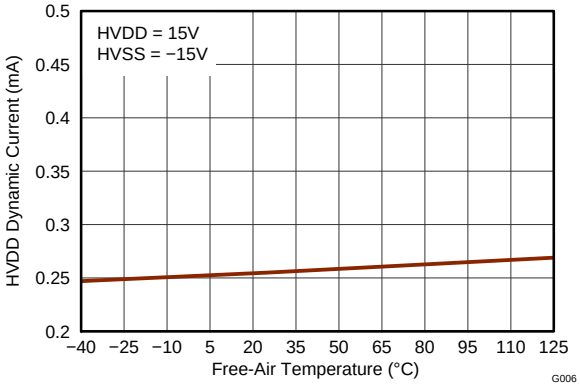

Figure 61.

POSITIVE HIGH-VOLTAGE SUPPLY CURRENT (Dynamic) vs POSITIVE HIGH-VOLTAGE SUPPLY

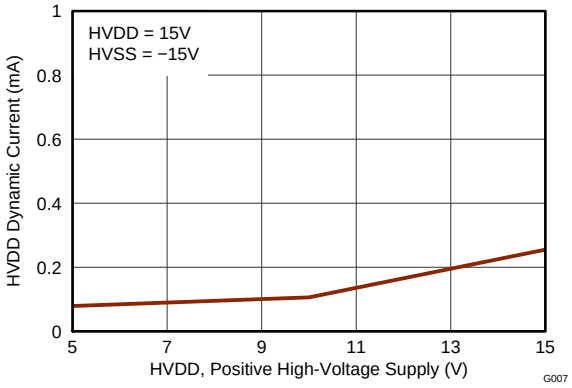

Figure 62.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, internal reference = 2.5V, channel 0, range = ±2.5V, AVDD = 2.7V, DVDD = 1.8V, HVDD = 10V, HVSS = –10V, and f_{SAMPLE} = 1MSPS, unless otherwise noted.

POSITIVE HIGH-VOLTAGE SUPPLY CURRENT (Dynamic) vs SAMPLE RATE

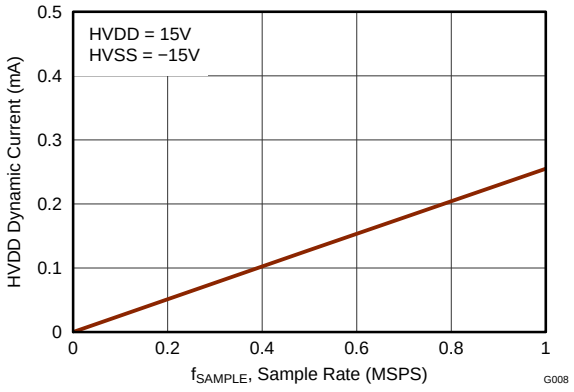

Figure 63.

NEGATIVE HIGH-VOLTAGE SUPPLY CURRENT (Dynamic) vs ANALOG SUPPLY VOLTAGE

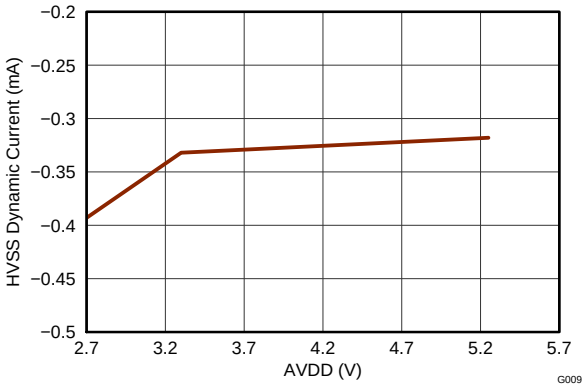

Figure 64.

NEGATIVE HIGH-VOLTAGE SUPPLY CURRENT (Dynamic) vs FREE-AIR TEMPERATURE

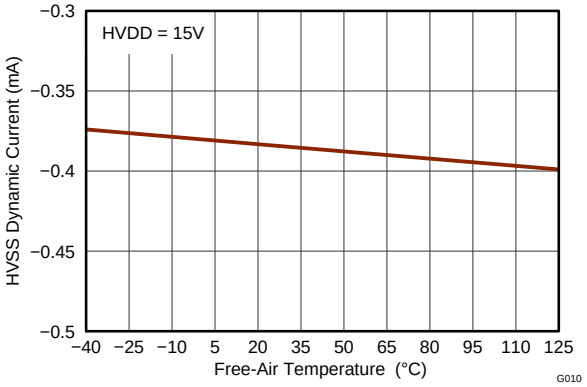

Figure 65.

NEGATIVE HIGH-VOLTAGE SUPPLY CURRENT (Dynamic) vs NEGATIVE HIGH-VOLTAGE SUPPLY

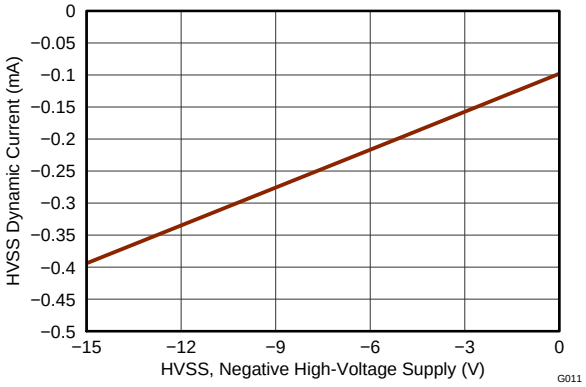

Figure 66.

NEGATIVE HIGH-VOLTAGE SUPPLY CURRENT (Dynamic) vs SAMPLE RATE

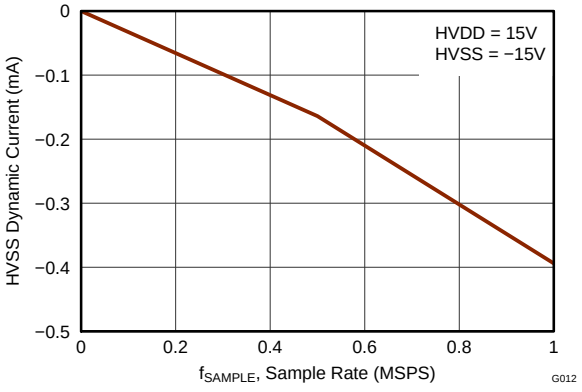

Figure 67.

DNL

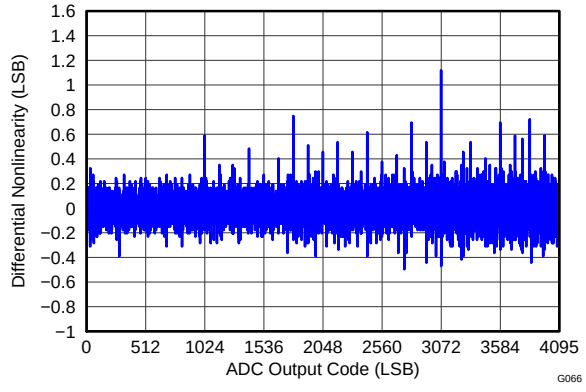

Figure 68.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, internal reference = 2.5V, channel 0, range = ±2.5V, AVDD = 2.7V, DVDD = 1.8V, HVDD = 10V, HVSS = –10V, and f_{SAMPLE} = 1MSPS, unless otherwise noted.

INL

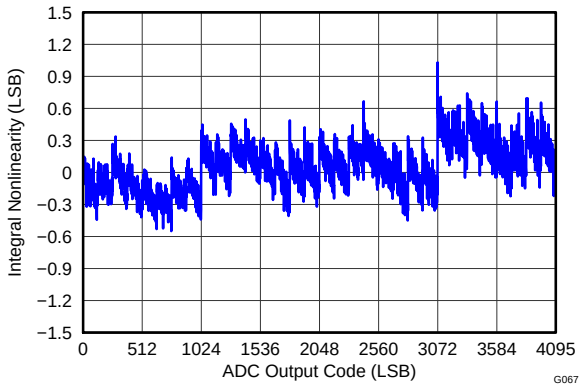

Figure 69.

SPECTRAL RESPONSE

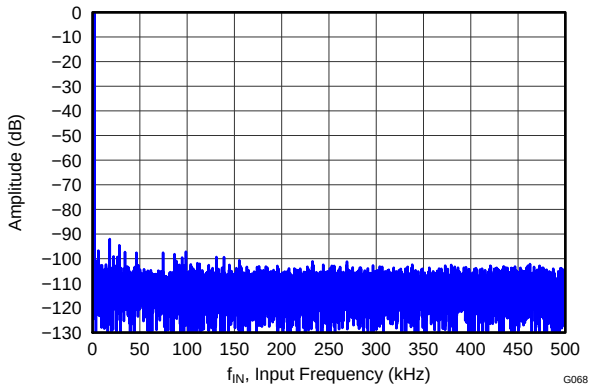

Figure 70.

TEMPERATURE SENSOR OUTPUT vs FREE-AIR TEMPERATURE

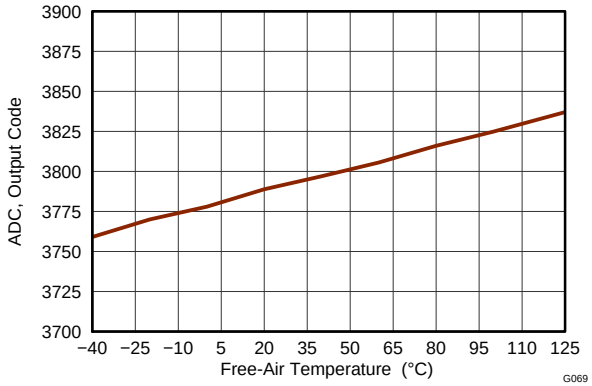

Figure 71.

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OVERVIEW

The ADS8634 and ADS8638 are 12-bit, 4- and 8-channel devices, respectively. The ADS8634/8 feature software-selectable bipolar and unipolar ranges, an internal reference with an option to use an external reference, and an internal temperature sensor. Independent power-down control for the internal reference and temperature sensor blocks allows for optimal power based on application. The following sections describe the individual blocks and operation.

MULTIPLEXER AND ANALOG INPUT

The ADS8634/8 feature single ended inputs with ground sense and a 4-/8-channel, single-pole multiplexer, respectively. The ADC samples the difference voltage between analog input pins *AINx* and the ground sense pin *AINGND*. The ADS8634/8 can scan these analog inputs in either manual or auto-scan mode. In manual mode, the channel is selected for every sample via a register write; in auto-scan mode, the channel number is incremented automatically on every $\overline{CS}$ falling edge after the present channel is sampled. It is possible to select the analog inputs for an auto scan with register settings. The devices automatically scan only the selected analog inputs in ascending order.

The ADS8634/8 offer multiple software-programmable ranges ±10V, ±5V, ±2.5V, 0V to 5V, and 0V to 10V with a 2.5V reference. Any of these ranges can be assigned to any analog input (for instance, ±10V can be assigned to AIN1, ±2.5V to AIN2, 0V to 10V can be assigned to AIN3, and so on). During a scan (either auto or manual), the programmed signal range is assigned to the selected channel. The range selection, however, can be temporarily overridden using the DIN line for a particular scan. This feature is useful for zooming into a narrow range when needed. Refer to Table 11 for configuration register settings.

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Figure 72 shows electrostatic discharge (ESD) diodes connected to the HVDD and HVSS supplies. Make sure these diodes do not turn on by keeping the analog inputs within the specified range.

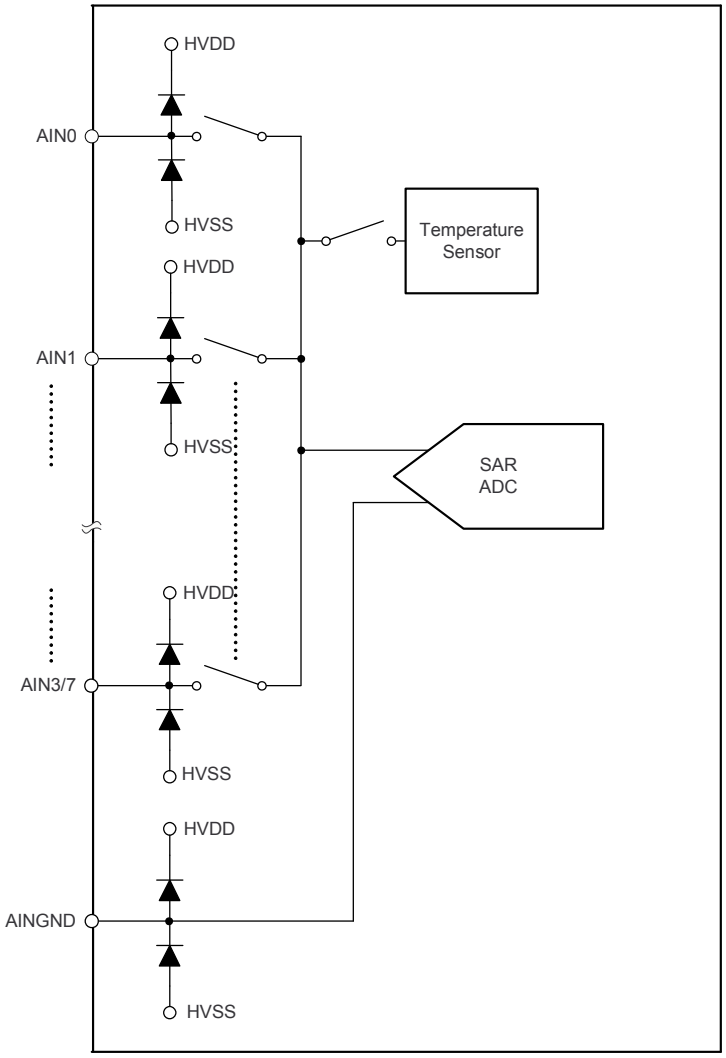

Figure 72. Analog Inputs

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The ADS8634/8 sample the voltage difference (V_{AINx} – V_{AINGND}) between the selected analog input channel and the AINGND pin. The ADS8634/8 allow a ±0.2V range on AINGND. This feature is useful in modular systems where the sensor/signal conditioning block is removed from the ADC and when there could be a difference in the ground potential of the sensor/signal condioner from the ADC ground. In such cases, it is recommended to run separate wires from the AINGND terminal of the device to the sensor/signal conditioner ground.

REFERENCE

The ADS8634/8 measure the analog input signals relative to the voltage reference using either an internal precision 2.5V voltage reference (Figure 73) or an external voltage reference (Figure 74). Binary-weighted capacitors are switched onto the reference terminal during conversion. The switching frequency is the same as the SCLK frequency. Whether it is an internal or external reference, be sure to decouple the REF terminal to REFGND with a 10µF capacitor. Place the capacitor close to the REFP and REFGND pins.

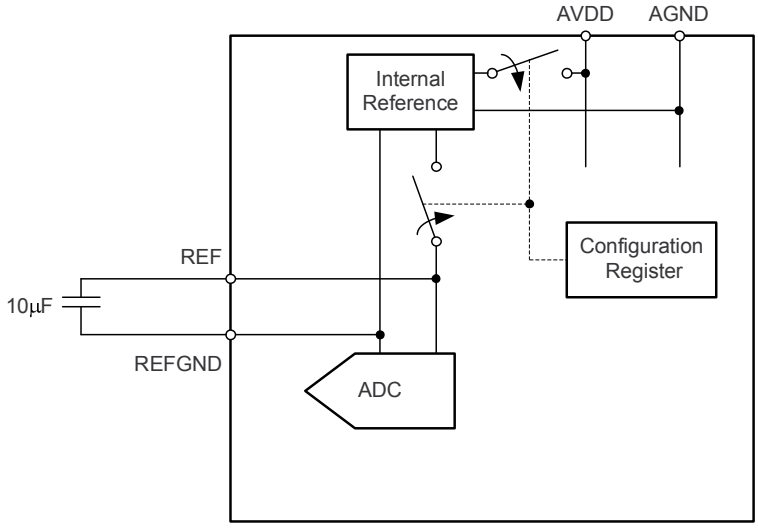

Figure 73. Operation Using The Internal Reference
(Refer to Table 11 for more details on the configuration register settings)

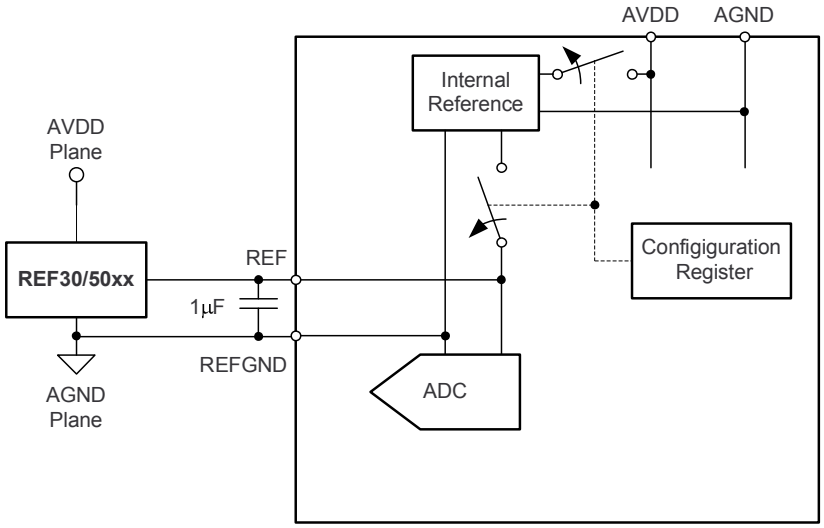

Figure 74. Operation Using an External Reference
(Refer to Table 11 for more details on the configigiuration register settings)

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These devices allow the use of an external reference in the range of 2.0V to 3.0V. The nominal input ranges ±10V, ±5V, ±2.5V, 0V to 5V, and 0V to 10V assume a 2.5V reference; a different reference voltage scales the full-scale ranges proportionately. For example, if a 3.0V reference is used and the ±10V range is selected, the actual input range is scaled by (3.0/2.5) for a full-scale range of ±12V.

The internal reference can be enabled/disabled through the configuration register. The reference block is powered down when the internal reference is disabled. Ensure that the internal reference is disabled when the external reference is connected. The external reference is the default selection after power-on or reset.

TEMPERATURE SENSOR

The ADS8634/8 feature an on-chip temperature sensoras shown in Figure 75. The device temperature can be read at any time during a scan, either in auto or manual mode.There are three registers associated with the temperature sensor operation. The temperature sensor can be enabled/disabled through the Aux-Config configuration register. Disabling the temperature sensor powers down the temperature block. It is necessary to enable (power up) the temperature sensor at least one cycle before the device temperature sensor is selected with the channel sequencing control registers (manual/auto). This selection overrides the input channel scan sequence and range selection and connects the ADC input to an internal temperature sensor. The temperature sensor must be deselected with channel sequencing control registers (manual/auto) to resume normal scanning. In case of auto-sequencing, the device starts scanning from where it left off before the temperature measurement. The temperature sensor is disabled by default after power-on or reset.

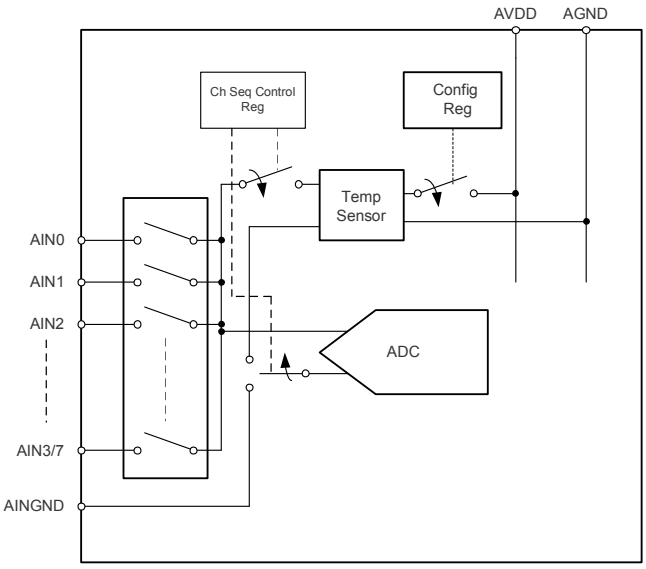

Figure 75. Reading the ADS8634/8 Temperature
(Refer to Table 11 for more details on configuration register settings)

The temperature sensor transfer function follows a straight line, as shown in Equation 1:

$$\text{Output Code} = m_{REF} \times \text{Device Temperature in °C} + C_{REF} \quad (1)$$

Equation 1 can be re-written as Equation 2:

$$\text{Device Temperature in °C} = (\text{Output Code} - C_{REF})/m_{REF}$$

where:

m_{REF} = the slope,

and C_{REF} = the offset (in ADC output code) of the temperature sensor transfer function (2)

Both m_{REF} and C_{REF} change with the reference voltage. The initial values of m_{REF} and C_{REF} at a 2.5V reference are: $m_{REF_2.5}$ = 0.47 and $C_{REF_2.5}$ = 3777.2

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Values of m_{REF} and C_{REF} for any reference voltage other than 2.5V can be calculated using Equation 3 and Equation 4:

$$m_{REF} = m_{REF_2.5} \times 2.5/V_{REF} \quad (3)$$

$$C_{REF} = (C_{REF_2.5} - 3584) \times 2.5/V_{REF} + 3584 \quad (4)$$

For example, at a 2V reference:

$m_{REF_2} = 0.47 \times 2.5/2 = 0.59$ and

$C_{REF_2} = (3777.2 - 3584) \times 2.5/2 + 3584 = 3825.5$

For the reference voltage used, Equation 2 can be rewritten using m_{REF} and C_{REF} as calculated in Equation 3 and Equation 4.

Table 3 can be used as quick reference for temperature sensor transfer function at typical reference values.

Table 3. Temperature Sensor Transfer Function at Typical Reference Values

REFERENCE VOLTAGE (V)	TRANSFER FUNCTION
2	Device temperature in °C = (output code – 3825.5)/0.59
2.5	Device temperature in °C = (output code – 3777.2)/0.47
3	Device temperature in °C = (output code – 3745.0)/0.39

DATA FORMAT

The ADS8634/8 output 12-bits of ADC conversion results in binary format (MSB first) for all ranges, as shown in Table 4. Figure 76 shows the ADC transfer function for bipolar signal ranges. The unipolar range output is shown in Table 5 and Figure 77 shows the transfer function.

Table 4. Bipolar Range Ideal Output Codes(1)

INPUT SIGNAL (AINx – AINGND)			IDEAL OUTPUT CODE
±10V RANGE (V)	±5V RANGE (V)	±2.5V RANGE (V)	
≥ 10 × (2^{11}– 1)/2^{11}(2)	≥ 5 × (2^{11}– 1)/2^{11}	≥ 2.5 × (2^{11}– 1)/2^{11}	FFFh
10/2^{11}	5/2^{11}	2.5/2^{11}	801h
0	0	0	800h
–10 /2^{11}	–5/2^{11}	–2.5/2^{11}	7FFh
≤ –10 × (2^{11}– 1)/2^{11}	≤ –5 × (2^{11}– 1)/2^{11}	≤ –2.5 × (2^{11}– 1)/2^{11}	000h

(1) Excludes noise, offset and gain errors.
(2) LSB size for the bipolar ranges = positive (or negative) full-scale/2^{11}. The ADS8634/8 offer 12-bit resolution across the entire range from positive full-scale to negative full-scale; in other words, the resolution for half range from '0' to positive (or negative) full-scale is 11 bits. For example, a 1LSB for a ±10V range is 10/2^{11}.

Table 5. Unipolar Range Ideal Output Codes(1)

INPUT SIGNAL (AINx – AINGND)		IDEAL OUTPUT CODE
0V TO 10V RANGE (V)	0V TO 5V RANGE (V)	
≥ 10 × (2^{12}– 1)/2^{12}	≥ 5 × (2^{12}– 1)/2^{12}	FFFh
10/2^{12}	5/2^{12}	001h
< 10/2^{12}	< 5/2^{12}	000h

(1) Excludes noise, offset and gain errors.

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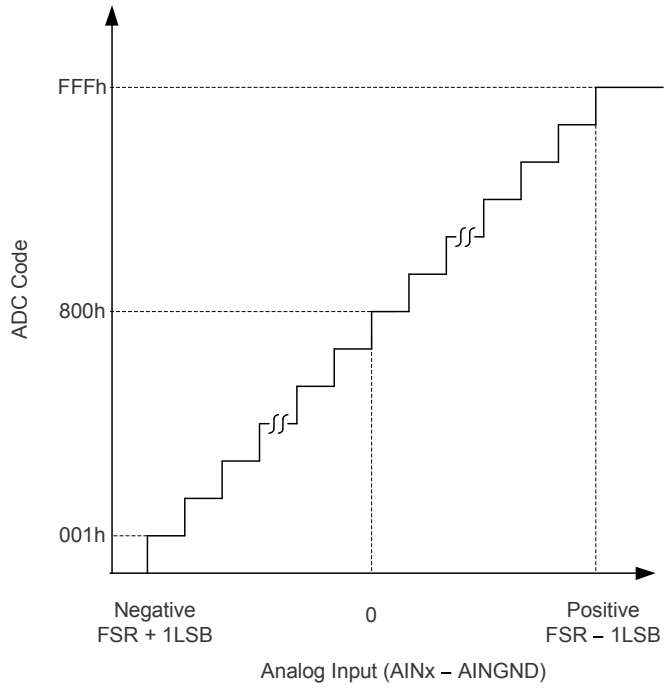

Figure 76. Transfer Function for Bipolar Signal Ranges

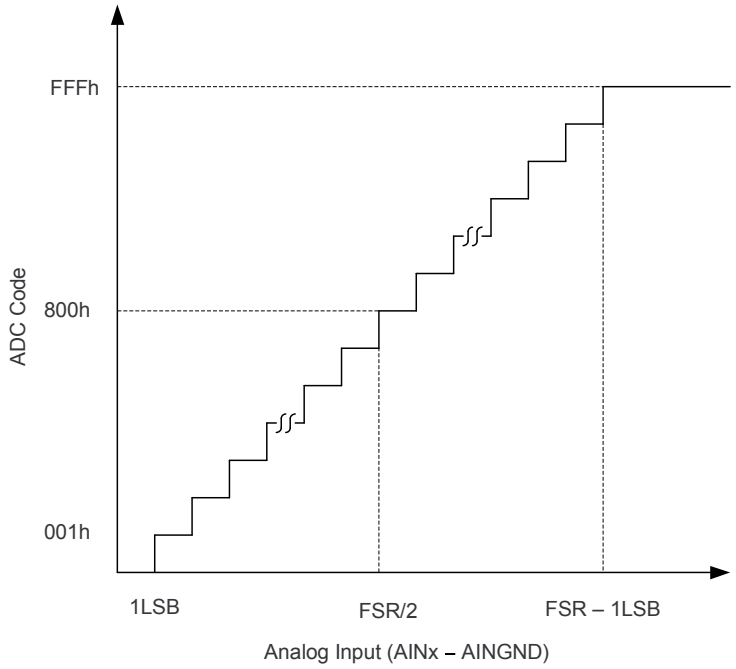

Figure 77. Transfer Function for Unipolar Signal Ranges

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AL_PD: USER-CONFIGURABLE PIN

The ADS8634/8 feature a user-configurable AL_PD pin. This pin can either be configured as an alarm output (AL) or as a power-down control pin ($\overline{PD}$). Refer to the *Page 0, Register Descriptions for the ADS8638* and *Page 0, Register Descriptions for the ADS8634* sections for details.

When programmed as an alarm output, an active-high alarm is flagged on this pin if there is a high or low alarm on any channel. The *Alarm Functionality* section describes the pin details.

When programmed as $\overline{PD}$, the AL_PD pin functions as an active-low power-down input pin. Powering down through this pin is asynchronous. The devices power down immediately after the pin goes low. The *Power-Down Functionality* section describes the pin details.

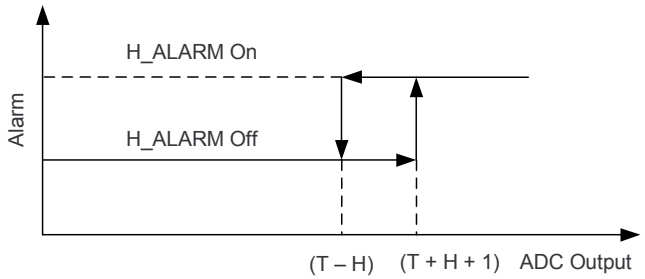
This pin is configured as a $\overline{PD}$ input by default after power-on or reset.

Alarm Functionality

The ADS8634/8 output an active-high alarm on the AL_PD pin when it is programmed as an AL. AL is synchronous and changes its state on the 16th SCLK rising edge. A high level on AL indicates there is an active alarm on one or more channels. This pin can be wired to interrupt the host input. When an alarm interrupt is received, the alarm flag registers are read to determine which channels have an alarm.

The ADS8634/8 feature independently-programmable alarms for each channel. There are two alarms per channel (low and high alarm) and each alarm threshold has a separate hysteresis setting.

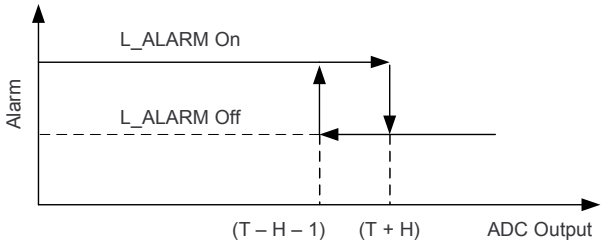
The ADS8634/8 set a high alarm when the digital output for a particular channel exceeds the high alarm upper limit (high alarm threshold *T* + hysteresis *H*). The alarm resets when the digital output for the channel is less than or equal to the high alarm lower limit (high alarm T – H). This function is shown in Figure 78.



NOTE: T = alarm threshold and H = hysteresis.

Figure 78. High-Alarm Hysteresis

Similarly, the lower alarm is triggered when the digital output for a particular channel falls below the low alarm lower limit (low alarm threshold T – H). The alarm resets when the digital output for the channel is greater than or equal to the low alarm higher limit (low alarm T + H). This function is shown in Figure 79.



NOTE: T = alarm threshold and H = hysteresis.

Figure 79. Low-Alarm Hysteresis

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Figure 80 shows a functional block diagram for a single-channel alarm. For each high and low alarm there are two flags: Active Alarm Flag and Tripped Alarm Flag; refer to the *Alarm Flags for the ADS8638 (Read-Only)* and *Alarm Flags for the ADS8634 (Read-Only)* sections for more details. The active alarm flag is triggered when an alarm condition is encountered for a particular channel; the active alarm flag resets when the alarm shuts off. A tripped alarm flag sets an alarm condition in the same manner as it does for an active alarm flag; however, it remains latched and resets only when the appropriate alarm flag register is read.

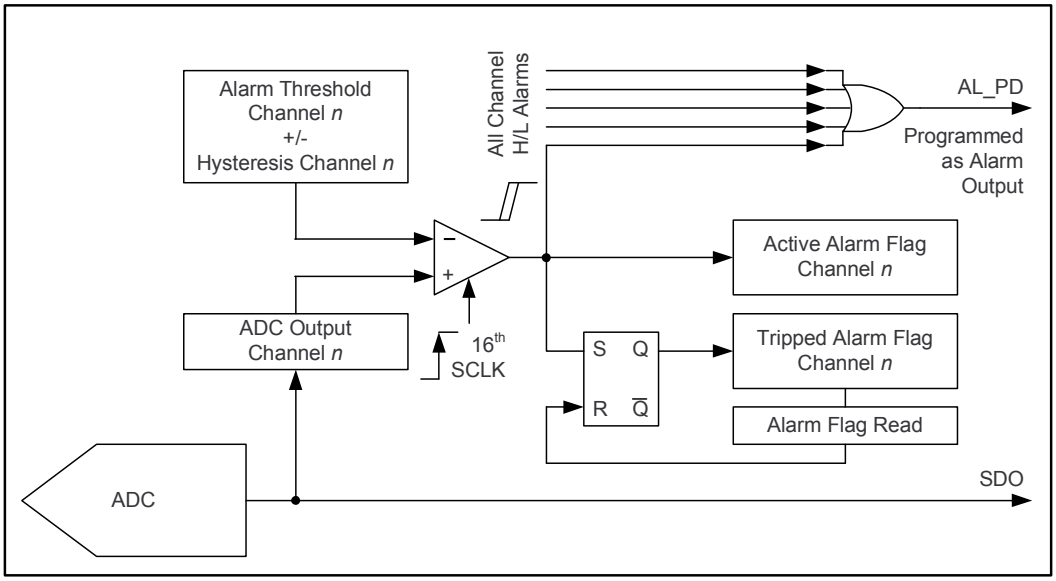

Figure 80. Alarm Functionality

Power-Down Functionality

The ADS8634/8 feature a power-down/up control through the programmable AL_PD pin or the channel sequencing control registers; see the *Channel Sequencing Control Registers for the ADS8638* and *Channel Sequencing Control Registers for the ADS8634* sections for more details. This feature is extremely useful for saving power while running the ADS8634/8 at a slower speed, or for acquiring data at full-speed in bursts and then waiting in a power-down state for the next acquisition start event. Figure 81 through Figure 84 describe entry to and exit from the power-down state.

The AL_PD pin can be programmed as a power-down control pin. The AL_PD pin, when programmed as $\overline{PD}$, is shown in Figure 81. A low on AL_PD powers down the device immediately; this action is asynchronous operation. Data on DOUT are not valid when the device is in a power-down state.

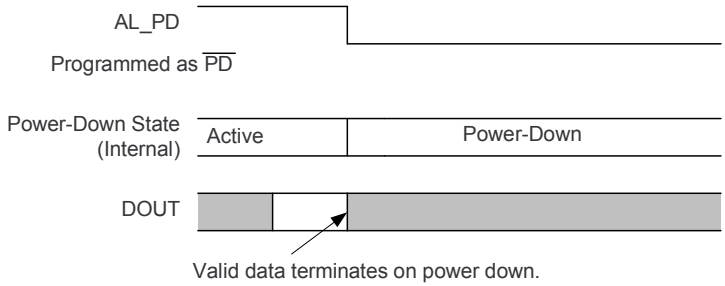

Figure 81. Power-Down Using the AL_PD Pin

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A high level on AL_PD acts as a power-up request and the power-up sequence begins on the next $\overline{CS}$ falling edge. The device is active after $t_{d(PWRUP)}$. The first valid acquisition initiates in the first data frame (with a $\overline{CS}$ falling edge) after a power-up delay. The first valid data are presented in the second data frame after the device attains an active state, as shown in Figure 82.

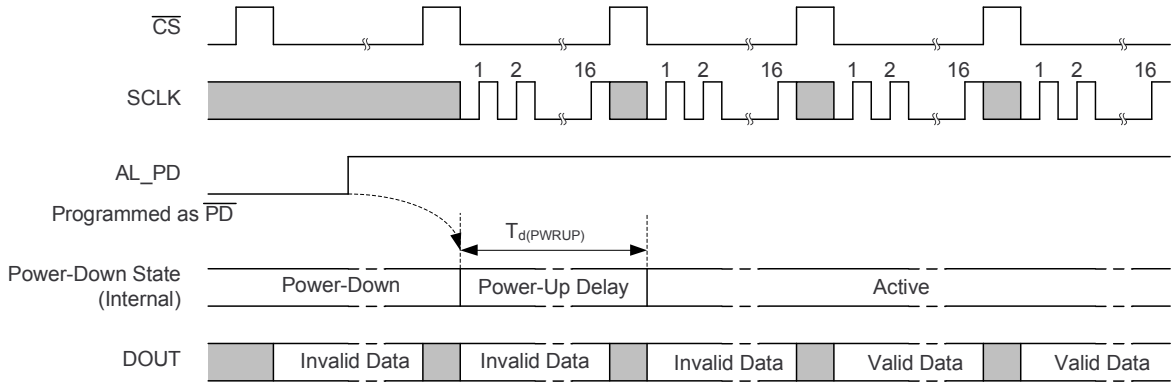

Figure 82. Power-Up Via the AL_PD Pin

The power-down/up operation can also be controlled with register settings. See the *Channel Sequencing Control Registers for the ADS8638* and *Channel Sequencing Control Registers for the ADS8634* sections for details. Figure 83 illustrates power-down and power-up commands for quick reference.

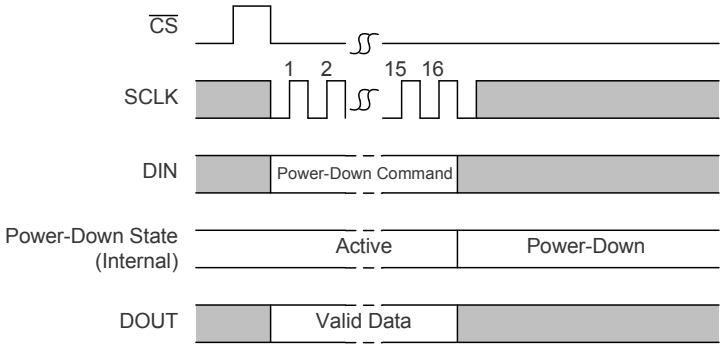

Figure 83. Power-Down Via Register Write

After receiving a valid power-down command, the device enters a power-down state on 16th SCLK falling edge. An example of this command is given in Table 6.

Table 6. Power-Down Command Example

	REGISTER ADDRESS							RD/$\overline{WR}$	DATA							
PIN	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DIN	0	0	0	0	1	0	X	0	0	X	X	X	1	1	1	X
	Auto/manual sequence							$\overline{W}$	0	X	X	X	Power-down			X

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The serial interface is active even during a device power-down state. Commands can be issued via the DIN pin during a power-down state.

A power-up command (through DIN) is acknowledged on the next $\overline{CS}$ falling edge and a power-up sequence initiates. An example of this command is given in Table 7. The device is in an active state after $t_{d(PWRUP)}$ and initiates a valid acquisition in the first data frame (initiated with a $\overline{CS}$ falling edge) after a power-up delay. The first valid data are presented in the second data frame after the device attains an active state, as shown in Figure 84.

Table 7. Power-Up Command Example

PIN	REGISTER ADDRESS							RD/$\overline{WR}$	DATA							
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DIN	0	0	0	0	1	0	X	0	0	X	X	X	Any combination from 000 to 110, except 111			X
	Auto/manual sequence							$\overline{W}$	0	X	X	X	Power-up			X

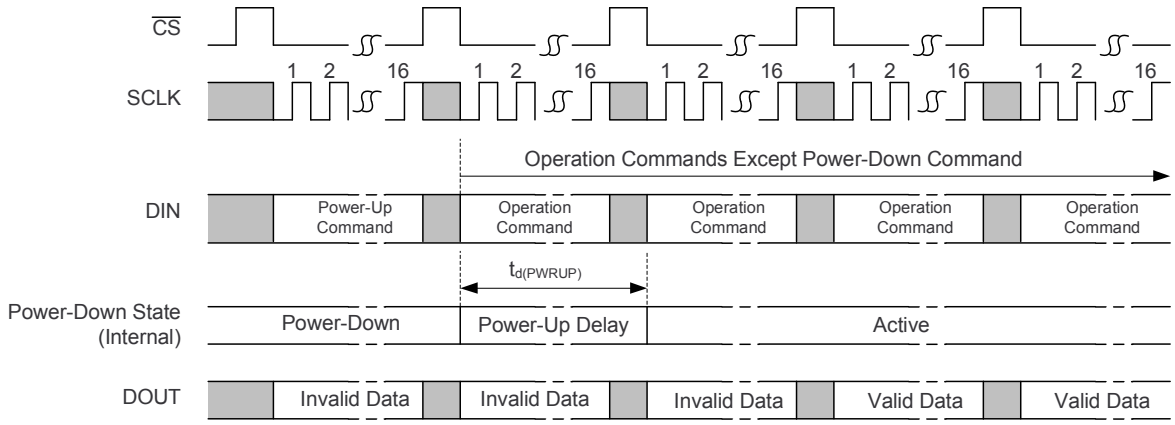

Figure 84. Power-Up Via Register Write

Use only one method (DIN pin or register settings) for power-down/up control. Do not combine these two methods or the results may be confusing. Do not issue a power-down command through DIN while using the AL_PD pin. Similarly, do not pull the AL_PD pin low while using the register write method for power-down/up control.

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DEVICE OPERATION

The ADS8634/8 are 12-bit, 4-/8-channel devices. Each frame begins with a $\overline{CS}$ falling edge. The ADS8634/8 sample the input signal from the selected channel on the $\overline{CS}$ falling edge and initiate conversion. SCLK is used for conversion and data are output on the DOUT line while conversion is in process. The 16-bit data word contains a 4-bit channel address followed by the 12-bit conversion result in MSB-first format. The MSB of the 4-bit channel address is output on the $\overline{CS}$ falling edge; the remaining address bits are clocked out serially for three SCLK falling edges. The MSB of the 12-bit conversion result is output on the fourth SCLK falling edge. Afterwards, the next lower data bits are ouput serially on every subsequen SCLK falling edge. Each data bit can be read (latched) immediately on the next SCLK falling edge from the SCLK falling edge on which the respective data bits are output. For example, if the MSB of a 12-bit data word is output on the fourth SCLK falling edge then the same word can be latched on the fifth SCLK falling edge. Refer to the *Hold time*, *SCLK falling to DOUT valid*, and *Delay time, SCLK falling to DOUT* parameters in the *Timing Requirements* section.

The 16-bit word is read on the DIN pin while the data are output on the DOUT pin. DIN data are latched on every SCLK rising edge, starting with the first clock, as shown in Figure 85.

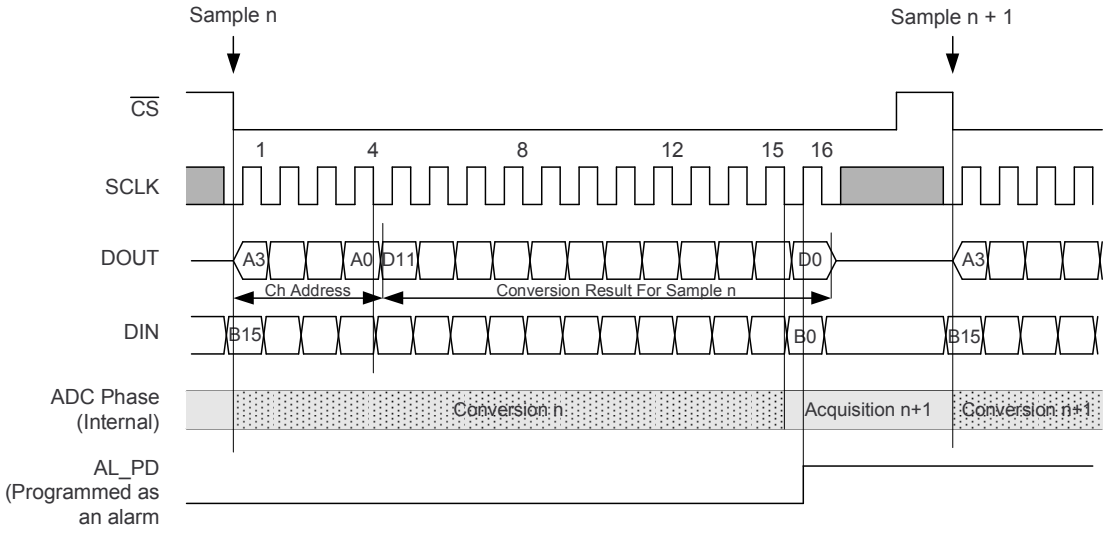

Figure 85. ADS8634/8 Operation

Device configuration and operation mode are controlled through register settings. It is recommended to write to the configuration registers after powering on the device. The configuration information is retained until the devices are powered off or reset. Note that powering down the device with either the AL_PD pin or a register write does not erase the device configuration.

The ADS8634/8 feature an AL_PD pin that functions as a alarm output/power-down pin. The pin can be programmed as an alarm output (AL) or it can be programmed as a power-down control pin ($\overline{PD}$). When AL_PD is programmed as an alarm output, it is refreshed on every 16th SCLK rising edge.

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CHANNEL SEQUENCING MODES

The ADS8634/8 offer two channel sequencing modes: auto and manual. In auto-scan mode, the channel number automatically increments every frame. In manual mode, the channel is selected for every frame of a register write. The analog inputs can be selected for an automatic scan with a register setting. The device automatically scans only the selected analog inputs in ascending order.

The auto-mode sequence can be reset at any time during an automatic scan (refer to the *Auto* register in the *PAGE-0 Register Map for the ADS8638* section). When the reset command has been received, the ongoing auto-mode sequence is reset and restarts it from the lowest selected channel in the sequence.

Figure 86 shows the DIN command sequence for transitions from auto to manual mode. Figure 87 shows the DIN command sequence for transitions from manual to auto-scan mode. Note that each DIN command is executed on the next $\overline{CS}$ falling edge.

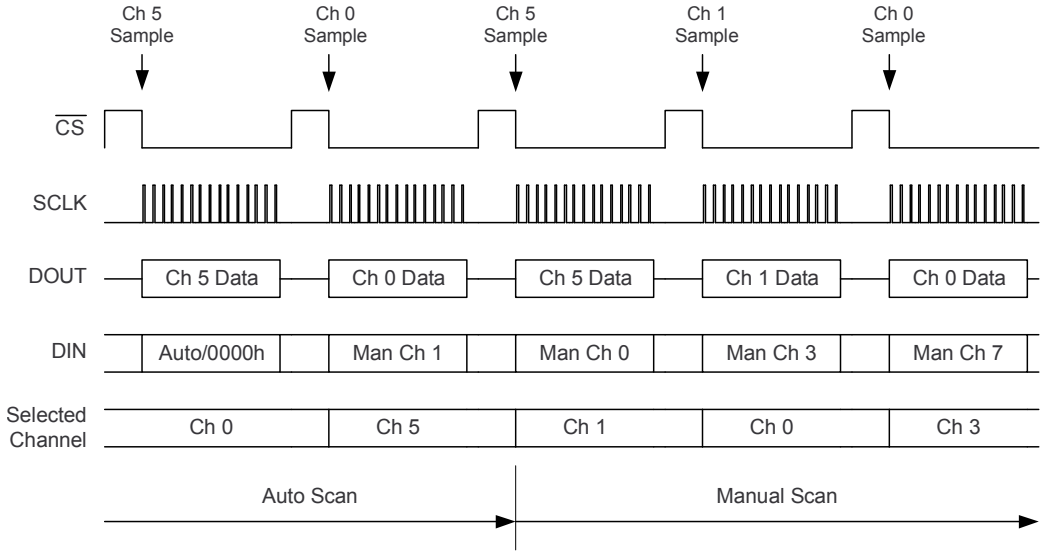

Figure 86. Transition from Auto to Manual Mode (Channels 0 and 5 are selected for auto sequence)

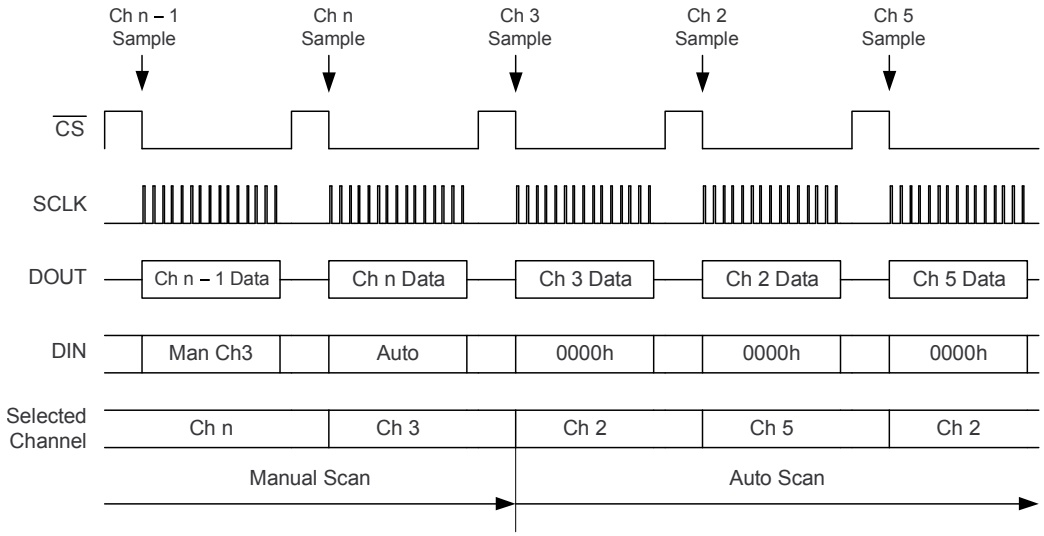

Figure 87. Transition from Manual to auto-scan mode (Channels 2 and 5 are selected for auto sequence)

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DEVICE TEMPARATURE READ

The ADS8634/8 feature an internal temperature sensor. The device temperature can be read at any time during any scan. It is essential to enable (power-up) the internal temperature at least one cycle before selecting the temperature sensor for the device temperature measurement. The temperature sensor must be deselected after temperature measurement. The device resumes the channel sequence from where it left the scan after deselection of the temperature sensor. Do not disable (power-down) the temperature sensor before it is deselected. Figure 88 illustrates a typical command sequence for device temperature measurement during an auto scan.

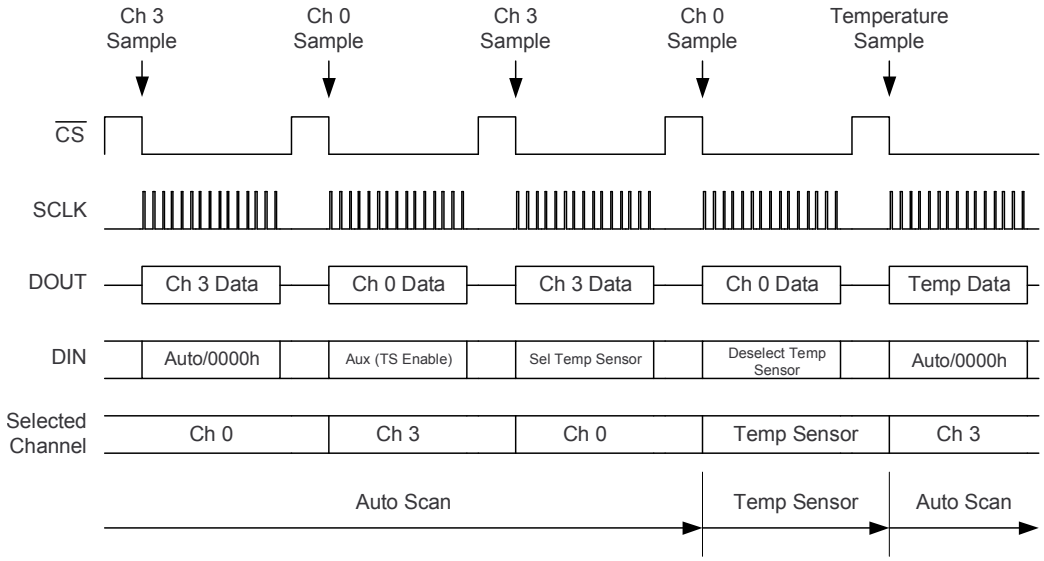

Figure 88. Reading Temperature During Auto Scan (Channels 0 and 3 are selected for auto sequence)

SPI INTERFACE

The ADS8634/8 employ a four-wire SPI-compatible interface. Apart from the interface, $\overline{CS}$ and SCLK also perform an ADC control function.

The data frame is synchronized with the $\overline{CS}$ falling edge. A low level on $\overline{CS}$ releases the DOUT pin from three-state and the ADC conversion results are output on the DOUT line. Data bits are clocked out on the falling edges of SCLK. The ADS8634/8 sample the analog input signal on the falling edge of $\overline{CS}$ and conversion is performed using SCLK.

DOUT is the serial data output line. Depending on register settings,the ADC conversion results are output along with the selected channel address or register data on the DOUT pin. The data output frame always consists of 16 bits. The SDO line goes to three-state after all the 16-bits of data frame are output or after $\overline{CS}$ goes high.

DIN is a serial data input line. It is used to program various registers for either device configuration or for dynamic changes applicable on the next immediate $\overline{CS}$ falling edge.

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DOUT DATA FORMAT

The device outputs 16-bit data in every cycle. Table 8 shows the DOUT data format.

Table 8. DOUT Data Format

	CHANNEL ADDRESS				CONVERSION RESULT											
PIN	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOUT	ADDR 3	ADDR 2	ADDR 1	ADDR 0	D11 (MSB)	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0 (LSB)

Bit Description for the ADS8638 DOUT Data

Bits[15:12] **Channel/temperature sensor address**

These bits represent the adress of channel or temperature sensor.

0000 = Channel 0
0001 = Channel 1
0010 = Channel 2
0011 = Channel 3
0100 = Channel 4
0101 = Channel 5
0110 = Channel 6
0111 = Channel 7
1111 = Temperature sensor

Bits[11:0] **Conversion result for the channel/temperature sensor represented by bits[15:12], in MSB-first format**

Bit Description for the ADS8634 DOUT Data

Bits[15:12] **Channel/temperature sensor address**

These bits represent the adress of channel or temperature sensor.

000X = Channel 0
001X = Channel 1
010X = Channel 2
011X = Channel 3
1111 = Temperature sensor

Bits[11:0] **Conversion result for the channel/temperature sensor represented by bits[15:12], in MSB-first format**

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DIN DATA FORMAT (SPI COMMAND WORD)

Device registers can be written to and read from. There must be a minimum of 16 SCLKs after the $\overline{CS}$ falling edge for any read or write operation. The device receives the command (as shown in Table 9 and Table 10) through DIN where the first seven bits (bits[15:9]) represent the register address and the eighth bit (bit 8) is the read/write instruction. For a write cycle, the next eight bits (bits[7:0]) in the DIN are the desired data for the addressed register (Table 9). For a read cycle, the next eight bits (bits[7:0]) in the DIN are *don't care*. DOUT outputs the 8-bit data from the addressed register (Table 10) during these eight clocks, corresponding to bits[7:0].

Table 9. Write Cycle Command Word

	REGISTER ADDRESS							RD/WR	DATA							
PIN	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DIN	ADDR 6	ADDR 5	ADDR 4	ADDR 3	ADDR 2	ADDR 1	ADDR 0	R/$\overline{W}$	DIN7	DIN6	DIN5	DIN4	DIN3	DIN2	DIN1	DIN0

Table 10. Read Cycle Command Word

	REGISTER ADDRESS							RD/WR	DATA							
PIN	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DIN	ADDR 6	ADDR 5	ADDR 4	ADDR 3	ADDR 2	ADDR 1	ADDR 0	R/$\overline{W}$	X	X	X	X	X	X	X	X
DOUT	X	X	X	X	X	X	X	X	DOUT 7	DOUT 6	DOUT 5	DOUT 4	DOUT 3	DOUT 2	DOUT 1	DOUT 0

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SPI REGISTER WRITE CYCLE

Figure 89 shows a timing diagram of the SPI write cycle. The device executes the command on the first $\overline{CS}$ falling edge after a command write cycle. The only exception to this command execution timing is the power-down command. The power-down command (through a register write) is executed on the 16th falling edge of SCLK. This falling edge occurs immediately after the last command bit is written to the device.

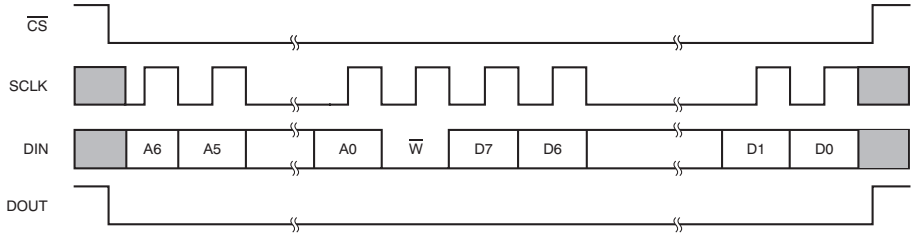

Figure 89. Write Cycle

SPI REGISTER READ CYCLE

Figure 90 shows a timing diagram of the SPI read cycle.

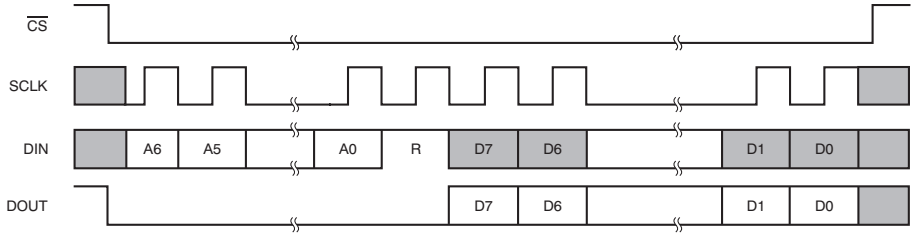

Figure 90. Read Cycle

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REGISTER MAP: ADS8638

The ADS8638 internal registers are mapped in two pages: page 0 and page 1. Page 0 is selected by default at power-up and after reset. Any register read/write operation performed while on page 0 addresses the page 0 registers. Writing 01h to register address 7Fh selects page 1 for any further register operations.

Page 0 registers are used to select the channel sequencing mode, program the configuration registers, and read the alarm flags. Page 1 resisters are used to program alarm thresholds for each channel and for the temperature sensor. Table 11 details page 0 and Table 12 details page 1.

Table 11. ADS8638 Page 0 Register Map

REGISTER	REGISTER ADDRESS BITS[15:9]	DEFAULT VALUE(1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Channel Sequencing Control Registers										
Manual	04h	00h	0	Channel Select[2:0]			Range Select[2:0]			Sel Temp Sensor
Auto	05h	00h	Reset-Seq	0	0	0	Range Select[2:0]			Sel Temp Sensor
Holding the DIN line low continuously (equivalent to writing '0' to all 16 bits) during device operation as per Figure 85 continues device operation in the last selected mode (auto or manual).										
Configuration Registers										
Reset-Device	01h	00h	0	0	0	0	0	0	0	Reset-Dev
Aux-Config	06h	08h	0	0	0	0	AL_PD Control	Int V_{REF} Enable	Temp Sensor Enable	0
Auto-Md Ch-Sel	0Ch	00h	Sel Ch0	Sel Ch1	Sel Ch2	Sel Ch3	Sel Ch4	Sel Ch5	Sel Ch6	Sel Ch7
Ch0-1 Range	10h	11h	0	Range Select Ch0[2:0]			0	Range Select Ch1[2:0]		
Ch2-3 Range	11h	11h	0	Range Select Ch2[2:0]			0	Range Select Ch3[2:0]		
Ch4-5 Range	12h	11h	0	Range Select Ch4[2:0]			0	Range Select Ch5[2:0]		
Ch6-7 Range	13h	11h	0	Range Select Ch6[2:0]			0	Range Select Ch7[2:0]		
Alarm Flag Registerss (Read-Only)										
Temp-Flag	20h	00h	Tripped Alarm Flag Temperature Low	Tripped Alarm Flag Temperature High	Active Alarm Flag Temperature Low	Active Alarm Flag Temperature High	0	0	0	0
Ch0-3 Tripped-Flag	21h	00h	Tripped Alarm Flag Ch0 Low	Tripped Alarm Flag Ch0 High	Tripped Alarm Flag Ch1 Low	Tripped Alarm Flag Ch1 High	Tripped Alarm Flag Ch2 Low	Tripped Alarm Flag Ch2 High	Tripped Alarm Flag Ch3 Low	Tripped Alarm Flag Ch3 High
Ch0-3 Active-Flag	22h	00h	Active Alarm Flag Ch0 Low	Active Alarm Flag Ch0 High	Active Alarm Flag Ch1 Low	Active Alarm Flag Ch1 High	Active Alarm Flag Ch2 Low	Active Alarm Flag Ch2 High	Active Alarm Flag Ch3 Low	Active Alarm Flag Ch3 High
Ch4-7 Tripped-Flag	23h	00h	Tripped Alarm Flag Ch4 Low	Tripped Alarm Flag Ch4 High	Tripped Alarm Flag Ch5 Low	Tripped Alarm Flag Ch5 High	Tripped Alarm Flag Ch6 Low	Tripped Alarm Flag Ch6 High	Tripped Alarm Flag Ch7 Low	Tripped Alarm Flag Ch7 High
Ch4-7 Active-Flag	24h	00h	Active Alarm Flag Ch4 Low	Active Alarm Flag Ch4 High	Active Alarm Flag Ch5 Low	Active Alarm Flag Ch5 High	Active Alarm Flag Ch6 Low	Active Alarm Flag Ch6 High	Active Alarm Flag Ch7 Low	Active Alarm Flag Ch7 High
Page Selection Register										
Page	7Fh	00h	0	0	0	0	0	0	0	Page Addr

(1) All registers are reset to the default values at power-on or at device reset using the register settings method.

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Table 12. ADS8638 Page 1 Register Map

REGISTER	REGISTER ADDRESS BITS[15:9]	DEFAULT VALUE(1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Alarm Threshold Registers										
TLA MSB	00h	00h	TLA Hysteresis[3:0]				TLA[11:8]			
TLA LSB	01h	00h	TLA[7:0]							
THA MSB	02h	00h	THA Hysteresis[3:0]				THA[11:8]			
THA LSB	03h	00h	THA[7:0]							
Ch0LA MSB	04h	00h	Ch0-LA Hysteresis[3:0]				Ch0-LA[11:8]			
Ch0LA LSB	05h	00h	Ch0-LA[7:0]							
Ch0HA MSB	06h	00h	Ch0-HA Hysteresis[3:0]				Ch0-HA[11:8]			
Ch0HA LSB	07h	00h	Ch0-HA[7:0]							
Ch1LA MSB	08h	00h	Ch1-LA Hysteresis[3:0]				Ch1-LA[11:8]			
Ch1LA LSB	09h	00h	Ch1-LA[7:0]							
Ch1 HA MSB	0Ah	00h	Ch1-HA Hysteresis[3:0]				Ch1-HA[11:8]			
Ch1 HA LSB	0Bh	00h	Ch1-HA[7:0]							
Ch2 LA MSB	0Ch	00h	Ch2-LA Hysteresis[3:0]				Ch2-LA[11:8]			
Ch2 LA LSB	0Dh	00h	Ch2-LA[7:0]							
Ch2 HA MSB	0Eh	00h	Ch2-HA Hysteresis[3:0]				Ch2-HA[11:8]			
Ch2 HA LSB	0Fh	00h	Ch2-HA[7:0]							
Ch3 LA MSB	10h	00h	Ch3-LA Hysteresis[3:0]				Ch3-LA[11:8]			
Ch3 LA LSB	11h	00h	Ch3-LA[7:0]							
Ch3 HA MSB	12h	00h	Ch3-HA Hysteresis[3:0]				Ch3-HA[11:8]			
Ch3 HA LSB	13h	00h	Ch3-HA[7:0]							
Ch4 LA MSB	14h	00h	Ch4-LA Hysteresis[3:0]				Ch4-LA[11:8]			
Ch4 LA LSB	15h	00h	Ch4-LA[7:0]							
Ch4 HA MSB	16h	00h	Ch4-HA Hysteresis[3:0]				Ch4-HA[11:8]			
Ch4 HA LSB	17h	00h	Ch4-HA[7:0]							
Ch5 LA MSB	18h	00h	Ch5-LA Hysteresis[3:0]				Ch5-LA[11:8]			
Ch5 LA LSB	19h	00h	Ch5-LA[7:0]							
Ch5 HA MSB	1Ah	00h	Ch5-HA Hysteresis[3:0]				Ch5-HA[11:8]			
Ch5 HA LSB	1Bh	00h	Ch5-HA[7:0]							
Ch6 LA MSB	1Ch	00h	Ch6-LA Hysteresis[3:0]				Ch6-LA[11:8]			
Ch6 LA LSB	1Dh	00h	Ch6-LA[7:0]							
Ch6 HA MSB	1Eh	00h	Ch6-HA Hysteresis[3:0]				Ch6-HA[11:8]			
Ch6 HA LSB	1Fh	00h	Ch6-HA[7:0]							
Ch7 LA MSB	20h	00h	Ch7-LA Hysteresis[3:0]				Ch7-LA[11:8]			
Ch7 LA LSB	21h	00h	Ch7-LA[7:0]							
Ch7 HA MSB	22h	00h	Ch7-HA Hysteresis[3:0]				Ch7-HA[11:8]			
Ch7 HA LSB	23h	00h	Ch7-HA[7:0]							
Page Selection Register										
Page	7Fh	00h	0	0	0	0	0	0	0	Page Addr

(1) All registers are reset to the default values at power-on or at device reset using the register settings method.

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PAGE 0 REGISTER DESCRIPTIONS: ADS8638

This section provides bit-by-bit descriptions of each page 0 register.

Channel Sequencing Control Registers for the ADS8638

There are two modes for channel sequencing: auto and manual mode. In auto-scan mode, the device automatically scans the preselected channels in sequential order with a new channel selected for every conversion. In manual mode, the channel is manually selected for the next conversion. In both modes, the preselected signal range is considered for each channel independently. Note that the range can be temporarily overriden.

Manual: Manual Mode Register (Address = 04h; Page 0)

7	6	5	4	3	2	1	0
0	Channel Select[2:0]			Range Select[2:0]			Sel Temp Sensor

This register selects device operation in manual scan mode, selects the channel for the next conversion, allows the preselected signal range to be temporarily overriden for the next conversion, and enables the device temperature to be read.

Bit 7 **Must always be set to '0'**

Bits[6:4] **Channel Select[2:0]**

These bits select the channel for acquisition during the next frame.
For example, if this register is written in frame number *n*, then the addressed channel signal is acquired in frame number *n + 1* and the conversion result is available in frame number *n + 2*.

000 = Channel 0
001 = Channel 1
010 = Channel 2
011 = Channel 3
100 = Channel 4
101 = Channel 5
110 = Channel 6
111 = Channel 7

Bits[3:1] **Range Select[2:0]**

These bits select the signal range for the channel acquired in the next frame.
For example, if this register is written in frame number *n*, then the selected range is applicable for frame number *n + 1*. This is a dynamic range selection and overrides selection through the configuration registers (address 10h to 13h, page 0) only for the next frame.

000 = Ranges as selected through the configuration registers (address 10h to 13h, page 0)
001 = Range is set to ±10V
010 = Range is set to ±5V
011 = Range is set to ±2.5V
100 = Reserved; do not use this setting
101 = Range is set to 0V to 10V
110 = Range is set to 0V to 5V
111 = Powers down the device immediately after the 16th SCLK falling edge

Bit 0 **Sel Temp Sensor**

This bit selects the temperature sensor for acquisition in the next frame. This selection overrides channel selection through bits[6:4]. Range selection is not applicable for the temperature sensor.

0 = Next conversion as per selection through bits[3:1]
1 = The temperature sensor is selected for acquisition in the next frame

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Auto: Auto-Scan Mode Register (Address = 05h; Page 0)

7	6	5	4	3	2	1	0
Reset-Seq	0	0	0	Range Select[2:0]			Sel Temp Sensor

This register selects device operation in auto-scan mode, allows the preselected signal range to be temporarily overriden for the next conversion, and enables the device temperature to be read.

Bit 7 **Reset-Seq**

This bit resets the auto-mode sequence counter.
The counter is reset to the lowest channel number in the selected sequence.
For example, if the Auto-Md Ch-Sel register is programmed to *01101100* (the auto-mode sequence channels are 2, 3, 5, 6, 2, 3, 5, 6…2, 3, 5, 6), and, if the Reset-Seq bit is programmed to '1' in frame *n* while channel 3 is sampled, then the auto-mode sequence counter is reset to channel 2 in frame *n* + *1*. This setting means that channel 2 is sampled instead of channel 5 in frame *n* + *1*.

0 = No reset (continue the sequence from the present channel number)
1 = Reset the channel sequncing counter

Bits[6:4] **Must always be set to '0'**

Bits[3:1] **Range Select[2:0]**

These bits select the signal range for the channel acquired in the next frame.
For example, if this register is written in frame number *n*, then the selected range is applicable for frame number *n* + *1*. This is a dynamic range selection and overrides selection through the configuration registers (address 10h to 13h, page 0) only for the next frame.

000 = Ranges as selected through the configuration registers (address 10h to 13h)
001 = Range is set to ±10V
010 = Range is set to ±5V
011 = Range is set to ±2.5V
100 = Reserved; do not use this setting
101 = Range is set to 0V to 10V
110 = Range is set to 0V to 5V
111 = Powers down the device immediately after the 16th SCLK falling edge

Bit 0 **Sel Temp Sensor**

This bit selects the temperature sensor for acquisition in the next frame.
This selection overrides the channel selection through the auto sequence only for the next frame. The auto-mode sequence continues from where it was interrupted after the temperature sensing frame.
For example, if the programmed auto sequence is channels 0, 1, 3, 0, 1, 3…0, 1, 3, and if the temperature sensor is selected in frame number *n* while channel 0 is sampled, then the temperature sensor is sampled in frame *n* + *1*. The auto sequence resumes from frame *n* + *2* sampling channel 1.
Range selection is not applicable for the temperature sensor.

0 = Next conversion as selected through bits[3:1]
1 = The temperature sensor is selected for acquisition in the next frame

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Continued Operation in the Selected Mode for the ADS8638

Holding the DIN line low continuously (equivalent to writing '0' to all 16 bits) during device operation as per Figure 85, continues device operation in the last selected mode (auto or manual). The device follows the range selection from the configuration registers (address 10h to 13h). The the internal temperature sensor continues to be read if the temperature sensor was selected during the last auto/manual mode frame.

Configuration Registers for the ADS8638

The configuration registers allow device configuration (signal range selection for individual channels, selection of channels for auto sequence, enabling/disabling of the internal reference and temperature sensor, and configuration of the AL_PD pin as either an alarm output or a power-down input). All registers can be reset to the default values using the configuration register.

Reset-Device: Device Reset Register (Address = 01h; Page 0)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	Reset-Dev

This register resets the device and assigns default values to all internal registers. The reset value for this register is 00h; as a result, this bit is self-clearing.

Bits[7:1] **Must always be set to '0'**

Bit 0 **Reset-Dev**

This bit initiates a software reset immediately after the 16th SCLK falling edge.
All registers in the device are assigned the reset values mentioned in Table 11 and Table 12.

0 = No reset
1 = Device reset

Aux-Config: Device Auxiliary Blocks Enable/Disable Control Register (Address = 06h; Page 0)

7	6	5	4	3	2	1	0
0	0	0	0	AL_PD Control	Int V_{REF} Enable	Temp Sensor Enable	0

This register controls the functionality of the AL_PD pin and enables/disables blocks such as the internal reference and internal temperature sensor.

Bits[7:4] **Must always be set to '0'**

Bit 3 **AL_PD Control**

This bit controls the functionality of the AL_PD pin.

0 = AL_PD pin functions as an alarm output pin
1 = AL_PD pin functions as a power-down control pin

Bit 2 **Int V_{REF} Enable**

This bit powers up the internal V_{REF}.

0 = Internal reference block is powered down at the next frame
1 = Internal reference block is powered up at the next frame

Bit 1 **Temp Sensor Enable**

This bit powers up the internal temperature sensor.

0 = Internal temperature sensor block is powered down from the next frame
1 = Internal temperature sensor block is powered up from the next frame

Bit 0 **Must always be set to'0'**

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Auto-Md Ch-Sel: Channel Selection Register for Auto-Scan Mode (Address = 0Ch; Page 0)

7	6	5	4	3	2	1	0
Sel Ch0	Sel Ch1	Sel Ch2	Sel Ch3	Sel Ch4	Sel Ch5	Sel Ch6	Sel Ch7

This register selects the channels for the auto-mode sequence. The device scans only the selected channels in ascending order during auto-scan mode, starting with the lowest channel selected. For example, if the Auto-Md Ch-Sel register is programmed to *01100100*, then the auto-mode sequence is channels 2, 5, 6, 2, 5, 6…2, 5, 6. In this case, the sequence always starts at channel 2. Channel 0 is selected if this register is programmed to *00000000*.

Bit 7 **Sel Ch0**

This bit selects channel 0.

0 = Channel 0 not selected
1 = Channel 0 selected

Bit 6 **Sel Ch1**

This bit selects channel 1.

0 = Channel 1 not selected
1 =Channel 1 selected

Bit 5 **Sel Ch2**

This bit selects channel 2.

0 = Channel 2 not selected
1 = Channel 2 selected

Bit 4 **Sel Ch3**

This bit selects channel 3.

0 = Channel 3 not selected
1 = Channel 3 selected

Bit 3 **Sel Ch4**

This bit selects channel 4.

0 = Channel 4 not selected
1 = Channel 4 selected

Bit 2 **Sel Ch5**

This bit selects channel 5.

0 = Channel 5 not selected
1 = Channel 5 selected

Bit 1 **Sel Ch6**

This bit selects channel 6.

0 = Channel 6 not selected
1 = Channel 6 selected

Bit 0 **Sel Ch7**

This bit selects channel 7.

0 = Channel 7 not selected
1 = Channel 7 selected

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Ch0-1 Range to Ch6-7 Range: Range Selection Registers for Channels 0 to 7 (Address = 10h to 13h; Page 0)

REGISTER	ADDRESS ON PAGE 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Ch0-1 Range	10h	0	Range Select Ch0[2:0]			0	Range Select Ch1[2:0]		
Ch2-3 Range	11h	0	Range Select Ch2[2:0]			0	Range Select Ch3[2:0]		
Ch4-5 Range	12h	0	Range Select Ch4[2:0]			0	Range Select Ch5[2:0]		
Ch6-7 Range	13h	0	Range Select Ch6[2:0]			0	Range Select Ch7[2:0]		

A selection of signal ranges are featured for each channel. The selected range is automatically assigned for a channel during conversion, regardless of the channel scan mode (auto or manual). These registers (Ch0-1 Range to Ch6-7 Range) allow for range selection of all channels.

Bit 7 **Must always be set to '0'**

Bits[6:4] **Range Select Chn[2:0]**

These bits select the signal range for channel *n*, where *n* is 0, 2, 4, or 6, depending on the register address.

000 = Reserved; do not use this setting
001 = Range is set to ±10V
010 = Range is set to ±5V
011 = Range is set to ±2.5V
100 = Reserved; do not use this setting
101 = Range is set to 0V to 10V
110 = Range is set to 0V to 5V
111 = Reserved; do not use this setting

Bit 3 **Must always be set to '0'**

Bits[2:0] **Range Select Chm[2:0]**

These bits select the signal range for channel *m*, where *m* is 1, 3, 5, or 7, depending on the register address.

000 = Reserved; do not use this setting
001 = Range is set to ±10V
010 = Range is set to ±5V
011 = Range is set to ±2.5V
100 = Reserved; do not use this setting
101 = Range is set to 0V to 10V
110 = Range is set to 0V to 5V
111 = Reserved; do not use this setting

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Alarm Flag Registers for the ADS8638 (Read-Only)

The alarm conditions related to individual channels are stored in these registers. The flags can be read when an alarm interrupt is received on the AL_PD pin. There are two types of flag for every alarm: active and tripped. The active flag is set to '1' under the alarm condition (when data cross the alarm limit) and remains so as long as the alarm condition persists. The tripped flag turns on the alarm condition similar to the active flag, but it remains set until it is read. This feature relieves the device from having to track alarms.

Temp Flag: Alarm Flags Register for Temperature Sensor (Address = 20h; Page 0)

7	6	5	4	3	2	1	0
Tripped Alarm Flag Temperature Low	Tripped Alarm Flag Temperature High	Active Alarm Flag Temperature Low	Active Alarm Flag Temperature High	0	0	0	0

The Temp Flag register stores the alarm flags for the temperature sensor. There are two alarm thresholds, and for each threshold there are two flags. An active alarm flag is enabled when an alarm is triggered (when data cross the alarm threshold) and remains enabled as long as the alarm condition persists. A tripped alarm flag is enabled in the same manner as an active alarm flag, but it remains latched until it is read.

Bit 7 **Tripped Alarm Flag Temperature Low**

This bit indicates the tripped low alarm flag status for the temperature sensor.

0 = No alarm detected
1 = Alarm detected

Bit 6 **Tripped Alarm Flag Temperature High**

This bit indicates the tripped high alarm flag status for the temperature sensor.

0 = No alarm detected
1 = Alarm detected

Bit 5 **Active Alarm Flag Temperature Low**

This bit indicates the active low alarm flag status for the temperature sensor.

0 = No alarm
1 = Alarm detected

Bit 4 **Active Alarm Flag Temperature High**

This bit indicates the active-high alarm flag status for the temperature sensor.

0 = No alarm detected
1 = Alarm detected

Bits[3:0] **Always read '0'**

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Ch0-3 Tripped-Flag to Ch4-7 Active-Flag: Alarm Flags Register for Channels 0 to 7 (Address = 21h to 24h; Page 0)

REGISTER	ADDRESS ON PAGE 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Ch0-3 Tripped-Flag	21h	Tripped Alarm Flag Ch0 Low	Tripped Alarm Flag Ch0 High	Tripped Alarm Flag Ch1 Low	Tripped Alarm Flag Ch1 High	Tripped Alarm Flag Ch2 Low	Tripped Alarm Flag Ch2 High	Tripped Alarm Flag Ch3 Low	Tripped Alarm Flag Ch3 High
Ch0-3 Active-Flag	22h	Active Alarm Flag Ch0 Low	Active Alarm Flag Ch0 High	Active Alarm Flag Ch1 Low	Active Alarm Flag Ch1 High	Active Alarm Flag Ch2 Low	Active Alarm Flag Ch2 High	Active Alarm Flag Ch3 Low	Active Alarm Flag Ch3 High
Ch4-7 Tripped-Flag	23h	Tripped Alarm Flag Ch4 Low	Tripped Alarm Flag Ch4 High	Tripped Alarm Flag Ch5 Low	Tripped Alarm Flag Ch5 High	Tripped Alarm Flag Ch6 Low	Tripped Alarm Flag Ch6 High	Tripped Alarm Flag Ch7 Low	Tripped Alarm Flag Ch7 High
Ch4-7 Active-Flag	24h	Active Alarm Flag Ch4 Low	Active Alarm Flag Ch4 High	Active Alarm Flag Ch5 Low	Active Alarm Flag Ch5 High	Active Alarm Flag Ch6 Low	Active Alarm Flag Ch6 High	Active Alarm Flag Ch7 Low	Active Alarm Flag Ch7 High

There are two alarm thresholds (high and low) per channel, with two flags for each threshold. An active alarm flag is enabled when an alarm is triggered (when data cross the alarm threshold) and remains enabled as long as the alarm condition persists. A tripped alarm flag is enabled in the same manner as an active alarm flag, but it remains latched until it is read. Registers 21h to 24h on page 0 store the active and tripped alarm flags for all eight channels.

Bits[7:0] **Active/Tripped Alarm Flag Chn High/Low**

Each individual bit indicates an active/tripped, high/low alarm flag status for each channel, as per the Alarm Flags Register for channels 0 to 7.

0 = No alarm detected
1 = Alarm detected

Page Selection Register for the ADS8638

The registers are arranged on two pages: page 0 and page 1. The page register selects the register page.

Page: Page Selection Register (Address = 7Fh; Page 0)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	Page Addr

Bits[7:1] **Must always be set to '0'**

Bit 0 **Page Addr**

This bit selects the page address.

0 = Selects page 0 for the next register read or write command; all register read/write operations after this are performed on the page 0 registers until page 1 is selected
1 = Selects page 1 for the next register read or write command; all register read/write operations after this are performed on the page 1 registers until page 0 is selected

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PAGE 1 REGISTER DESCRIPTIONS: ADS8638

This section provides bit-by-bit descriptions of each page 1 register. As described earlier, the device registers are mapped to two pages. Page 0 is selected by default at power-up and after reset. Page 1 can be selected by writing 01h to register address 7Fh. After selecting page 1, any register read/write action addresses the page 1 registers. Writing 00h to register address 7Fh selects page 0 for any further register operations.

Alarm Threshold Setting Registers for the ADS8638

The ADS8634/8 feature high and low alarms individually for the temperature sensor and each of the eight channels. Each alarm threshold is 12 bits wide with a 4-bit hysteresis. This 16-bit setting is accomplished through two 8-bit registers associated with every high/low alarm.

TLA MSB to THA LSB: Temperature Alarm Registers (Address = 00h to 03h; Page 1)

REGISTER	ADDRESS ON PAGE 1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TLA MSB		TLA Hysteresis[3:0]				TLA[11:8]			
TLA LSB		TLA[7:0]							
THA MSB		THA Hysteresis[3:0]				THA[11:8]			
THA LSB		THA[7:0]							

THA/LA MSB REGISTER

Bits[7:4] **THA/LA Hysteresis[3:0]**

These bits set the temperature high/low alarm hysteresis.

0000 = No hyeteresis
0001 = ±1LSB hystetesis
0010 to 1110 = ±2LSB to ±14LSB hystetesis
1111 = ±15LSB hystetesis

Bits[3:0] **THA/LA[11:8]**

These bits set the MSB nibble for the 12-bit temperature high/low alarm.
For example, the temperature high alarm threshold is AFFh when the THA MSB register (address 02h, page 1) setting is Ah and the THA LSB register (address 03h, page 1) register setting is FFh.

0000 = MSB nibble is 0h
0001 = MSB nibble is 1h
0010 to 1110 = MSB nibble is 2h to Eh
1111 = MSB nibble is Fh

THA/LA LSB REGISTER

Bits[7:0] **THA/LA[7:0]**

These bits set the LSB byte for the 12-bit temperature high alarm.
For example, the temperature low alarm threshold is F02h when the TLA LSB register (address 01h) setting is 02h and the TLS MSB register (address 00h, page 1) register setting is Fh.

0000 0000 = LSB byte is 0h
0000 0001 = LSB byte is 1h
0000 0010 to 1110 1111 = LSB byte is 02h to EFh
1111 1111 = LSB byte is FFh

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Ch0LA MSB to Ch7HA LSB: Channels 0 to 7 Alarm Registers (Address = 04h to 23h; Page 1)

REGISTER	ADDRESS ON PAGE 1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Ch0LA MSB	04h	Ch0-LA Hysteresis[3:0]				Ch0-LA[11:8]			
Ch0LA LSB	05h	Ch0-LA[7:0]							
Ch0HA MSB	06h	Ch0-HA Hysteresis[3:0]				Ch0-HA[11:8]			
Ch0HA LSB	07h	Ch0-HA[7:0]							
Ch1LA MSB	08h	Ch1-LA Hysteresis[3:0]				Ch1-LA[11:8]			
Ch1LA LSB	09h	Ch1-LA[7:0]							
Ch1HA MSB	0Ah	Ch1-HA Hysteresis[3:0]				Ch1-HA[11:8]			
Ch1HA LSB	0Bh	Ch1-HA[7:0]							
Ch2LA MSB	0Ch	Ch2-LA Hysteresis[3:0]				Ch2-LA[11:8]			
Ch2LA LSB	0Dh	Ch2-LA[7:0]							
Ch2HA MSB	0Eh	Ch2-HA Hysteresis[3:0]				Ch2-HA[11:8]			
Ch2HA LSB	0Fh	Ch2-HA[7:0]							
Ch3LA MSB	10h	Ch3-LA Hysteresis[3:0]				Ch3-LA[11:8]			
Ch3LA LSB	11h	Ch3-LA[7:0]							
Ch3HA MSB	12h	Ch3-HA Hysteresis[3:0]				Ch3-HA[11:8]			
Ch3HA LSB	13h	Ch3-HA[7:0]							
Ch4LA MSB	14h	Ch4-LA Hysteresis[3:0]				Ch4-LA[11:8]			
Ch4LA LSB	15h	Ch4-LA[7:0]							
Ch4HA MSB	16h	Ch4-HA Hysteresis[3:0]				Ch4-HA[11:8]			
Ch4HA LSB	17h	Ch4-HA[7:0]							
Ch5LA MSB	18h	Ch5-LA Hysteresis[3:0]				Ch5-LA[11:8]			
Ch5LA LSB	19h	Ch5-LA[7:0]							
Ch5HA MSB	1Ah	Ch5-HA Hysteresis[3:0]				Ch5-HA[11:8]			
Ch5HA LSB	1Bh	Ch5-HA[7:0]							
Ch6LA MSB	1Ch	Ch6-LA Hysteresis[3:0]				Ch6-LA[11:8]			
Ch6LA LSB	1Dh	Ch6-LA[7:0]							
Ch6HA MSB	1Eh	Ch6-HA Hysteresis[3:0]				Ch6-HA[11:8]			
Ch6HA LSB	1Fh	Ch6-HA[7:0]							
Ch7LA MSB	20h	Ch7-LA Hysteresis[3:0]				Ch7-LA[11:8]			
Ch7LA LSB	21h	Ch7-LA[7:0]							
Ch7HA MSB	22h	Ch7-HA Hysteresis[3:0]				Ch7-HA[11:8]			
Ch7HA LSB	23h	Ch7-HA[7:0]							

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CHANNEL N HA/LA MSB REGISTER

Bits[7:4] **Chn-HA/LA Hysteresis[3:0]**

These bits set the channel *n* high/low alarm hysteresis.
For example, bits[7:4] of the channel 6 HA MSB register (address 1Eh, page 1) set the channel 6 high alarm hysteresis.

0000 = No hyeteresis
0001 = ±1LSB hystetesis
0010 to 1110 = ±2LSB to ±14LSB hystetesis
1111 = ±15-LSB hystetesis

Bits[3:0] **Chn-HA/LA[11:8]**

These bits set the MSB nibble for the 12-bit channel *n* high/low alarm.
For example, the channel 7 high alarm threshold is AFFh when bits[3:0] of the channel 7 HA MSB register (address 22h, page 1) are set to Ah and the channel 7 HA LSB (address 23h, page 1) register setting is FFh.

0000 = MSB nibble is 0h
0001 = MSB nibble is 1h
0010 to 1110 = MSB nibble is 2h to Eh
1111 = MSB nibble is Fh

CHANNEL N HA/LA LSB REGISTER

Bits[7:0] **Chn HA[7:0]**

These bits set the LSB byte for the 12-bit channel *n* high/low alarm.
For example, the channel 2 low alarm threshold is F01h when the channel 2 LA LSB register (address 0Dh, page 1) setting is 01h and bits[3:0] of the channel 2 LA MSB (address 0Ch, page 1) are set to Fh.

0000 0000 = LSB byte is 0h
0000 0001 = LSB byte is 1h
0000 0010 to 1110 1111 = LSB byte is 02h to EFh
1111 1111 = LSB byte is FFh

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REGISTER MAP: ADS8634

The ADS8634 internal registers are mapped in two pages: page 0 and page 1. Page 0 is selected by default at power-up and after reset. Any register read/write action while on page 0 addresses the page 0 registers. Writing 01h to register address 7Fh selects page 1 for any further register operations.

Page 0 registers are used to select the channel sequencing mode, program the configuration registers, and to read the alarm flags. Page 1 resisters are used to program the alarm thresholds for each channel and for the temperature sensor. Table 13 details page 0 and Table 14 details page 1.

Table 13. Page 0 Register Map for the ADS8634

REGISTER	REGISTER ADDRESS BITS[15:9]	DEFAULT VALUE(1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Channel Sequencing Control Registers										
Manual	04h	00h	0	Channel Select[1:0]		X(2)	Range Select[2:0]			Sel Temp Sensor
Auto	05h	00h	Reset-Seq	0	0	0	Range Select[2:0]			Sel Temp Sensor
Holding DIN line continuously (equivalent to writing zero to all sixteen bits) during device operation as per Figure 85 continues device operation in the last selected mode (auto/manual)										
Configuration Registers										
Reset-Device	01h	00h	0	0	0	0	0	0	0	Reset-Dev
Aux-Config	06h	08h	0	0	0	0	AL_PD Control	Int V_{REF} Enable	Temp Sensor Enable	0
Auto-Md Ch-Sel	0Ch	00h	Sel Ch0	X	Sel Ch1	X	Sel Ch2	X	Sel Ch3	X
Ch0 Range	10h	11h	0	Range Select Ch0[2:0]			0	X	X	X
Ch1 Range	11h	11h	0	Range Select Ch1[2:0]			0	X	X	X
Ch2 Range	12h	11h	0	Range Select Ch2[2:0]			0	X	X	X
Ch3 Range	13h	11h	0	Range Select Ch3[2:0]			0	X	X	X
Alarm Flags (Read-Only)										
Temp-Flag	20h	00h	Tripped Alarm Flag Temperature Low	Tripped Alarm Flag Temperature High	Active Alarm Flag Temperature Low	Active Alarm Flag Temperature High	0	0	0	0
Ch0-1 Tripped-Flag	21h	00h	Tripped Alarm Flag Ch0 Low	Tripped Alarm Flag Ch0 High	X	X	Tripped Alarm Flag Ch1 Low	Tripped Alarm Flag Ch1 High	X	X
Ch0-1 Active-Flag	22h	00h	Active Alarm Flag Ch0 Low	Active Alarm Flag Ch0 High	X	X	Active Alarm Flag Ch1 Low	Active Alarm Flag Ch1 High	X	X
Ch2-3 Tripped-Flag	23h	00h	Tripped Alarm Flag Ch2 Low	Tripped Alarm Flag Ch2 High	X	X	Tripped Alarm Flag Ch3 Low	Tripped Alarm Flag Ch3 High	X	X
Ch2-3 Active-Flag	24h	00h	Active Alarm Flag Ch2 Low	Active Alarm Flag Ch2 High	X	X	Active Alarm Flag Ch3 Low	Active Alarm Flag Ch3 High	X	X
Page Selection Register										
Page	7Fh	00h	0	0	0	0	0	0	0	Page Addr

(1) All registers are reset to the default values at power-on or at device reset using the register settings method.
(2) X = don't care.

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Table 14. Page 1 Register Map for the ADS8634

REGISTER	REGISTER ADDRESS BITS[15:9]	DEFAULT VALUE(1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Alarm Threshold Registers										
TLA MSB	00h	00h	TLA Hysteresis[3:0]				TLA[11:8]			
TLA LSB	01h	00h	TLA[7:0]							
THA MSB	02h	00h	THA Hysteresis[3:0]				THA[11:8]			
THA LSB	03h	00h	THA[7:0]							
Ch0LA MSB	04h	00h	Ch0-LA Hysteresis[3:0]				Ch0-LA[11:8]			
Ch0LA LSB	05h	00h	Ch0-LA[7:0]							
Ch0HA MSB	06h	00h	Ch0-HA Hysteresis[3:0]				Ch0-HA[11:8]			
Ch0HA LSB	07h	00h	Ch0-HA[7:0]							
No function	08h to 0Bh	00h	X(2)	X	X	X	X	X	X	X
Ch1LA MSB	0Ch	00h	Ch1-LA Hysteresis[3:0]				Ch1-LA[11:8]			
Ch1LA LSB	0Dh	00h	Ch1-LA[7:0]							
Ch1 HA MSB	0Eh	00h	Ch1-HA Hysteresis[3:0]				Ch1-HA[11:8]			
Ch1 HA LSB	0Fh	00h	Ch1-HA[7:0]							
No function	10h to 13h	00h	X	X	X	X	X	X	X	X
Ch2 LA MSB	14h	00h	Ch2-LA Hysteresis[3:0]				Ch2-LA[11:8]			
Ch2 LA LSB	15h	00h	Ch2-LA[7:0]							
Ch2 HA MSB	16h	00h	Ch2-HA Hysteresis[3:0]				Ch2-HA[11:8]			
Ch2 HA LSB	17h	00h	Ch2-HA[7:0]							
No function	18h to 1Bh	00h	X	X	X	X	X	X	X	X
Ch3 LA MSB	1Ch	00h	Ch3-LA Hysteresis[3:0]				Ch3-LA[11:8]			
Ch3 LA LSB	1Dh	00h	Ch3-LA[7:0]							
Ch3 HA MSB	1Eh	00h	Ch3-HA Hysteresis[3:0]				Ch3-HA[11:8]			
Ch3 HA LSB	1Fh	00h	Ch3-HA[7:0]							
No function	20h to 23h	00h	X	X	X	X	X	X	X	X
Page Selection Register										
Page	7Fh	00h	0	0	0	0	0	0	0	Page Addr

(1) All registers are reset to the default values at power-on or at device reset using the register settings method.
(2) X = don't care.

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PAGE 0 REGISTER DESCRIPTIONS (ADS8634)

This section provides bit-by-bit descriptions of each page 0 register. As described earlier, the device registers are mapped to two pages: page 0 and page 1. Page 0 is selected by default at power-up and after reset. Any register read/write action while on page 0 addresses the page 0 registers. Writing 01h to register address 7Fh selects page 1 for any further register operations.

Channel Sequencing Control Registers for the ADS8634

There are two modes for channel sequencing: auto and manual mode. In auto-scan mode, the device automatically scans the preselected channels in chronological order; a new channel is selected for every conversion. In manual mode, the channel is selected for the next conversion. In both modes, the preselected signal range is considered for each channel independently; however, the range can be temporarily overriden.

Manual: Manulal Mode Register (Address = 04h; Page 0)

7	6	5	4	3	2	1	0
0	Channel Select[1:0]		X(1)	Range Select[2:0]			Sel Temp Sensor

(1) X = don't care.

This register selects device operation in manual scan mode, selects channel for next conversion, allows the preselected signal range for the next conversion to be temporarialy overridden, and enables the device temperature to be read.

Bit 7 **Must always be set to '0'**

Bits[6:5] **Channel Select[1:0]**

These bits select the channel for acquisition during the next frame.
For example, if this register is written in frame number *n*, then the addressed channel signal is acquired in frame number *n + 1* and the conversion result is available in frame number *n + 2*.

00 = Channel 0
01 = Channel 1
10 = Channel 2
11 = Channel 3

Bit 4 **Don't care (can be 1 or 0); this bit has no function assigned**

Bits[3:1] **Range Select[2:0]**

These bits select the signal range for the channel acquired in the next frame.
For example, if this register is written in frame number *n*, then the selected range is applicable for frame number *n + 1*. This is a dynamic range selection and overrides selection through the configuration registers (addresses 10h to 13h, page 0) only for the next frame.

000 = Ranges as selected through the configuration registers (address 10h to 13h, page 0)
001 = Range is set to ±10V
010 = Range is set to ±5V
011 = Range is set to ±2.5V
100 = Reserved; do not use this setting
101 = Range is set to 0V to 10V
110 = Range is set to 0V to 5V
111 = Powers down the device immediately after the 16th SCLK falling edge

Bit 0 **Sel Temp Sensor**

This bit selects the temperature sensor for acquisition in the next frame.
This selection overrides channel selection through bits[6:4]. Range selection is not applicable for the temperature sensor.

0 = Next conversion as per selection through bits[3:1]
1 = Device selects the temperature sensor for acquisition in the next frame

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Auto: Auto-Scan Mode Register (Address = 05h; Page 0)

7	6	5	4	3	2	1	0
Reset-Seq	0	0	0	Range Select[2:0]			Sel Temp Sensor

This register selects device operation in auto-scan mode, allows the preselected signal range for the next conversion to be temporarily overriden, and enables the device temperature to be read.

Bit 7 **Reset-Seq**

This bit resets the auto-mode sequence counter. The counter is reset to the lowest channel number in the selected sequence.
For example, if the Auto-Md Ch-Sel register is programmed to *01101100* (auto-mode sequence channels 2, 3, 5, 6, 2, 3, 5, 6…2, 3, 5, 6) and, if the auto register bit 7 is programmed to '1' in frame *n* while channel 3 is sampled, then the auto-mode sequence counter resets to channel 2 in frame *n + 1*. This setting means channel 2 is sampled instead of channel 5 in frame *n + 1*.

0 = No reset (continue sequence from the present channel number)
1 = Reset channel sequncing counter

Bits[6:4] **Must always be set to '0'**

Bits[3:1] **Range Select[2:0]**

These bits select the signal range for the channel acquired in the next frame.
For example, if this register is written in frame number *n*, then the selected range is applicable for frame number *n + 1*. This is a dynamic range selection and overrides selection through the configuration registers (address 10h to 13h, page 0) only for the next frame.

000 = Ranges as selected through the configuration registers (addresses 10h to 13h)
001 = Range is set to ±10V
010 = Range is set to ±5V
011 = Range is set to ±2.5V
100 = Reserved; do not use this setting
101 = Range is set to 0V to 10V
110 = Range is set to 0V to 5V
111 = Powers down the device immediately after the 16th SCLK falling edge

Bit 0 **Sel Temp Sensor**

This bit selects the temperature sensor for acquisition in the next frame.
This selection overrides channel selection through the auto sequence only for the next frame. The auto sequence continues from where it was interrupted after the temperature sensing frame.
For example, if the programmed auto sequence is channels 0, 1, 3, 0, 1, 3…0, 1, 3 and, if the temperature sensor is selected in frame number *n* while channel 0 is sampled, then the temperature sensor is sampled in frame *n + 1*. The auto sequence resumes from frame *n + 2* sampling channel 1. Range selection is not applicable for the temperature sensor.

0 = Next conversion as per selection through bits[3:1]
1 = The temperature sensor is selected for acquisition in the next frame

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Continued Operation in the Selected Mode for the ADS8634

Holding the DIN line low continuously (equivalent to writing '0' to all 16 bits) during device operation as per Figure 85 continues device operation in the last selected mode (auto or manual). The device follows range selection through the configuration registers (address 10h to 13h). The internal temperature sensor continues to be read if the temperature sensor was selected during the last auto/manual mode frame.

Configuration Registers for the ADS8634

These registers allow device configuration (such as signal range selection for individual channels, selection of channels for auto sequence, enabling/disabling of internal reference and temperature sensor, and configuration of the AL_PD pin as an alarm output or as a power-down input). All of the registers can be reset to the default values using the configuration register.

Reset-Device: Device Reset Register (Address = 01h; Page 0)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	Reset-Dev

This register resets the device and assigns default values to all internal registers. The reset value for this register is 00h; as a result, this bit is self-clearing.

Bits[7:1] **Must always be set to '0'**

Bit 0 **Reset-Dev**

This bit initiates a software reset immediately after the 16th SCLK falling edge.
All registers in the device are assigned the reset values mentioned in and Table 11 and Table 12.

0 = No reset
1 = Reset device

Aux-Config: Device Auxiliary Blocks Enable/Disable Control Register (Address = 06h; Page 0)

7	6	5	4	3	2	1	0
0	0	0	0	AL_PD Control	Int V_{REF} Enable	Temp Sensor Enable	0

This register controls functionality of the AL_PD pin and enables/disables blocks such as the internal reference and the internal temperature sensor.

Bits[7:4] **Must always be set to '0'**

Bit 3 **AL_PD Control**

This bit controls the functionality of the AL_PD pin.

0 = The AL_PD pin functions as an alarm output pin
1 = The AL_PD pin functions as a power-down control pin

Bit 2 **Int V_{REF} Enable**

This bit powers up the internal V_{REF}.

0 = Internal reference block is powered down from the next frame
1 = Internal reference block is powered up from the next frame

Bit 1 **Temp Sensor Enable**

This bit powers up the internal temperature sensor.

0 = Internal temperature sensor block is powered down from the next frame
1 = Internal temperature sensor block is powered up from the next frame

Bit 0 **Must always be set to '0'**

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Auto-Md Ch-Sel: Channel Selection Registers for Auto-Scan Mode (Address = 0Ch; Page 0)

7	6	5	4	3	2	1	0
Sel Ch0	X(1)	Sel Ch1	X	Sel Ch2	X	Sel Ch3	X

(1) X = don't care.

This register selects channels for the auto-mode sequence. The device scans only the selected channels in ascending order during auto-scan mode, starting with the lowest channel selected. For example, if the Auto-Md Ch-Sel register is programmed to *01100100*, then the auto-mode sequence is channels 2, 5, 6, 2, 5, 6…2, 5, 6, and in this case, the sequence always starts from channel 2. Channel 0 is selected if this register is programmed to *00000000*.

Bit 7 **Sel Ch0**

This bit selects channel 0.

0 = Channel 0 not selected
1 = Channel 0 selected

Bit 6 **Don't care (can be 1 or 0); this bit has no function assigned**

Bit 5 **Sel Ch1**

This bit selects channel 1.

0 = Channel 1 not selected
1 = Channel 1 selected

Bit 4 **Don't care (can be 1 or 0); this bit has no function assigned**

Bit 3 **Sel Ch2**

This bit selects channel 2.

0 = Channel 2 not selected
1 = Channel 2 selected

Bit 2 **Don't care (can be 1 or 0); this bit has no function assigned**

Bit 1 **Sel Ch3**

This bit selects channel 3.

0 = Channel 3 not selected
1 = Channel 3 selected

Bit 0 **Don't care (can be 1 or 0); this bit has no function assigned**

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Ch0 Range to Ch3 Range: Range Selection Registers for Channels 0 to 3 (Address = 10h to 13h; Page 0)

REGISTER	ADDRESS ON PAGE 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Ch0 Range	10h	0	Range Select Ch0[2:0]			0	X(1)	X	X
Ch1 Range	11h	0	Range Select Ch1[2:0]			0	X	X	X
Ch2 Range	12h	0	Range Select Ch2[2:0]			0	X	X	X
Ch3 Range	13h	0	Range Select Ch3[2:0]			0	X	X	X

(1) X = don't care.

A selection of signal ranges are featured for each channel. The selected range is automatically assigned for a channel during conversion, regardless of the channel scan mode (auto or manual). These registers (Ch0 Range to Ch3 Range) allow for selection of ranges for all channels.

Bit 7 **Must always be set to '0'**

Bits[6:4] **Range Select Chn[2:0]**

These bits select the signal range for channel *n*, where n is 0, 1, 2, or 3, depending on the register address.

000 = Reserved; do not use this setting
001 = Range is set to ±10V
010 = Range is set to ±5V
011 = Range is set to ±2.5V
100 = Reserved; do not use this setting
101 = Range is set to 0V to 10V
110 = Range is set to 0V to 5V
111 = Reserved; do not use this setting

Bit 3 **Must always be set to '0'**

Bit 2 : 0 **Don't care (can be 1 or 0); this bit has no function assigned**

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Alarm Flag Registers for the ADS8634 (Read-Only)

The alarm conditions related to individual channels are stored in these registers. When an alarm interrupt is received, the flags can be read on the AL_PD pin. There are two types of flag for every alarm: active and tripped. An active alarm flag is enabled when an alarm is triggered (when data cross the alarm threshold) and remains enabled as long as the alarm condition persists. A tripped alarm flag is enabled in the same manner as an active alarm flag, but it remains latched until it is read. This feature relieves the device from having to track alarms.

Temp Flag: Alarm Flags Register for the Temperature Sensor (Address = 20h; Page 0)

7	6	5	4	3	2	1	0
Tripped Alarm Flag Temperature Low	Tripped Alarm Flag Temperature High	Active Alarm Flag Temperature Low	Active Alarm Flag Temperature High	0	0	0	0

The Temp Flag register stores alarm flags for the temperature sensor. There are two alarm thresholds, with two flags for each threshold. An active alarm flag is enabled when an alarm is triggered (when data cross the alarm threshold) and remains enabled as long as the alarm condition persists. A tripped alarm flag is enabled in the same manner as an active alarm flag, but it remains latched until it is read.

Bit 7 **Tripped Alarm Flag Temperature Low**

This bit indicates the tripped low alarm flag for the temperature sensor.

0 = No alarm detected
1 = Alarm detected

Bit 6 **Tripped Alarm Flag Temperature High**

This bit indicates the tripped high alarm flag for the temperature sensor.

0 = No alarm detected
1 = Alarm detected

Bit 5 **Active Alarm Flag Temperature Low**

This bit indicates the active low alarm flag for the temperature sensor.

0 = No alarm
1 = Alarm detected

Bit 4 **Active Alarm Flag Temperature High**

This bit indicates the active-high alarm flag for the temperature sensor.

0 = No alarm detected
1 = Alarm detected

Bits[3:0] **Always read '0'**

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Ch0-1 Tripped-Flag to Ch2-3 Active-Flag: Alarm Flags Register for Channels 0 to 3 (Address = 21h to 24h; Page 0)

REGISTER	ADDRESS ON PAGE 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Ch0-1 Tripped-Flag	21h	Tripped Alarm Flag Ch0 Low	Tripped Alarm Flag Ch0 High	X(1)	X	Tripped Alarm Flag Ch1 Low	Tripped Alarm Flag Ch1 High	X	X
Ch0-1 Active-Flag	22h	Active Alarm Flag Ch0 Low	Active Alarm Flag Ch0 High	X	X	Active Alarm Flag Ch1 Low	Active Alarm Flag Ch1 High	X	X
Ch2-3 Tripped-Flag	23h	Tripped Alarm Flag Ch2 Low	Tripped Alarm Flag Ch2 High	X	X	Tripped Alarm Flag Ch3 Low	Tripped Alarm Flag Ch3 High	X	X
Ch2-3 Active-Flag	24h	Active Alarm Flag Ch2 Low	Active Alarm Flag Ch2 High	X	X	Active Alarm Flag Ch3 Low	Active Alarm Flag Ch3 High	X	X

(1) X = don't care.

There are two alarm thresholds (High and Low) per channel and for each threshold there are two flags. An active alarm flag is enabled when an alarm is triggered (when data cross the alarm threshold) and remains enabled as long as the alarm condition persists. A tripped alarm flag is enabled in the same manner as an active alarm flag, but it remains latched until it is read. Registers addressed 21h to 24h on page 0 store active and tripped alarm flags for all four channels.

Bits[7:6] **Active/Tripped Alarm Flag Chn High/Low**

Each individual bit indicates an active/tripped, high/low alarm flag for each channel, as per the Ch0-1 Tripped-Flag to Ch2-3 Active-Flag register.

0 = No alarm detected
1 = Alarm detected

Bits[5:4] **Don't care (1 or 0), these bits do not have any function assigned**

Bits[3:2] **Active/Tripped Alarm Flag Chn High/Low**

Each individual bit indicates an active/tripped, high/low alarm flag for each channel, as per the Ch0-1 Tripped-Flag to Ch2-3 Active-Flag register.

0 = No alarm detected
1 = Alarm detected

Bits[1:0] **Don't care (1 or 0), these bits do not have any function assigned**

Page Selection Register for the ADS8634

The registers are arranged on two pages: page 0 and page 1. The page register selects the register page.

Page: Page Selection Register (Address = 7Fh; Page 0)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	Page Addr

Bits[7:1] **Must always be set to '0'**

Bit 0 **Page Addr**

This bit selects the page address.

0 = Selects page 0 for the next register read or write command; all register read/write operations after this are performed on the page 0 registers until page 1 is selected
1 = Selects page 1 for the next register read or write command; all register read/write operations after this are performed on the page 1 registers until page 0 is selected

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PAGE 1 REGISTER DESCRIPTIONS (ADS8634)

This section provides bit-by-bit descriptions of each page 1 register. As described earlier, the device registers are mapped to two pages: page 0 and page 1. Page 0 is selected by default at power-up and after reset. Page 1 can be selected by writing 01h to register address 7Fh. After selecting page 1, any register read/write action addresses page 1 registers after a page 1 selection. Writing 00h to register address 7Fh selects page 0 for any further register operations.

Alarm Threshold Setting Registers for the ADS8634

The device features high and low alarms individually for the temperature sensor and each of the four channels. Each alarm threshold is 12-bits wide with 4-bit hysteresis. This 16-bit setting is accomplished with two 8-bit registers associated with every high/low alarm.

TLA MSB to THA LSB: Temperature Alarm Registers (Address = 00h to 03h; Page 1)

REGISTER	ADDRESS ON PAGE 1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TLA MSB		TLA Hysteresis[3:0]				TLA[11:8]			
TLA LSB		TLA[7:0]							
THA MSB		THA Hysteresis[3:0]				THA[11:8]			
THA LSB		THA[7:0]							

THA/LA MSB Register

Bits[7:4] **THA/LA Hysteresis[3:0]**

These bits set the temperature high/low alarm hysteresis.

0000 = No hyeteresis
0001 = ±1LSB hystetesis
0010 to 1110 = ±2LSB to ±14LSB hystetesis
1111 = ±15LSB hystetesis

Bits[3:0] **THA/LA[11:8]**

These bits set the MSB nibble for the 12-bit temperature high/low alarm.
For example, the temperature high alarm threshold is AFFh when the THA MSB register (address 02h, page 1) setting is Ah and the THA LSB register (address 03h, page 1) register setting is FFh.

0000 = MSB nibble is 0h
0001 = MSB nibble is 1h
0010 to 1110 = MSB nibble is 2h to Eh
1111 = MSB nibble is Fh

THA/LA LSB Register

Bits[7:0] **THA/LA[7:0]**

These bits set the LSB byte for the 12-bit temperature high alarm.
For example, the temperature low alarm threshold is F02h when the TLA LSB register (address 01h) setting is 02h and the TLS MSB register (address 00h, page 1) register setting is Fh.

0000 0000 = LSB byte is 0h
0000 0001 = LSB byte is 1h
0000 0010 to 1110 1111 = LSB byte is 02h to EFh
1111 1111 = LSB byte is FFh

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Ch0LA MSB to Ch3HA LSB: Channels 0 to 3 Alarm Registers (Address = 04h to 23h; Page 1)

REGISTER	ADDRESS ON PAGE 1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Ch0LA MSB	04h	Ch0-LA Hysteresis[3:0]				Ch0-LA[11:8]			
Ch0LA LSB	05h	Ch0-LA[7:0]							
Ch0HA MSB	06h	Ch0-HA Hysteresis[3:0]				Ch0-HA[11:8]			
Ch0HA LSB	07h	Ch0-HA[7:0]							
No function	08h to 0Bh	X(1)	X	X	X	X	X	X	X
Ch1LA MSB	0Ch	Ch1-LA Hysteresis[3:0]				Ch1-LA[11:8]			
Ch1LA LSB	0Dh	Ch1-LA[7:0]							
Ch1HA MSB	0Eh	Ch1-HA Hysteresis[3:0]				Ch1-HA[11:8]			
Ch1HA LSB	0Fh	Ch1-HA[7:0]							
No function	10h to 13h	X	X	X	X	X	X	X	X
Ch2LA MSB	14h	Ch2-LA Hysteresis[3:0]				Ch2-LA[11:8]			
Ch2LA LSB	15h	Ch2-LA[7:0]							
Ch2HA MSB	16h	Ch2-HA Hysteresis[3:0]				Ch2-HA[11:8]			
Ch2HA LSB	17h	Ch2-HA[7:0]							
No function	18h to 1Bh	X	X	X	X	X	X	X	X
Ch3LA MSB	1Ch	Ch3-LA Hysteresis[3:0]				Ch3-LA[11:8]			
Ch3LA LSB	1Dh	Ch3-LA[7:0]							
Ch3HA MSB	1Eh	Ch3-HA Hysteresis[3:0]				Ch3-HA[11:8]			
Ch3HA LSB	1Fh	Ch3-HA[7:0]							
No function	20h to 23h	X	X	X	X	X	X	X	X

(1) X = don't care.

Channel N HA/LA MSB Register

Bits[7:4] **Chn-HA/LA Hysteresis[3:0]**

These bits set the channel *n* high/low alarm hysteresis.
For example, bits[7:4] of the channel 2 HA MSB register (address 16h, page 1) set the channel 2 high alarm hysteresis.

0000 = No hyeteresis
0001 = ±1LSB hystetesis
0010 to 1110 = ±2LSB to ±14LSB hystetesis
1111 = ±15LSB hystetesis

Bits[3:0] **Chn-HA/LA[11:8]**

These bits set the MSB nibble for the 12-bit channel *n* high/low alarm.
For example, the channel 3 high alarm threshold is AFFh when bits[3:0] of the channel 3 HA MSB register (address 1Eh, page 1) are set to Ah and the channel 3 HA LSB (address 1Fh, page 1) register setting is FFh.

0000 = MSB nibble is 0h
0001 = MSB nibble is 1h
0010 to 1110 = MSB nibble is 2h to Eh
1111 = MSB nibble is Fh

Channel N HA/LA LSB Register

Bits[7:0] **Chn HA[7:0]**

These bits set the LSB byte for the 12-bit channel *n* high/low alarm.
For example, the channel 1 low alarm threshold is F01h when the channel 1 LA LSB register (address 0Dh, page 1) setting is 01h and bits[3:0] of the channel 1 LA MSB (address 0Ch, page 1) are set to Fh.

0000 0000 = LSB byte is 0h
0000 0001 = LSB byte is 1h
0000 0010 to 1110 1111 = LSB byte is 02h to EFh
1111 1111 = LSB byte is FFh

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APPLICATION INFORMATION

DRIVING ANALOG SIGNAL INPUT

The ADS8634/8 employ a sample-and-hold stage at the input. An 8pF sampling capacitor is connected during sampling. This configuration results in a glitch at the input terminals of the device at the start of the sample. The external circuit must be designed in such a way that the input can settle to the required accuracy during the chosen sampling time. Figure 91 shows a reccomended driving circuit for the analog inputs.

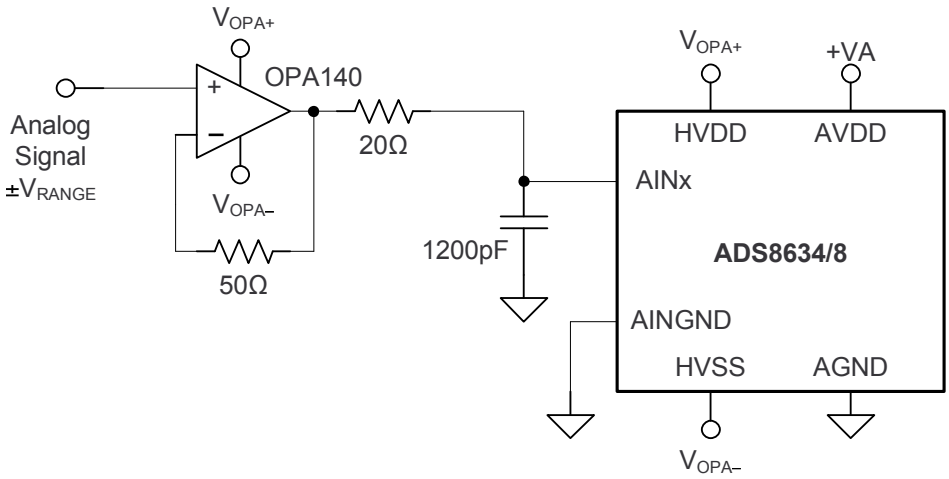

Figure 91. Reccomended Driving Circuit

The 8pF capacitor across the AINx and AINGND terminals decouples the driving op amp from the sampling glitch. The low-pass filter at the input limits noise bandwidth of the driving op amp. Select the filter bandwidth so that the full-scale step at the input can settle to the required accuracy during the sampling time. Equation 5, Equation 6, and Equation 7 are useful for filter component selection.

$$\text{Filter Time Constant } (t_{AU}) = \frac{\text{Sampling Time}}{\text{Settling Resolution} \times \ln(2)}$$

Where:

Settling resolution is the accuracy in LSB to which the input must settle. A typical settling resolution for the 12-bit device is 13 or 14. (5)

$$\text{Filter Time Constant } (t_{AU}) = R \times C \quad (6)$$

$$\text{Filter Bandwidth} = \frac{1}{2 \times \pi \times t_{AU}} \quad (7)$$

Also, make sure the driving op amp bandwidth does not limit the signal bandwidth to below the filter bandwidth. In many applications, signal bandwidth may be much lower than filter bandwidth. In this case, an additional low-pass filter may be used at the input of the driving op amp. This signal and filter bandwidth can be selected in accordance with the input signal bandwidth.

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POWER MANAGEMENT AT LOWER SPEEDS

There are multiple data acquisition applications that require sampling speeds much lower than 1MSPS. The ADS8634/8 offer power saving while running at lower speeds. As shown in Figure 92, the ADS8634/8 consume dynamic power from a $\overline{CS}$ rising edge until the 16th SCLK falling edge. While using the ADS8634/8 at lower sampling speeds, it is recommended to use SCLK at the maximum specified frequency. This setting allows the maximum static period t_{STATIC} at any given sampling speed. The ADS8634/8 consume considerably lower static current (current during t_{STATIC}) from all three power supplies (AVDD, HVDD, and HVSS). This consumption helps lower the average currents from each of the supplies, resulting in a lower average power consumption while using the device at lower sampling speeds.

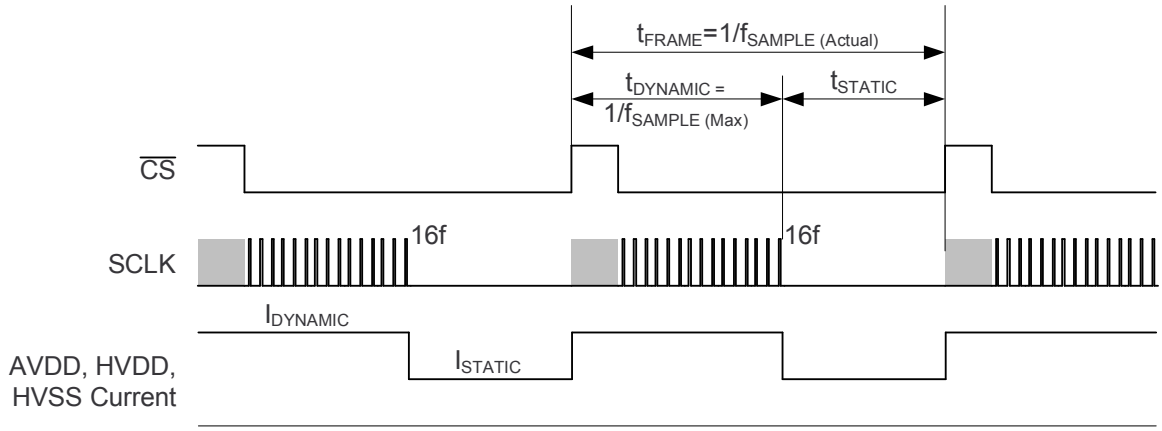

Figure 92. Supply Current Profile at Speeds Below 1MSPS

Table 15 shows t_{FRAME}, $t_{DYNAMIC}$, and t_{STATIC} at a 0.1MSPS sampling speed.

Table 15. Typical Static/Dynamic Time Distribution at Lower Speeds (0.1MSPS)

f_{SAMPLE} (MSPS)	t_{FRAME} (µs)	$t_{DYNAMIC}$ (µs)	t_{STATIC} (µs)
0.1	10	1	9

The average device power consumption can be calculated with Equation 8 and Equation 9:

Average Current, $I_{AVERAGE} = (I_{DYNAMIC} \times t_{DYNAMIC} + I_{STATIC} \times t_{STATIC})/(t_{DYNAMIC} + t_{STATIC})$ (8)

Average Power = Supply Voltage × $I_{AVERAGE}$ (9)

Table 16 shows the average power calculations at 0.1MSPS.

Table 16. Average Power Calculations at 0.1MSPS

PARAMETER	AVDD	HVDD	HVSS
Typical supply voltage (V)	3.3	10	10
$I_{DYNAMIC}$ (mA)	2.50	0.27	0.35
$t_{DYNAMIC}$ (µs)	1.0	1.0	1.0
I_{STATIC} (mA)	1.45	0.005	0.005
t_{STATIC} (µs)	9.0	9.0	9.0
Average current, $I_{AVERAGE}$ (mA)	1.555	0.032	0.040
Average power (mW)	5.132	0.315	0.395
Total average power (mW) = $P_{AVDD} + P_{HVDD} + P_{HVSS}$	5.842		

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PROGRAMMING SEQUENCE

A typical programming sequence for the ADS8634/8 is shown in Figure 93.

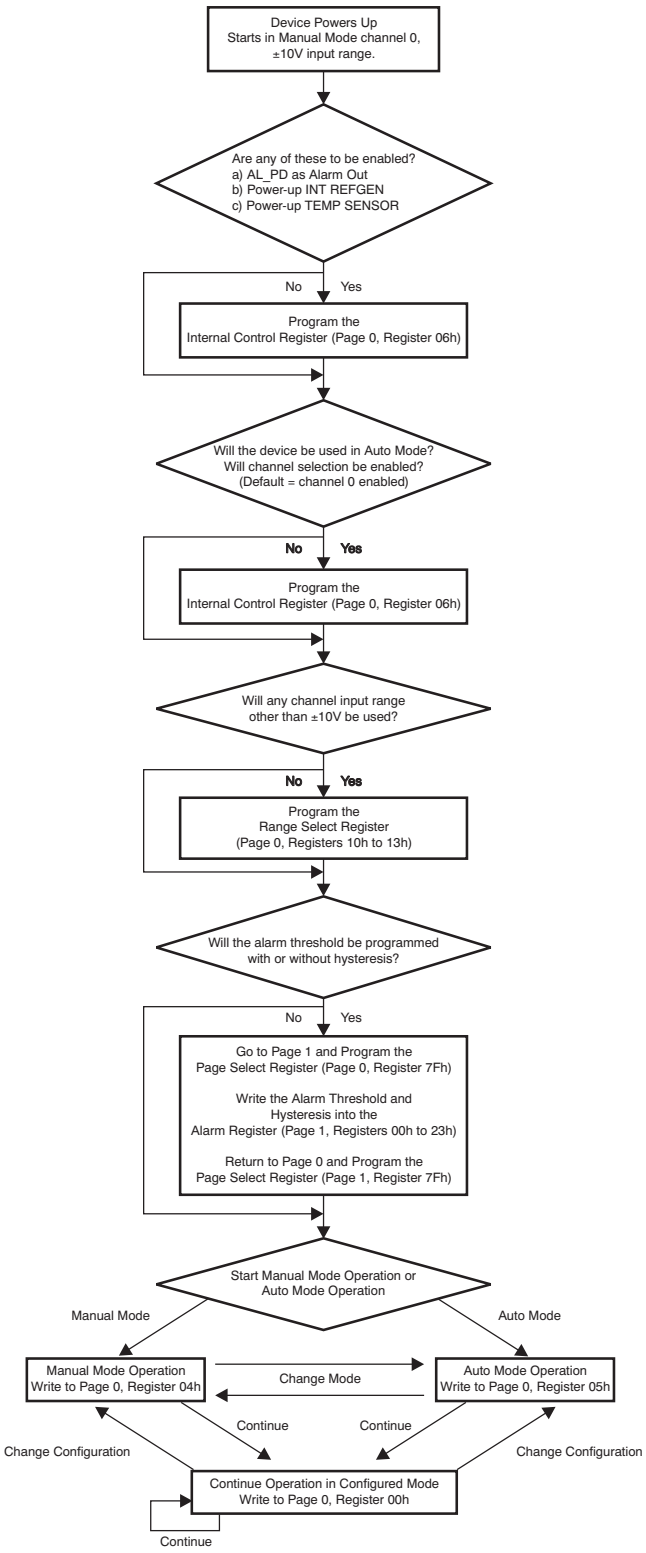

Figure 93. Programming Flowchart

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DRIVING ANALOG SIGNAL INPUT WITHOUT AN OPERATIONAL AMPLIFIER

There are some low input signal bandwidth applications, such as general-purpose programmable logic controllers (PLCs) I/O, where it is not required to operate an ADC at high sampling rates and it is desirable to avoid using a dedicated driving op amp from a cost perspective. In this case, the ADC input recognizes the impedance of the signal source (such as signal conditioning circuit, PGA, or sensor). This section elaborates on the effects of source impedance on sampling frequency.

Equation 5 can be rewritten as Equation 10:

Sampling Time = Filter Time Constant × Settling Resolution × ln(2) (10)

As shown in Figure 94, it is recommended to use a bypass capacitor across the positive and negative ADC input terminals.

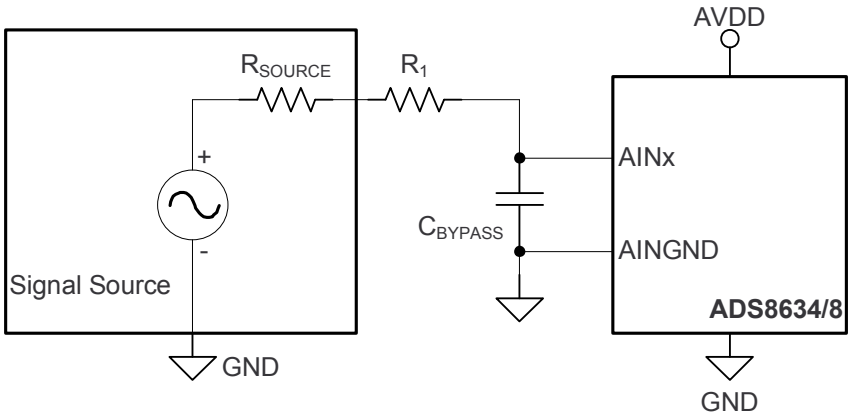

Figure 94. Driving Without an Operational Amplifier

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The source impedance (R_{SOURCE} + R_1) combined with (C_{BYPASS} + C_{SAMPLE}) acts as a low-pass filter with Equation 11:

Filter Time Constant = (R_{SOURCE} + R_1) × (C_{BYPASS} + C_{SAMPLE})

Where:

C_{SAMPLE} is the internal sampling capacitance of the ADC (equal to 32pF). (11)

Table 17 lists the recommended bypass capacitor values and the filter-time constant for different source resistances. It is recommended to use a bypass capacitor with a minimum value of 100pF. Table 17 assumes R_1 = 20Ω; however, depending on the application, R_1 can be bypassed (by shorting R_1) and the extra 20Ω margin can be used for source resistance.

Table 17. Filter-Time Constant versus Source Resistance

R_{SOURCE} (Ω)	R_{SOURCE} + R_1	APPROXIMATE C_{BYPASS} (pF)	C_{BYPASS} + C_{SAMPLE} (pF)	FILTER TIME CONSTANT (ns)
0	20	1200	1208	25
32	52	470	478	25
90	110	220	228	25
210	230	100	108	25
500	520	100	108	56
1000	1020	100	108	110
5000	5020	100	108	542

Typically, the settling resolution is selected as (ADC resolution + 2). For the ADS8634/8 (12-bit), the ideal settling resolution is 14. Using Equation 6 and Equation 7, the sampling time can be easily determined for a given source impedance. For source impedances greater than 210Ω, the filter-time constant continues to increase beyond the 25ns required for a 250ns sampling time. This incrementation increases the minimum permissible sampling time for 12-bit settling and the device must be operated at a lower sampling rate.

The device sampling rate can be maximized by using a 20MHz clock for even lower throughputs. Table 18 shows typical calculations for the ADS8634/8 (12-bit).

Table 18. Sampling Frequency versus Source Impedance for the ADS8634/8

R_{SOURCE} (Ω)	C_{BYPASS} (pF)	SAMPLING TIME, t_{ACQ} (ns)	CONVERSION TIME, t_{CONV} (ns)	CYCLE TIME, t_{ACQ} + t_{CONV} (ns)	SAMPLING RATE (MSPS)
210	100	250	750 (with 20MHz clock)	1000	1
500	100	545	750 (with 20MHz clock)	1295	0.8
1000	100	1070	750 (with 20MHz clock)	1820	0.5
5000	100	5260	750 (with 20MHz clock)	6010	0.2

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PCB LAYOUT SCHEMATIC RECCOMENDATIONS

ADCs are mixed-signal devices. For maximum performance, proper decoupling, grounding, and proper termination of digital signals is essential. Figure 95 and Figure 96 show the essential components around the ADC. All capacitors shown are ceramic. These decoupling capacitors must be placed close to the respective signal pins.

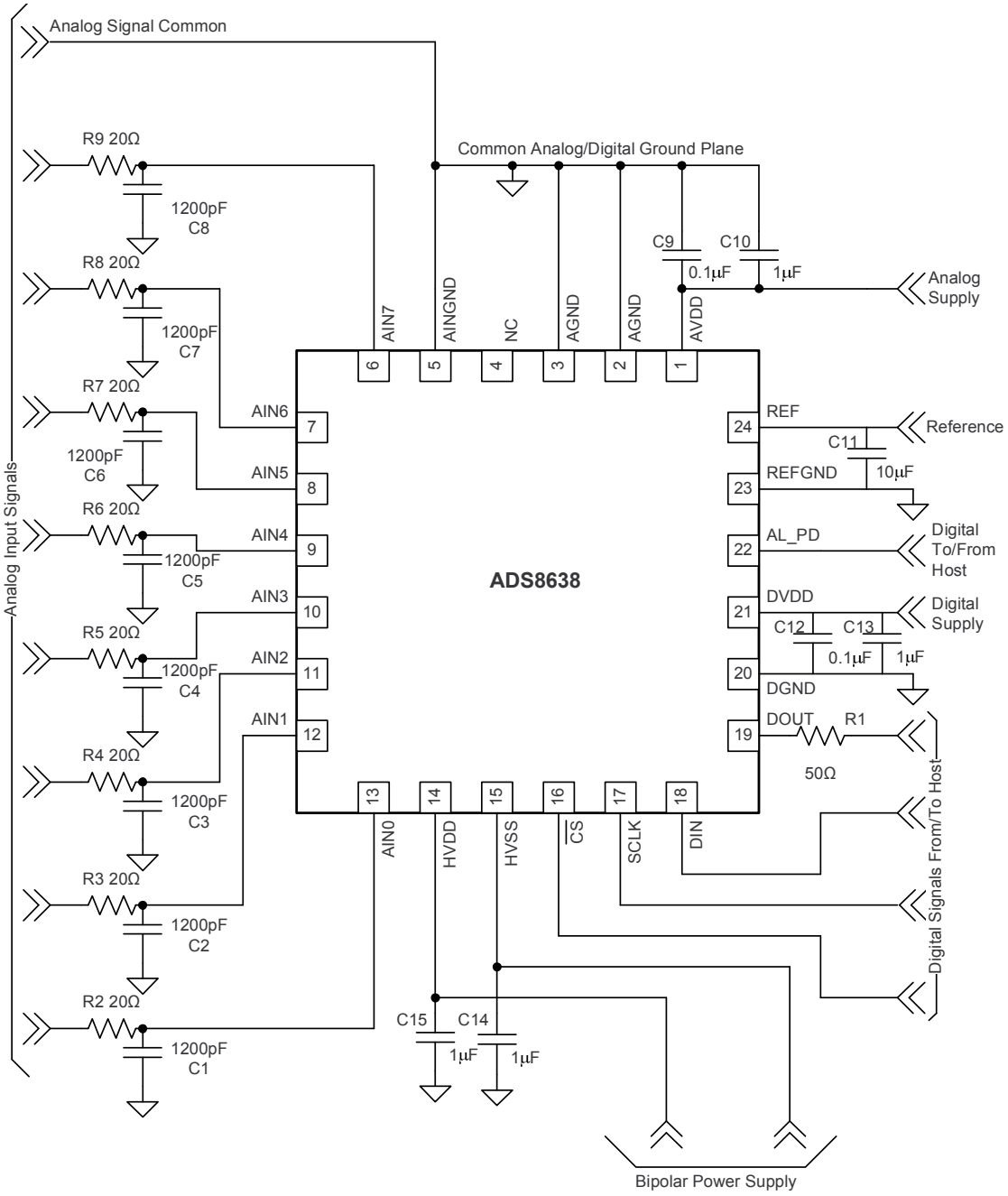

Figure 95. Reccomended Schematic for the ADS8638

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There is a 50Ω source series termination resistor shown on the DOUT signal. This resistor must be placed as close to DOUT as possible. Series terminations for SCLK and $\overline{CS}$ must be placed close to the host.

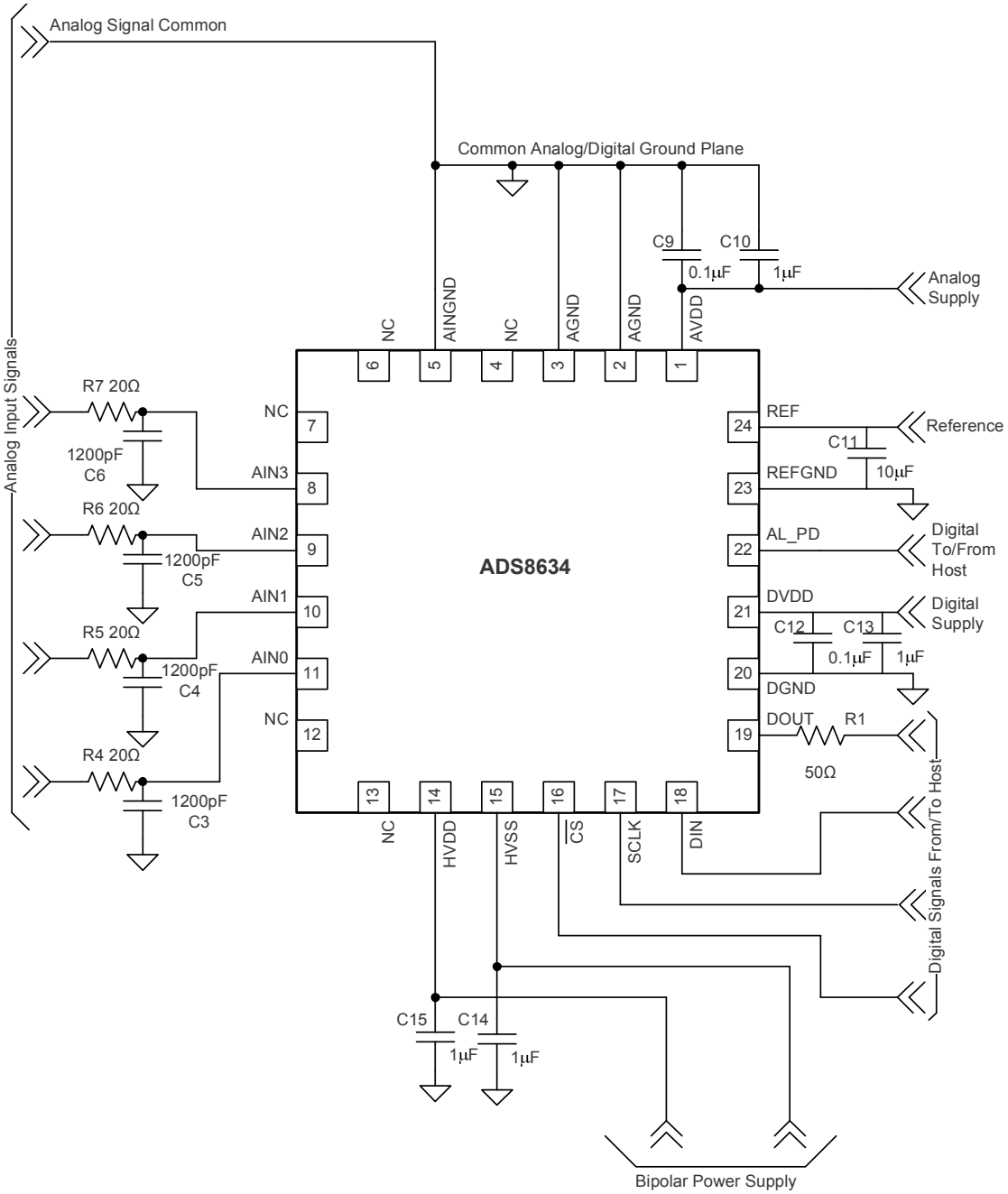

Figure 96. Reccomended Schematic for the ADS8634

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A common ground plane for both analog and digital often gives better results. Typically, the second printed circuit board (PCB) layer is the ground plane. The ADC ground pins are returned to the ground plane through multiple vias (PTH). It is a good practice to place analog components on one side and digital components on other side of the ADC (or ADCs). All signals must be routed, assuming there is a split ground plane for analog and digital. Furthermore, it is better to split the ground initially during layout. Route all analog and digital traces so that the traces see the respective ground all along the second layer. Then, short both grounds to form a common ground plane. Figure 97 Figure 98 show the reccomended layout around the ADS8638. The ADS8634 pinout is a subset of the ADS8638 pinout. It is possible to make a common layout for the ADS8634/8 . Or, one can delete the traces and components associated with the additional four channels of the ADS8638 to generate the ADS8634 layout.

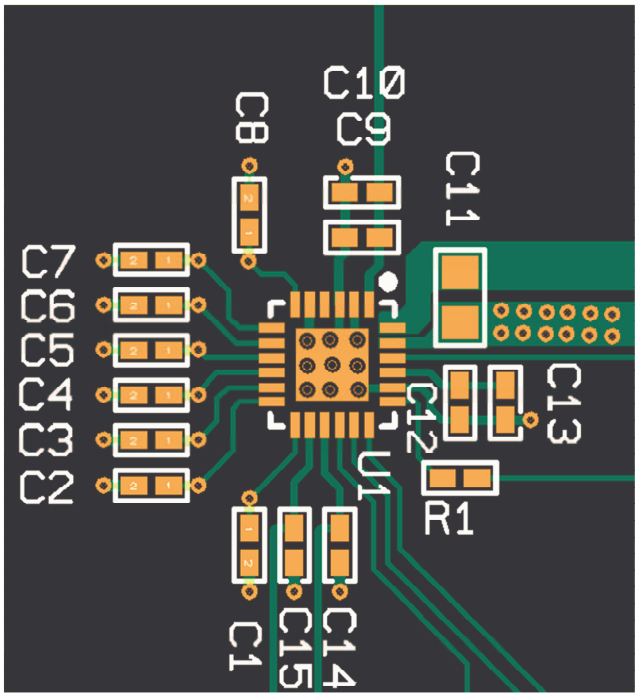

Figure 97. Reccomended Layout for the ADS8638 (Top layer)

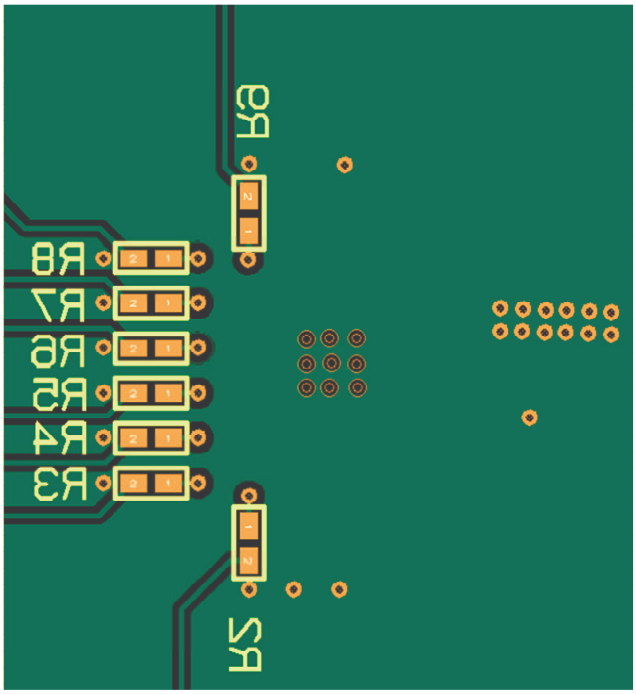

Figure 98. Reccomended Layout for the ADS8638 (Bottom layer)

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
ADS8634SRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	8634	Samples
ADS8634SRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	8634	Samples
ADS8638SRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	8638	Samples
ADS8638SRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	8638	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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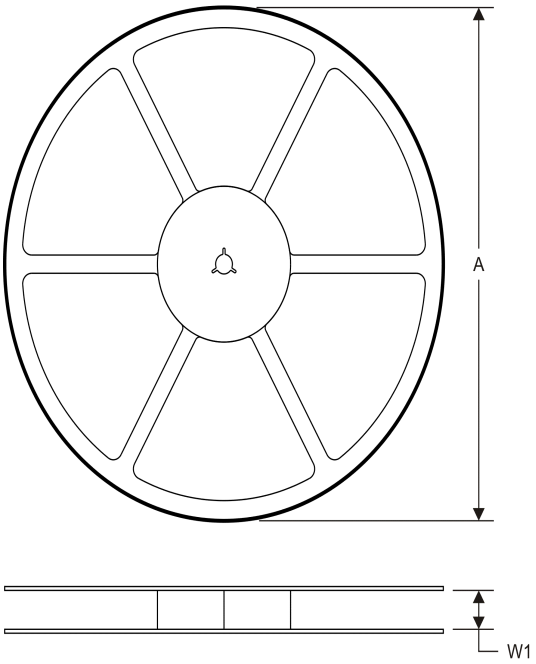
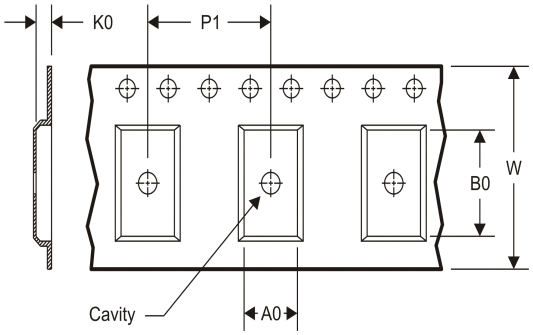
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8634SRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8634SRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8638SRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8638SRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

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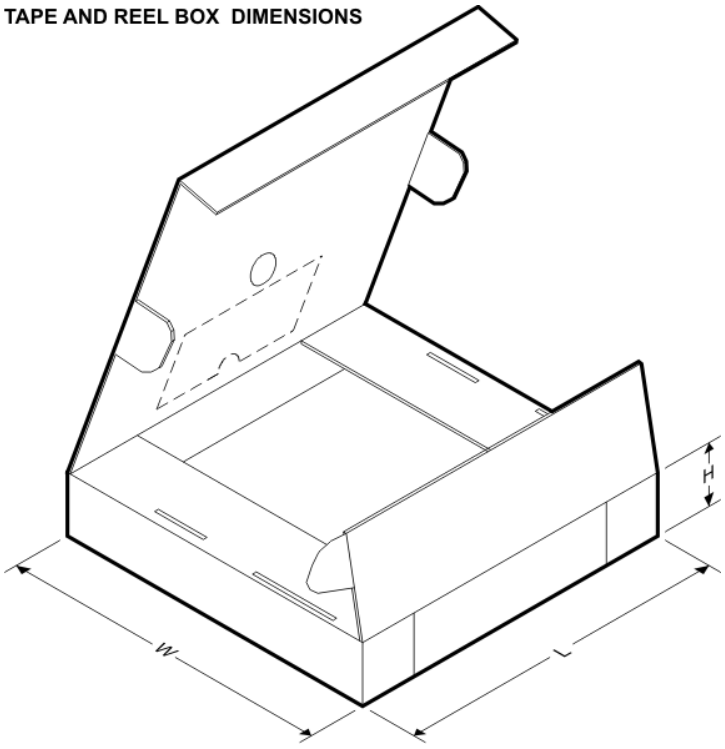
PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8634SRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
ADS8634SRGET	VQFN	RGE	24	250	210.0	185.0	35.0
ADS8638SRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
ADS8638SRGET	VQFN	RGE	24	250	210.0	185.0	35.0

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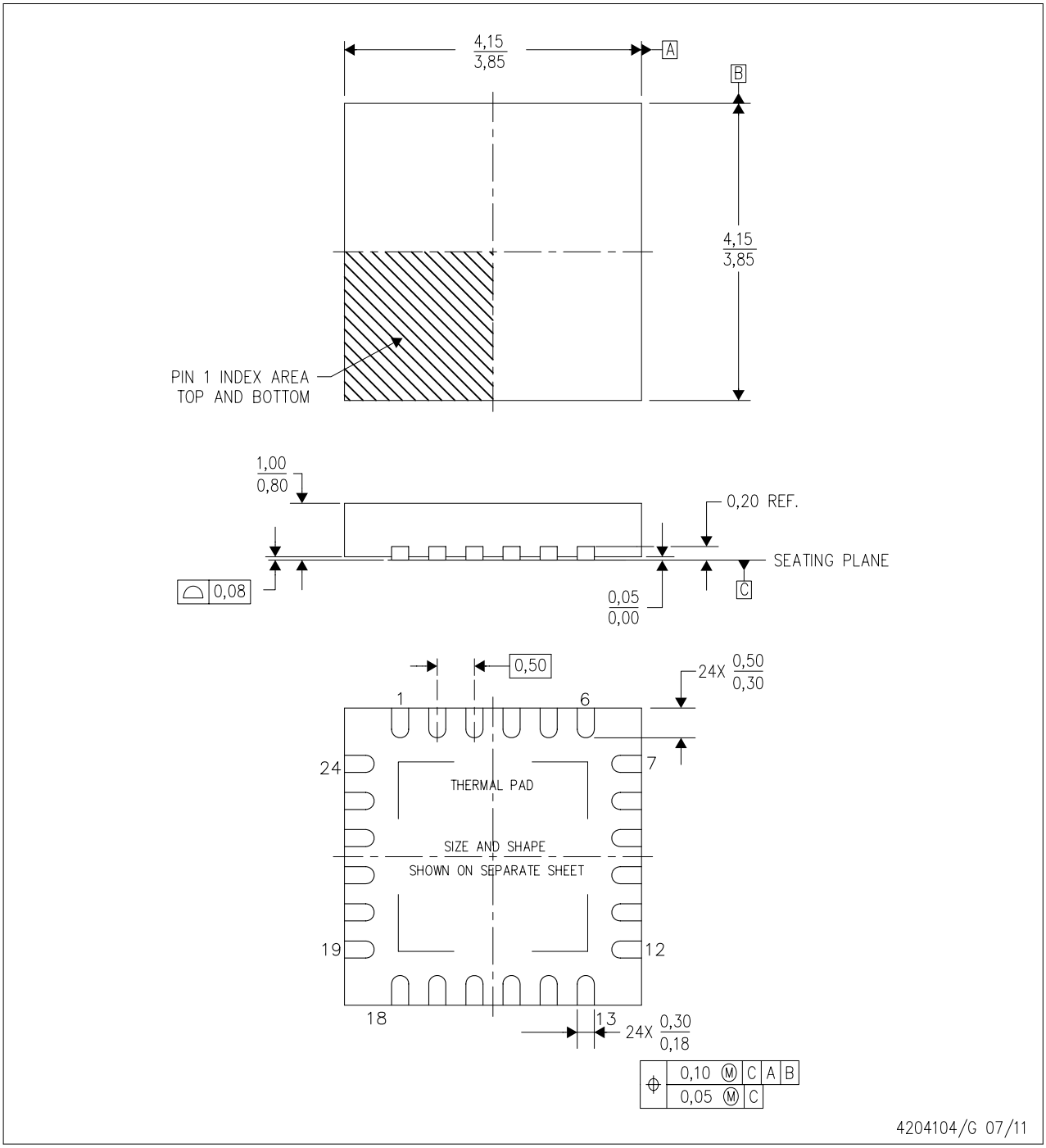
MECHANICAL DATA

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

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THERMAL PAD MECHANICAL DATA

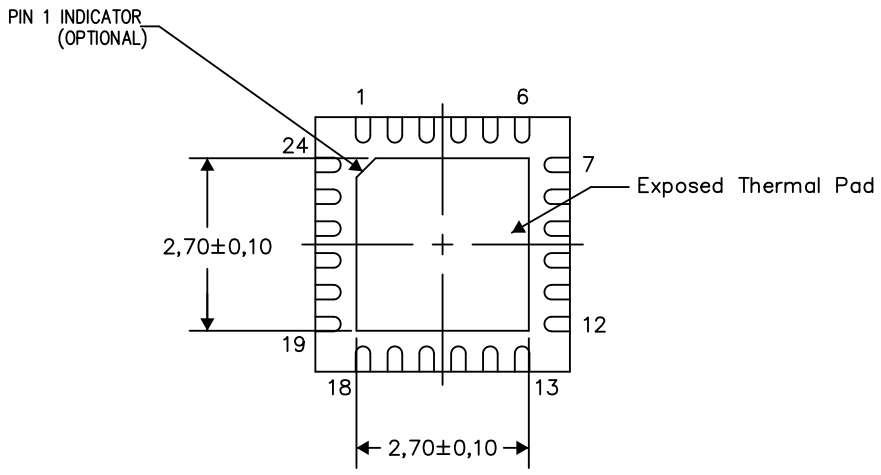
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206344–5/AK 08/15

NOTES: A. All linear dimensions are in millimeters

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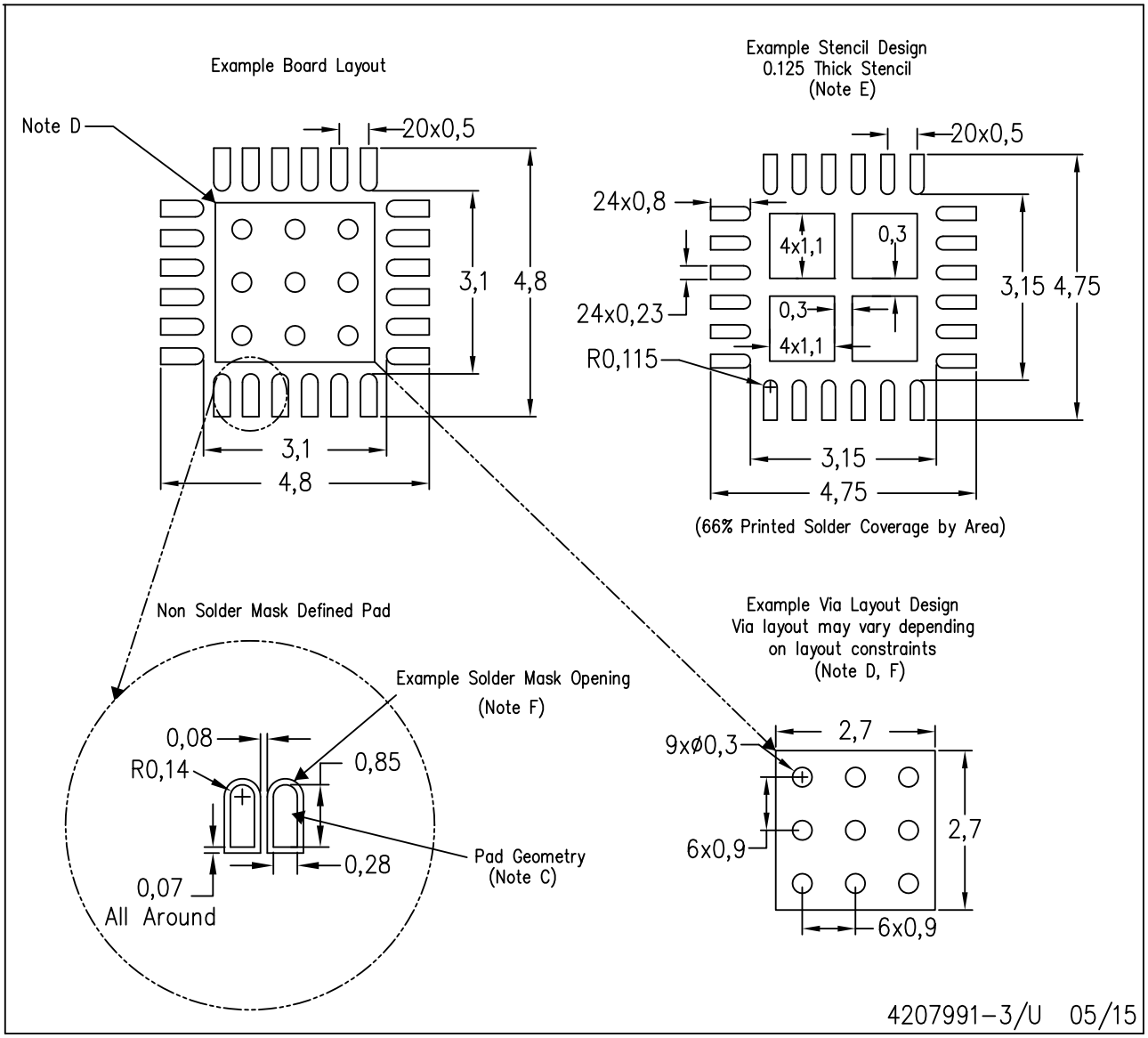
LAND PATTERN DATA

RGE (S-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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