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LM3241 6MHz, 750mA Miniature, Adjustable, Step-Down DC-DC Converter for RF Power Amplifiers

Check for Samples: LM3241

FEATURES

- **6MHz (typ.) PWM Switching Frequency**
- **Operates from a Single Li-Ion Cell (2.7V to 5.5V)**
- **Adjustable Output Voltage (0.6V to 3.4V)**
- **750 mA Maximum Load Capability**
- **High Efficiency (95% typ. at 3.9V_{IN}, 3.3V_{OUT} at 500 mA)**
- **Automatic ECO/PWM mode change**
- **6-bump DSBGA Package**
- **Current Overload Protection**
- **Thermal Overload Protection**
- **Soft Start Function**
- **C_{IN} and C_{OUT} are 0402 (1005) case size and 6.3V of rated-voltage ceramic capacitor**
- **Small Chip Inductor in 0805 (2012) case size**

APPLICATIONS

- **Battery-Powered 3G/4G Power Amplifiers**
- **Hand-Held Radios**
- **RF PC Cards**
- **Battery-Powered RF Devices**

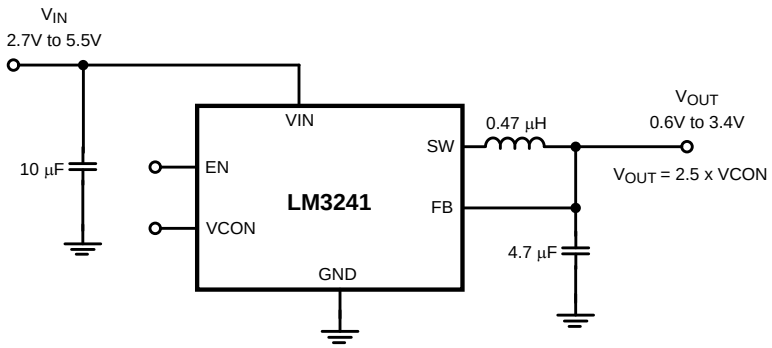
DESCRIPTION

The LM3241 is a DC-DC converter optimized for powering RF power amplifiers (PAs) from a single Lithium-Ion cell; however, it may be used in many other applications. It steps down an input voltage from 2.7V to 5.5V to an adjustable output voltage from 0.6V to 3.4V. Output voltage is set using a VCON analog input for controlling power levels and efficiency of the RF PA.

The LM3241 offers three modes of operation. In PWM mode the device operates at a fixed frequency of 6MHz (typ.) which minimizes RF interference when driving medium-to-heavy loads. At light load, the device enters into ECO mode automatically and operates with reduced switching frequency. In ECO mode, the quiescent current is reduced and extends the battery life. Shutdown mode turns the device off and reduces battery consumption to 0.1 µA (typ.).

The LM3241 is available in a 6-bump lead-free DSBGA package. A high-switching frequency (6MHz) allows use of tiny surface-mount components. Only three small external surface-mount components, an inductor and two ceramic capacitors are required.

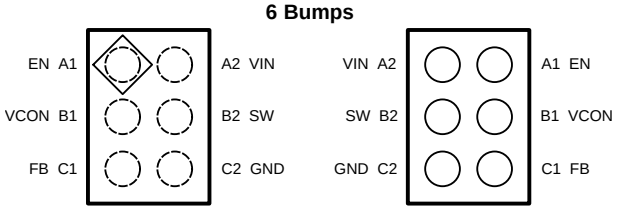
TYPICAL APPLICATION



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Thin DSBGA Package, Large Bump (0.5 mm Pitch) (YZR06E1A)
6 Bumps



Top View Bottom View

PIN DESCRIPTIONS

Pin #	Name	Description
A1	EN	Enable Input. Set this digital input high for normal operation. For shutdown, set low. Do not leave EN pin floating.
B1	VCON	Voltage Control Analog input. VCON controls VOUT in PWM mode. Do not leave VCON pin floating. V_{OUT} = 2.5 x VCON.
C1	FB	Feedback Analog Input. Connect to the output at the output inductor.
C2	GND	Ground
B2	SW	Switching Node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the maximum Switch Peak Current Limit specification of the LM3241.
A2	VIN	Power supply input. Connect to the input filter capacitor (Typical Application Circuit).

ABSOLUTE MAXIMUM RATINGS (1) (2)

VIN to GND	−0.2V to +6.0V
EN, FB, VCON, SW	(GND−0.2V) to (VIN+0.2V) w/ 6.0V
Continuous Power Dissipation (3)	Internally Limited
Junction Temperature (T_{J-MAX})	+150°C
Storage Temperature Range	−65°C to +150°C
Maximum Lead Temperature (Soldering, 10 sec)	+260°C
ESD Rating (4) Human Body Model: Charged Device Model:	 2kV 1250V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pins.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 125°C (typ.).
(4) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. (MIL-STD-883 3015.7)

OPERATING RATINGS (1) (2)

Input Voltage Range	2.7V to 5.5V
Recommended Load Current	0mA to 750 mA
Junction Temperature (T_J) Range	−30°C to +125°C
Ambient Temperature (T_A) Range (3)	−30°C to +85°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pins.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

THERMAL PROPERTIES

Junction-to-Ambient Thermal Resistance (θ_{JA}), YZR06 Package (1)	85°C/W

(1) Junction-to-ambient thermal resistance (θ_{JA}) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7.

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{FB,MIN}$	Feedback voltage at minimum setting	PWM mode, VCON = 0.24V	**0.58**	0.6	**0.62**	V
$V_{FB,MAX}$	Feedback voltage at maximum setting	PWM mode, VCON = 1.36V, V_{IN} = 3.9V	**3.332**	3.4	**3.468**	
I_{SHDN}	Shutdown supply current	EN = SW = VCON = 0V (4)		0.1	**2**	µA
I_{Q}_PWM	PWM mode Quiescent current	PWM mode, No switching VCON = 0V, FB = 1V (5)		620	**750**	µA
I_{Q}_ECO	ECO mode Quiescent current	ECO mode, No switching VCON = 0.8V, FB = 2.05V (5)		45	**60**	
$R_{DSON\ (P)}$	Pin-pin resistance for PFET	V_{IN} = V_{GS} = 3.6V I_{SW} = 200 mA		160	**250**	mΩ
$R_{DSON\ (N)}$	Pin-pin resistance for NFET	V_{IN} = V_{GS} = 3.6V I_{SW} = −200 mA		110	**200**	
I_{LIM}	PFET switch peak current limit	(6)	**1300**	1450	**1600**	mA
F_{OSC}	Internal oscillator frequency		**5.7**	6	**6.3**	MHz
V_{IH}	EN Logic high input threshold		**1.2**			V
V_{IL}	EN Logic low input threshold				**0.4**	
Gain	VCON to V_{OUT} gain	0.24V ≤ VCON ≤ 1.36V		2.5		V/V
I_{CON}	VCON pin leakage current	VCON = 1.0V			**±1**	µA

(1) All voltages are with respect to the potential at the GND pins.
(2) Min and Max limits are specified by design, test, or statistical analysis.
(3) **The parameters in the electrical characteristics table are tested under open loop conditions at V_{IN} = 3.6V unless otherwise specified. For performance over the input voltage range and closed-loop results, refer to the datasheet curves.**
(4) Shutdown current includes leakage current of PFET.
(5) I_Q specified here is when the part is not switching under test mode conditions. For operating quiescent current at no load, refer to datasheet curves.
(6) Current limit is built-in, fixed, and not adjustable.

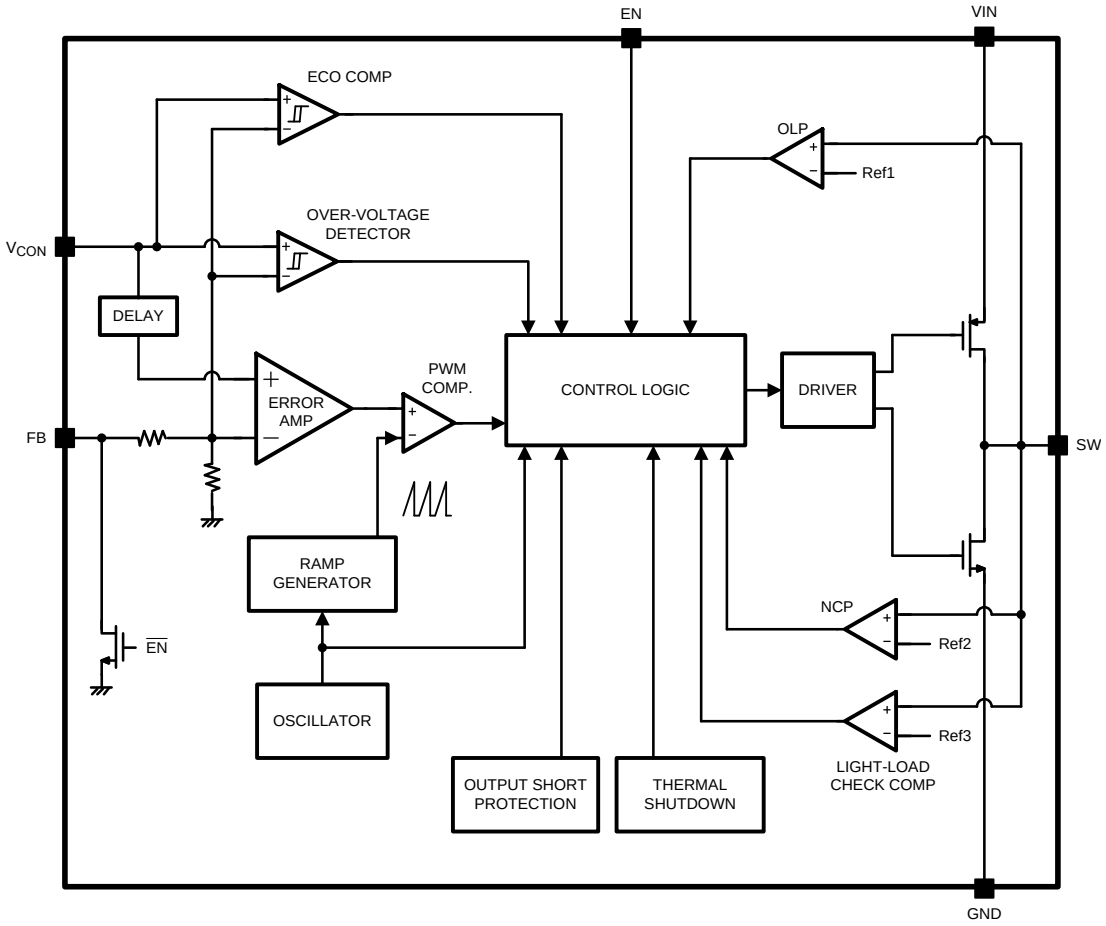
SYSTEM CHARACTERISTICS

The following spec table entries are guaranteed by design providing the component values in the Typical Application Circuit are used. **These parameters are not verified by production testing.** Min and Max values apply over the full operating ambient temperature range (-30°C ≤ T_A ≤ 85°C) and over the V_{IN} range = 2.7V to 5.5V unless otherwise specified. L = 0.47 µH, DCR = 50 mΩ, C_{IN} = 10 µF, 6.3V, 0603 (1608), C_{OUT} = 4.7 µF, 6.3V, 0603 (1608).

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{CON\ TR}$	V_{OUT} step rise time from 0.6V to 3.4V (to reach 3.26V)	V_{IN} = 3.6V, VCON = 0.24V to 1.36V VCON T_R = 1 µs, R_{LOAD} = 10Ω			25	µs
	V_{OUT} step fall time from 3.4V to 0.6V (to reach 0.74V)	V_{IN} = 3.6V, VCON = 1.36V to 0.24V VCON T_F = 1 µs, R_{LOAD} = 10Ω			25	
D	Maximum Duty cycle		100			%
I_{OUT}	Maximum output current capability	2.7V ≤ V_{IN} ≤ 5.5V 0.24V ≤ VCON ≤ 1.36V	750			mA
C_{CON}	VCON input capacitance	VCON = 1V Test frequency = 100 KHz		5	10	pF
Linearity	Linearity in control range 0.24V to 1.36V	Monotronic in nature (1)	−3		+3	%
			−50		+50	mV
T_{ON}	Turn-on time (time for output to reach 95% final value after Enable low-to-high transition)	EN = Low-to-High V_{IN} = 4.2V, V_{OUT} = 3.4V I_{OUT} = < 1mA, C_{OUT} = 4.7 µF			50	µs
η	Efficiency	V_{IN} = 3.6V, V_{OUT} = 0.8V I_{OUT} = 10 mA, ECO mode		75		%
		V_{IN} = 3.6V, V_{OUT} = 1.8V I_{OUT} = 200 mA, PWM mode		90		
		V_{IN} = 3.9V, V_{OUT} = 3.3V I_{OUT} = 500 mA, PWM mode		95		
$LINE_{TR}$	Line transient response	V_{IN} = 3.6V to 4.2V, T_R = T_F = 10 µs, I_{OUT} = 100 mA, V_{OUT} = 0.8V		50		mVpk
$LOAD_{TR}$	Load transient response	V_{IN} = 3.1V/3.6V/4.5V, V_{OUT} = 0.8V, I_{OUT} = 50 mA to 150 mA T_R = T_F = 0.1 µs		50		

(1) Linearity limits are ±3% or ±50 mV whichever is larger.

BLOCK DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = EN = 3.6V and T_A = +25°C, unless otherwise noted.

Shutdown Current vs Temperature (SW=VCON=EN=0V)

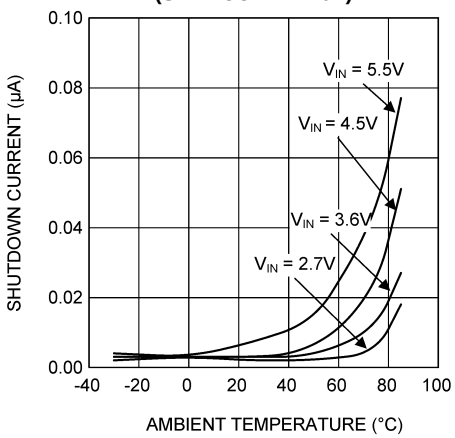


Figure 1.

Quiescent Current vs Supply Voltage (No switching, FB=1V, VCON=0V)

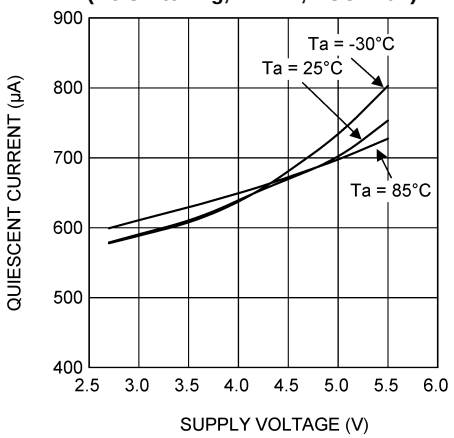


Figure 2.

ECO mode Supply Current vs Output Voltage (Closed loop, Switching, No load)

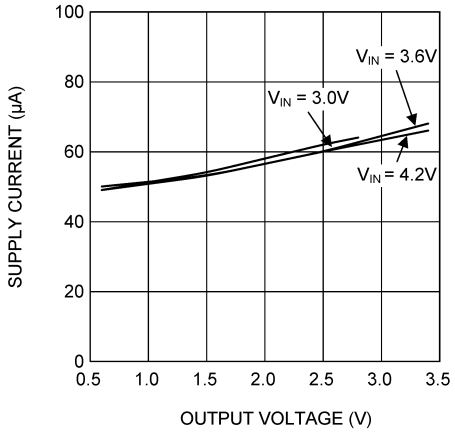


Figure 3.

Switching Frequency vs Temperature (V_{OUT}= 2.0V, I_{OUT}=200 mA)

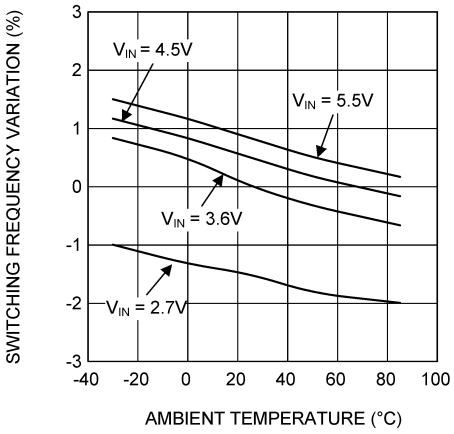


Figure 4.

Output Voltage vs Supply Voltage (V_{OUT}=2.0V, R_{LOAD}=10Ω)

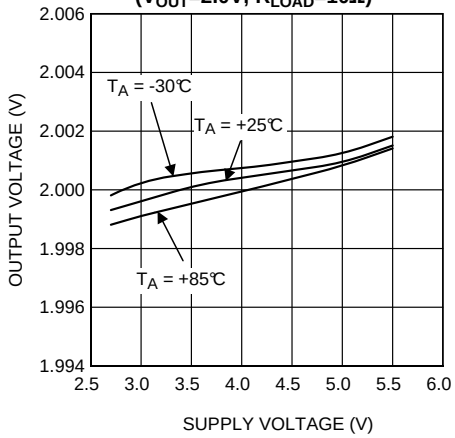


Figure 5.

Output Voltage vs Output Current (V_{OUT}=3.4V)

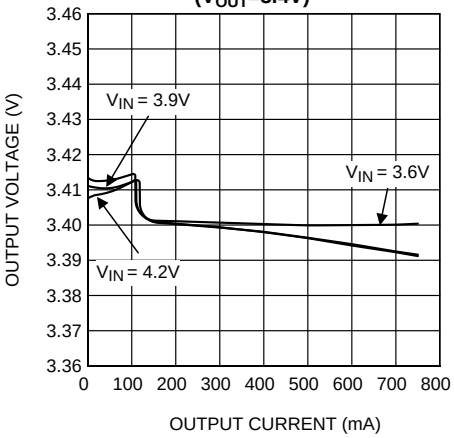


Figure 6.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = EN = 3.6V and T_A = +25°C, unless otherwise noted.

Output Voltage vs Output Current (V_{OUT}=0.6V)

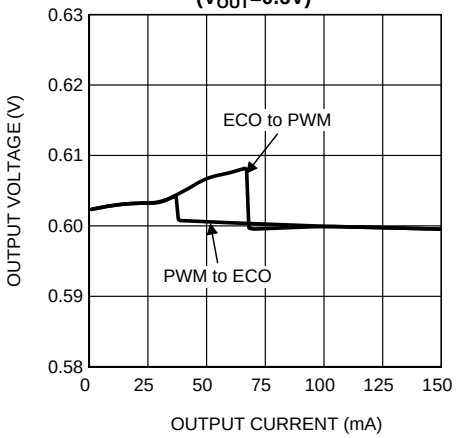


Figure 7.

Output Voltage vs Output Current (V_{OUT}=2.0V)

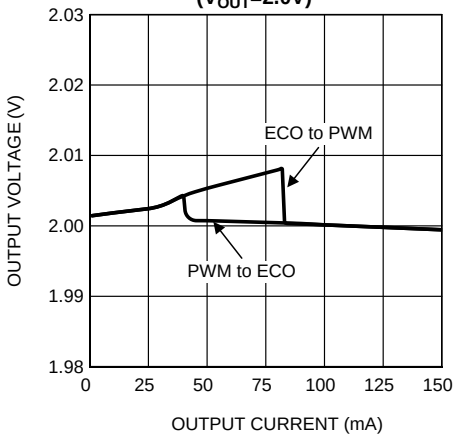


Figure 8.

ECO-PWM Mode Threshold Current vs Output voltage

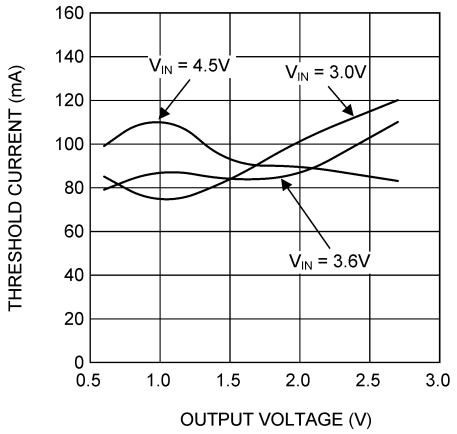


Figure 9.

PWM-ECO Mode Threshold Current vs Output voltage

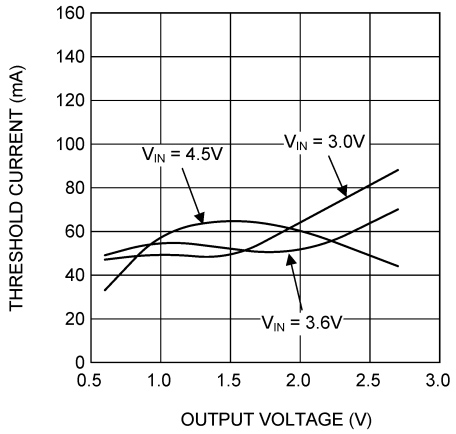


Figure 10.

Closed-loop Current Limit vs Temperature (V_{OUT}= 2.0V)

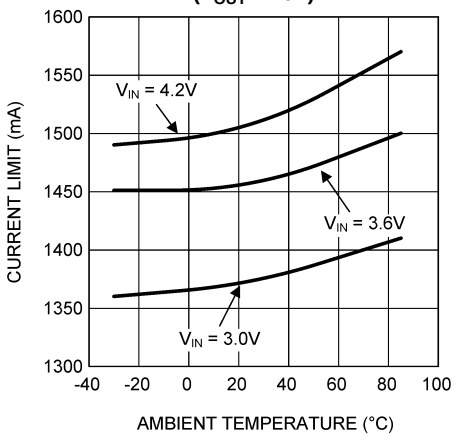


Figure 11.

Efficiency vs Output Current (V_{OUT}=0.8V)

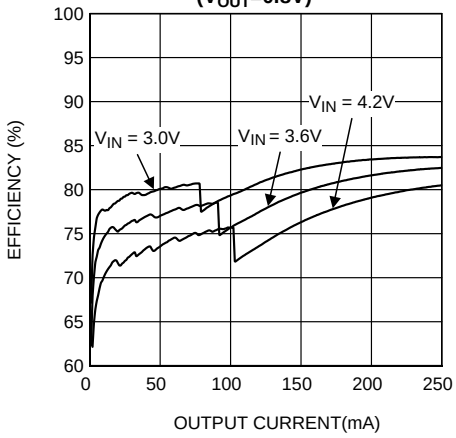


Figure 12.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = EN = 3.6V and T_A = +25°C, unless otherwise noted.

Efficiency vs Output Current (V_{OUT}=2.0V)

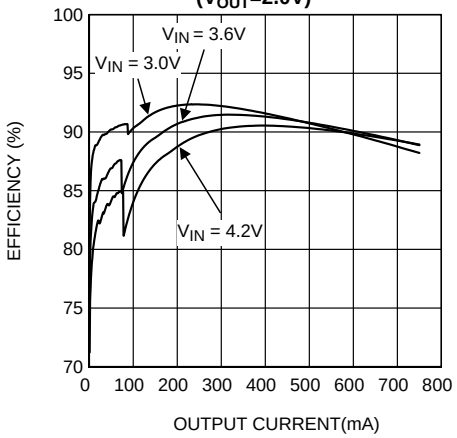


Figure 13.

Efficiency vs Output Current (V_{OUT}=3.3V)

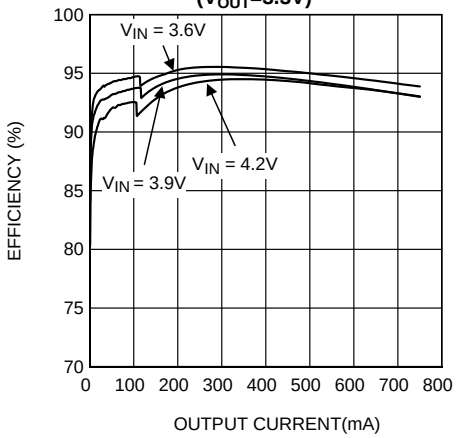


Figure 14.

Efficiency vs Output Voltage (R_{LOAD}=10Ω)

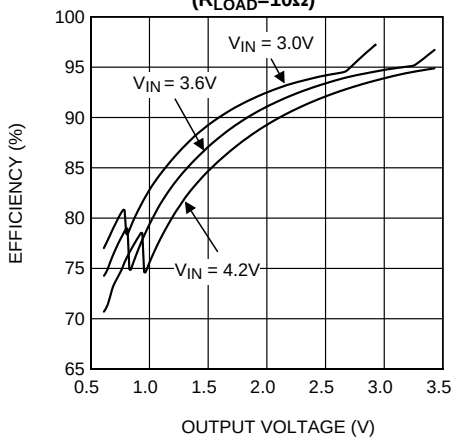


Figure 15.

PFET R_{DSON} vs Supply Voltage

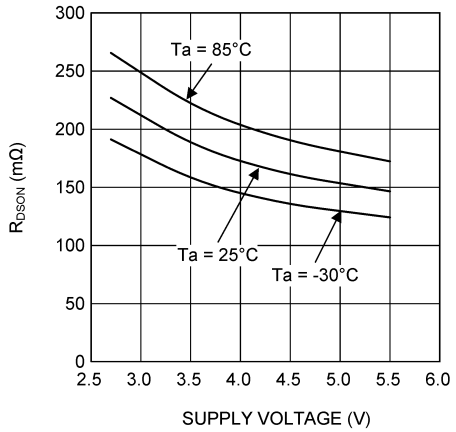


Figure 16.

NFET R_{DSON} vs Supply Voltage

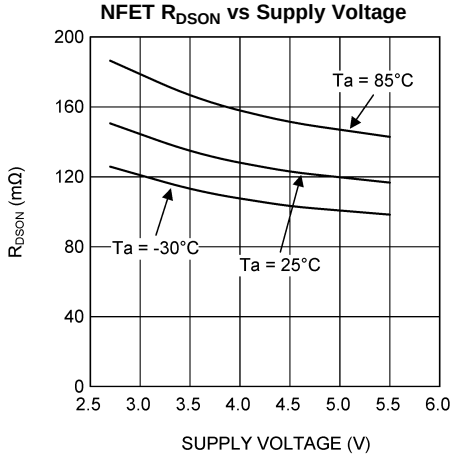


Figure 17.

Low VCON Voltage vs Output Voltage (R_{LOAD}=10Ω)

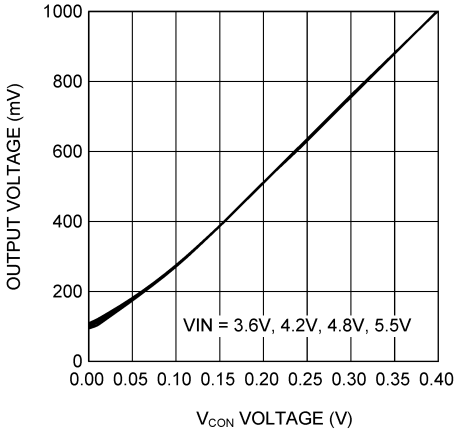


Figure 18.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = EN = 3.6V and T_A = +25°C, unless otherwise noted.

V_{IN}-V_{OUT} vs Output Current (100% Duty Cycle)

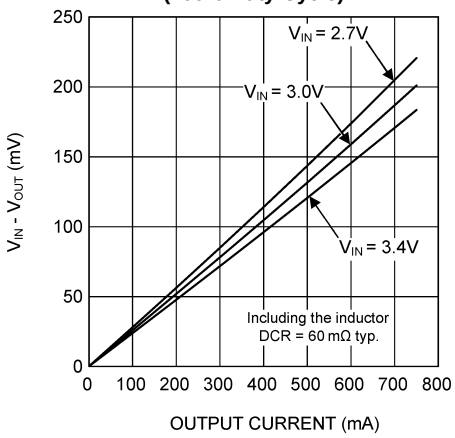


Figure 19.

EN High Threshold vs Supply Voltage

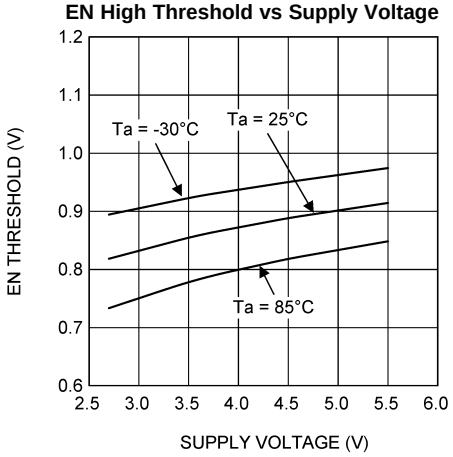


Figure 20.

Output Voltage Ripple in PWM Mode (V_{OUT}=2.0V, I_{OUT}=200 mA)

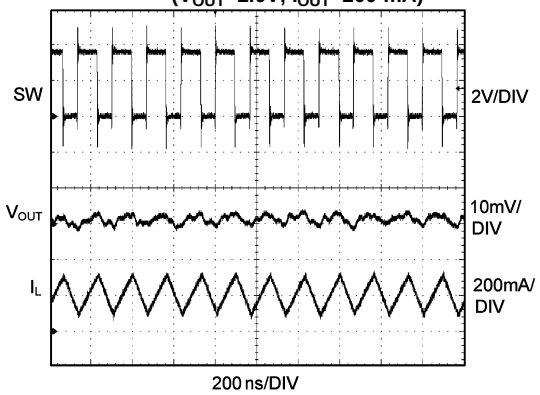


Figure 21.

Output Voltage Ripple in ECO Mode (V_{OUT}=2.0V, I_{OUT}=50 mA)

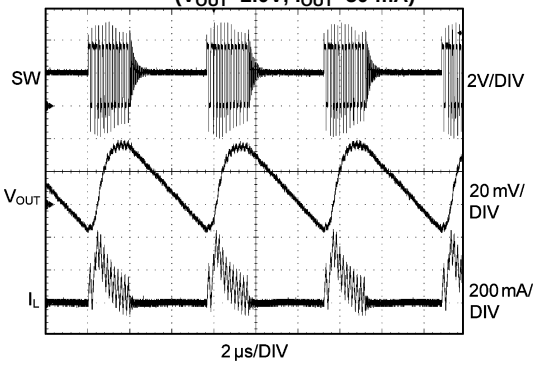


Figure 22.

VCON Transient Response (V_{OUT}=0.6V/3.4V, R_{LOAD}=10Ω)

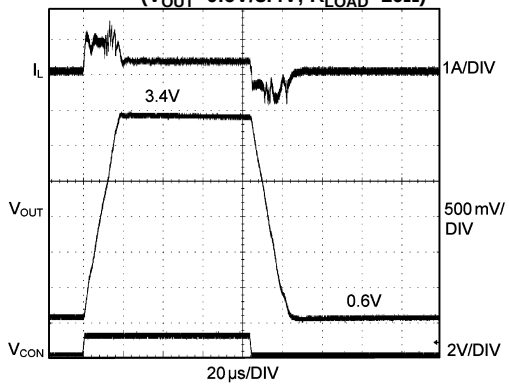


Figure 23.

Line Transient Response (V_{IN}=3.6V/4.2V, V_{OUT}=0.8V, R_{LOAD}=8Ω)

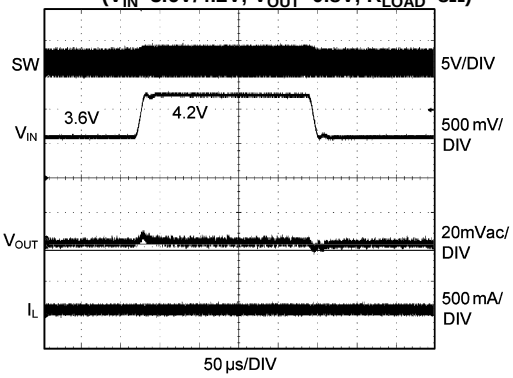


Figure 24.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = EN = 3.6V and T_A = +25°C, unless otherwise noted.

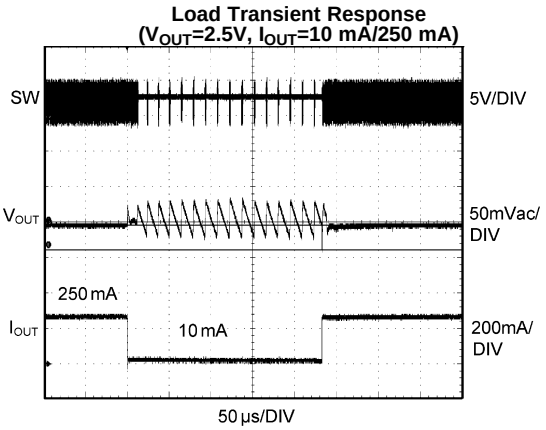


Figure 25.

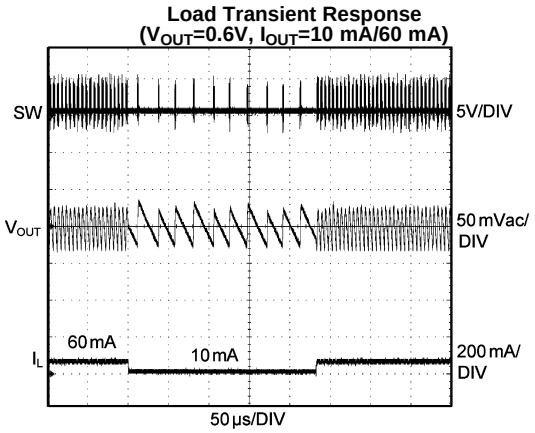


Figure 26.

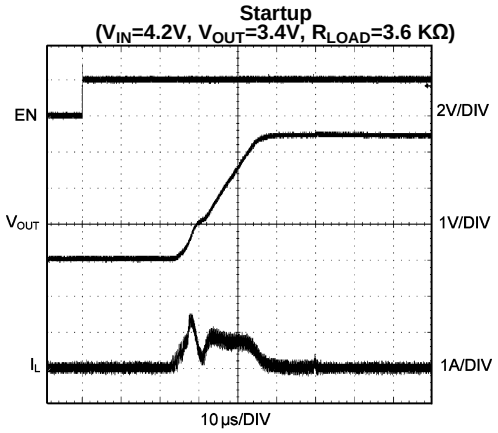


Figure 27.

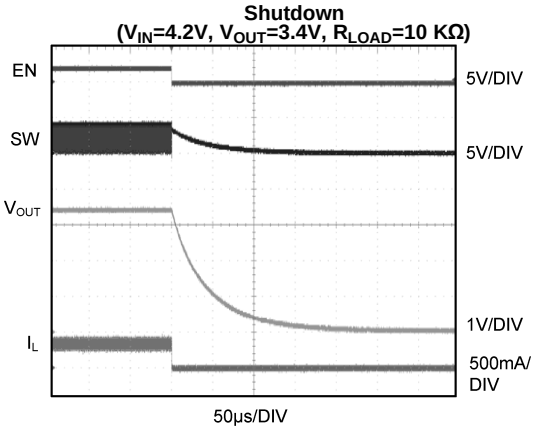


Figure 28.

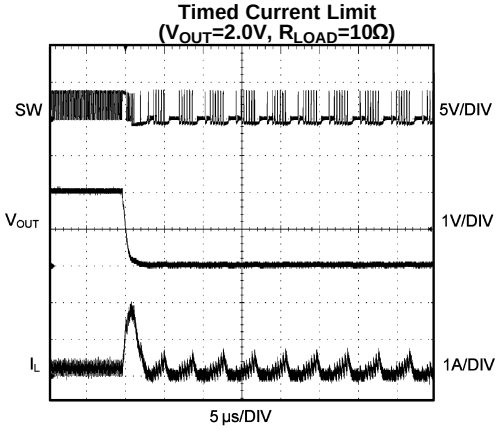


Figure 29.

FUNCTIONAL DESCRIPTION

Device Information

The LM3241 is a simple, step-down DC-DC converter optimized for powering RF power amplifiers (PAs) in mobile phones, portable communicators, and similar battery-powered RF devices. It is designed to allow the RF PA to operate at maximum efficiency over a wide range of power levels from a single Li-Ion battery cell. It is based on a voltage-mode buck architecture, with synchronous rectification for high efficiency. It is designed for a maximum load capability of 750 mA in PWM mode. Maximum load range may vary from this depending on input voltage, output voltage and the inductor chosen.

There are three modes of operation depending on the current required: PWM (Pulse Width Modulation), ECO (ECOnomy), and shutdown. The LM3241 operates in PWM mode at higher load current conditions. Lighter loads cause the device to automatically switch into ECO mode. Shutdown mode turns the device off and reduces battery consumption to 0.1 µA (typ.).

DC PWM mode output voltage precision is ±2% for $3.4V_{OUT}$. Efficiency is typically around 95% (typ.) for a 500 mA load with 3.3V output, 3.9V input. The output voltage is dynamically programmable from 0.6V to 3.4V by adjusting the voltage on the control pin (VCON) without the need for external feedback resistors. This ensures longer battery life by being able to change the PA supply voltage dynamically depending on its transmitting power.

Additional features include current overload protection and thermal overload shutdown.

The LM3241 is constructed using a chip-scale 6-bump DSBGA package. This package offers the smallest possible size for space-critical applications, such as cell phones, where board area is an important design consideration. Use of a high switching frequency (6MHz, typ.) reduces the size of external components. As shown in the Typical Application Circuit, only three external power components are required for implementation. Use of a DSBGA package requires special design considerations for implementation. (See DSBGA Package Assembly and Use in the APPLICATION INFORMATION section.) Its fine-bump pitch requires careful board design and precision assembly equipment. Use of this package is best suited for opaque-case applications, where its edges are not subject to high-intensity ambient red or infrared light. Also, the system controller should set EN low during power-up and other low supply voltage conditions. (See Shutdown Mode below.)

Circuit Operation

Referring to the Typical Application Circuit and the BLOCK DIAGRAM, the LM3241 operates as follows. During the first part of each switching cycle, the control block in the LM3241 turns on the internal top-side PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of around $(V_{IN} - V_{OUT}) / L$, by storing energy in a magnetic field. During the second part of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the bottom-side NFET synchronous rectifier on. In response, the inductor's magnetic field collapses, generating a voltage that forces current from ground through the synchronous rectifier to the output filter capacitor and load. As the stored energy is transferred back into the circuit and depleted, the inductor current ramps down with a slope around V_{OUT} / L. The output filter capacitor stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at SW to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

PWM Mode Operation

While in PWM mode operation, the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage is introduced. While in PWM mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

ECO Mode Operation

At very light loads (50 mA to 100 mA), the LM3241 enters ECO mode operation with reduced switching frequency and supply current to maintain high efficiency. During ECO mode operation, the LM3241 positions the output voltage slightly higher (+7mV typ.) than the normal output voltage during PWM mode operation, allowing additional headroom for voltage drop during a load transient from light to heavy load.

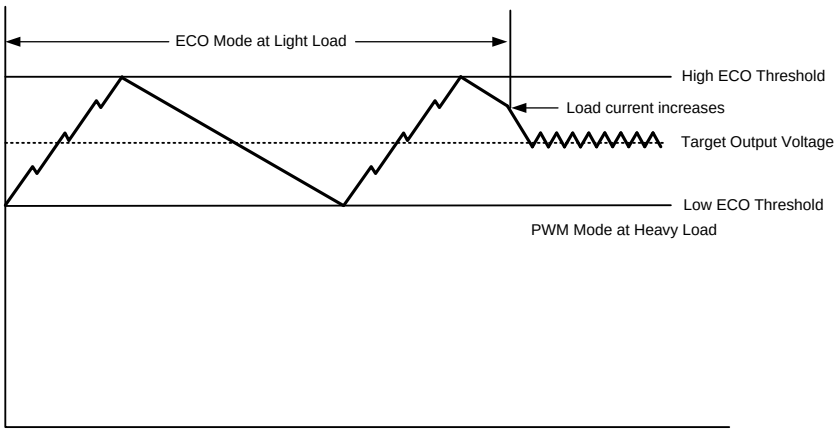


Figure 30. Operation in ECO Mode and Transfer to PWM Mode

Shutdown Mode

Setting the EN digital pin low (<0.4V) places the LM3241 in Shutdown mode (0.1 µA typ.). During shutdown, the PFET switch, the NFET synchronous rectifier, reference voltage source, control and bias circuitry of the LM3241 are turned off. Setting EN high (>1.2V) enables normal operation. EN should be set low to turn off the LM3241 during power-up and undervoltage conditions when the power supply is less than the 2.7V minimum operating voltage. The LM3241 has an UVLO (Under Voltage Lock Out) comparator to turn the power device off in the case the input voltage or battery voltage is too low. The typical UVLO threshold is around 2.0V for lock and 2.1V for release.

Internal Synchronization Rectification

While in PWM mode, the LM3241 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

With medium and heavy loads, the NFET synchronous rectifier is turned on during the inductor current down slope in the second part of each cycle. The synchronous rectifier is turned off prior to the next cycle. The NFET is designed to conduct through its intrinsic body diode during transient intervals before it turns on, eliminating the need for an external diode.

Current Limiting

The current limit feature allows the LM3241 to protect itself and external components during overload conditions. In PWM mode, the cycle-by-cycle current limit is 1450 mA (typ.). If an excessive load pulls the output voltage down to less than 0.3V (typ.), the NFET synchronous rectifier is disabled, and the current limit is reduced to 530 mA (typ.). Moreover, when the output voltage becomes less than 0.15V (typ.), the switching frequency will decrease to 3MHz, thereby preventing excess current and thermal stress.

Dynamically Adjustable Output Voltage

The LM3241 features dynamically adjustable output voltage to eliminate the need for external feedback resistors. The output can be set from 0.6V to 3.4V by changing the voltage on the analog VCON pin. This feature is useful in PA applications where peak power is needed only when the handset is far away from the base station or when data is being transmitted. In other instances the transmitting power can be reduced. Hence the supply voltage to the PA can be reduced, promoting longer battery life. See Setting the Output Voltage in the APPLICATION INFORMATION section for further details. The LM3241 moves into Pulse Skipping mode when duty cycle is over approximately 92% or less than approximately 15%, and the output voltage ripple increases slightly.

Thermal Overload Protection

The LM3241 has a thermal overload protection function that operates to protect itself from short-term misuse and overload conditions. When the junction temperature exceeds around 150°C, the device inhibits operation. Both the PFET and the NFET are turned off. When the temperature drops below 125°C, normal operation resumes. Prolonged operation in thermal overload conditions may damage the device and is considered bad practice.

Soft Start

The LM3241 has a soft-start circuit that limits in-rush current during startup. During startup the switch current limit is increased in steps. Soft start is activated if EN goes from low to high after V_{IN} reaches 2.7V.

APPLICATION INFORMATION

Setting the Output Voltage

The LM3241 features a pin-controlled adjustable output voltage to eliminate the need for external feedback resistors. It can be programmed for an output voltage from 0.6V to 3.4V by setting the voltage on the VCON pin, as in the following formula:

$$V_{OUT} = 2.5 \times VCON \quad (1)$$

When VCON is between 0.24V and 1.36V, the output voltage will follow proportionally by 2.5 times of VCON.

If VCON is less than 0.24V (V_{OUT} = 0.6V), the output voltage may be regulated. Refer to datasheet curve (Low VCON Voltage vs. Output Voltage) for details. This curve exhibits the characteristics of a typical part, and the performance cannot be guaranteed as there could be a part-to-part variation for output voltages less than 0.6V. For V_{OUT} lower than 0.6V, the converter might suffer from larger output ripple voltage and higher current limit operation.

Inductor Selection

There are two main considerations when choosing an inductor: the inductor should not saturate, and the inductor current ripple should be small enough to achieve the desired output voltage ripple. Different manufacturers follow different saturation current rating specifications, so attention must be given to details. Saturation current ratings are typically specified at 25°C so ratings over the ambient temperature of application should be requested from manufacturer.

Minimum value of inductance to guarantee good performance is 0.3 µH at bias current (I_{LIM} (typ.)) over the ambient temperature range. Shielded inductors radiate less noise and should be preferred. There are two methods to choose the inductor saturation current rating.

Method 1:

The saturation current should be greater than the sum of the maximum load current and the worst case average to peak inductor current. This can be written as:

$$I_{SAT} > I_{OUT\_MAX} + I_{RIPPLE}$$

where

$$I_{RIPPLE} = \left(\frac{V_{IN} - V_{OUT}}{2 \times L}\right) \times \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{f}\right)$$

- I_{RIPPLE}: average-to-peak inductor current
- I_{OUT_MAX}: maximum load current (750 mA)
- V_{IN}: maximum input voltage in application
- L: minimum inductor value including worst-case tolerances (30% drop can be considered for Method 1)
- F: minimum switching frequency (5.7 MHz)
- V_{OUT}: output voltage

Method 2:

A more conservative and recommended approach is to choose an inductor that can handle the maximum current limit of 1600 mA.

The inductor's resistance should be less than around 0.1Ω for good efficiency. Table 1 lists suggested inductors and suppliers.

Table 1. Suggested Inductors

Model	Size (W x L x H) (mm)	Vendor
MIPSZ2012D0R5	2.0 x 1.2 x 1.0	FDK
LQM21PNR54MG0	2.0 x 1.25 x 0.9	Murata
LQM2MPNR47NG0	2.0 x 1.6 x 0.9	Murata

Capacitor Selection

The LM3241 is designed for use with ceramic capacitors for its input and output filters. Use a 10 µF ceramic capacitor for input and a 4.7 µF ceramic capacitor for output. They should maintain at least 50% capacitance at DC bias and temperature conditions. Ceramic capacitors type such as X5R, X7R, and B are recommended for both filters. They provide an optimal balance between small size, cost, reliability and performance for cell phones and similar applications. Table 2 lists some suggested part numbers and suppliers. DC bias characteristics of the capacitors must be considered when selecting the voltage rating and case size of the capacitor. For C_{IN}, use of an 0805 (2012) size may also be considered if there is room on the system board.

Table 2. Suggested Capacitors

Capacitance, Voltage Rating, Case Size	Model	Vendor
4.7 µF, 6.3V, 0603	C1608X5R0J475M	TDK
4.7 µF, 6.3V, 0402	C1005X5R0J475M	TDK
4.7 µF, 6.3V, 0402	CL05A475MQ5NRNC	Samsung
10 µF, 6.3V, 0603	C1608X5R0J106M	TDK
10 µF, 6.3V, 0402	CL05A106MQ5NUNC	Samsung

The input filter capacitor supplies AC current drawn by the PFET switch of the LM3241 in the first part of each cycle and reduces the voltage ripple imposed on the input power source. The output filter capacitor absorbs the AC inductor current, helps maintain a steady output voltage during transient load changes, and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR (Equivalent Series Resistance) to perform these functions. The ESR of the filter capacitors is generally a major factor in voltage ripple.

DSBGA Package Assembly and Use

Use of the DSBGA package requires specialized board layout, precision mounting and careful re-flow techniques, as detailed in Texas Instruments Application Note 1112. Refer to the section *Surface Mount Technology (SMD) Assembly Considerations.* For best results in assembly, alignment ordinals on the PC board should be used to facilitate placement of the device. The pad style used with DSBGA package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the solder-mask and pad overlap when holding the device off the surface of the board causing interference with mounting. See Application Note 1112 for specific instructions how to do this.

The 6-bump package used for LM3241 has 300 micron solder balls and requires 10.82 mil pads for mounting on the circuit board. The trace to each pad should enter the pad with a 90° angle to prevent debris from being caught in deep corners. Initially, the trace to each pad should be 7 mil wide, for a section approximately 7 mil long, as a thermal relief. Then each trace should neck up or down to its optimal width. The important criterion is symmetry. This ensures the solder bumps on the LM3241 re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps A2 and C2. Because VIN and GND are typically connected to large copper planes, inadequate thermal relief can result in late or inadequate re-flow of these bumps.

The DSBGA package is optimized for the smallest possible size in applications with red or infrared opaque cases. Because the DSBGA package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metallization and/or epoxy coating, along with front-side shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges. In particular, DSBGA devices are sensitive to light in the red and infrared range shining on the package's exposed die edges.

It is recommended that a 10 nF capacitor be added between VCON and ground for non-standard ESD events or environments and manufacturing processes. It prevents unexpected output voltage drift.

Board Layout Considerations

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability. Poor layout can also result in re-flow problems leading to poor solder joints between the DSBGA package and board pads — poor solder joints can result in erratic or degraded performance. Good layout for the LM3241 can be implemented by following a few simple design rules, as illustrated in Figure 31.

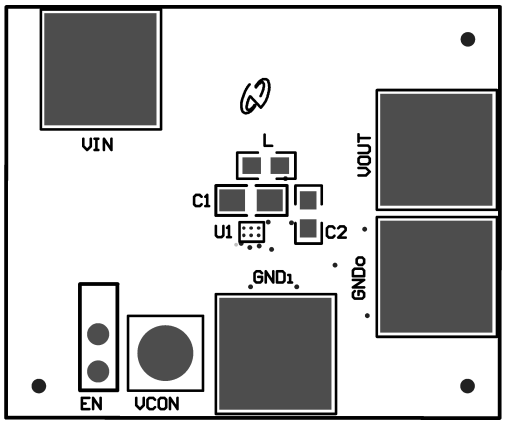
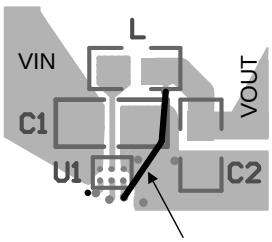


Figure 31. LM3241 Board Layout

1. Place the LM3241 on 10.82 mil pads. As a thermal relief, connect each pad with a 7mil wide, approximately 7mil long trace, and then incrementally increase each trace to its optimal width. V_{IN} and GND traces are especially recommended to be as wide as possible. The important criterion is symmetry to ensure the solder bumps re-flow evenly. (See AN-1112, *Surface Mount Technology (SMD) Assembly Considerations.*.)
2. Place the LM3241, inductor, and filter capacitors close together and make the traces short. The traces between these components carry relatively high switching current and act as antennae. Following this rule reduces radiated noise. **Special care must be given to place the input filter capacitor very close to the VIN and GND pads.**
3. Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor, through the LM3241 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the LM3241 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
4. Connect the ground pads of the LM3241 and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then connect this to the ground-plane (if one is used) with several vias. This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM3241 by giving it a low impedance ground connection.
5. Use side traces between the power components and for power connections to the DC-DC converter circuit. This reduces voltage errors caused by resistive losses across the traces.
6. Route noise sensitive traces such as the voltage feedback path away from noisy traces between the power components. The output voltage feedback point should be taken approximately 1.5 nH away from the output capacitor. The feedback trace also should be routed opposite to noise components. **The voltage feedback trace must remain close to the LM3241 circuit and should be routed directly from FB to VOUT at the inductor and should be routed opposite to noise components.** This allows fast feedback and reduces EMI radiated onto the DC-DC converter's own voltage feedback trace.



FB trace on another layer to be protected from noise.

7. Place noise-sensitive circuitry, such as radio IF blocks, away from the DC-DC converter, CMOS digital blocks, and other noisy circuitry. Interference with noise-sensitive circuitry in the system can be reduce through distance.

In mobile phones, for example, a common practice is to place the DC-DC converter on one corner of the board, arrange the CMOS digital circuitry around it (since this also generates noise), and then place sensitive preamplifiers and IF stages on the diagonally opposing corner. Often, the sensitive circuitry is shielded with a metal pan and power to it is post-regulated to reduce conducted noise, using low-dropout linear regulators.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3241TLE/NOPB	ACTIVE	DSBGA	YZR	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	H	Samples
LM3241TLX/NOPB	ACTIVE	DSBGA	YZR	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	H	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

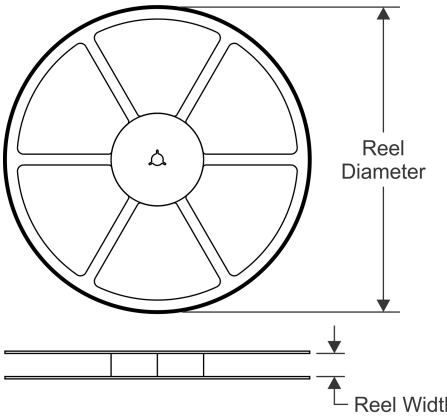
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

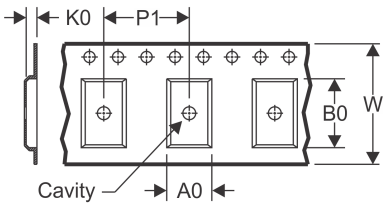
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

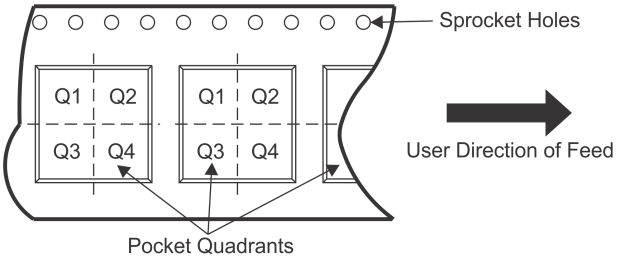


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

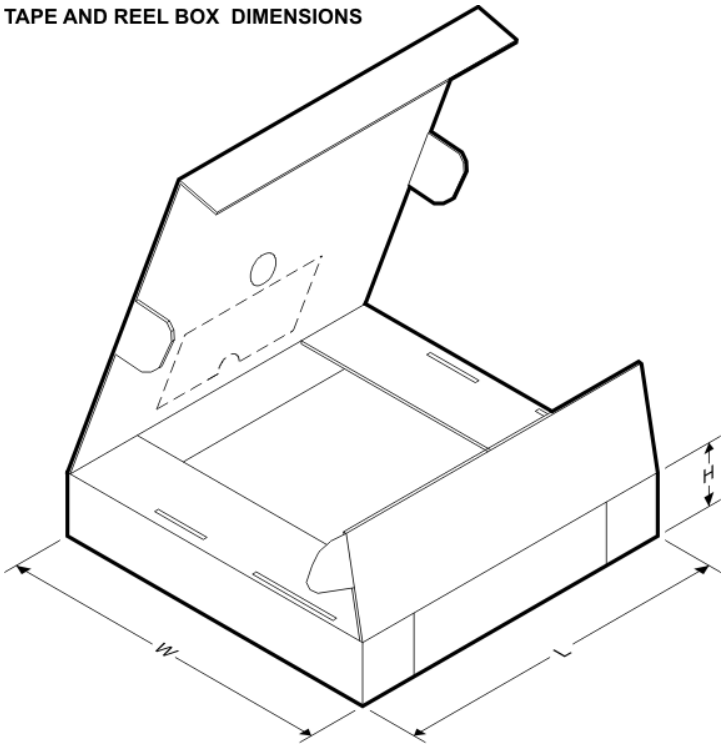


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3241TLE/NOPB	DSBGA	YZR	6	250	178.0	8.4	1.24	1.7	0.76	4.0	8.0	Q1
LM3241TLX/NOPB	DSBGA	YZR	6	3000	178.0	8.4	1.24	1.7	0.76	4.0	8.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

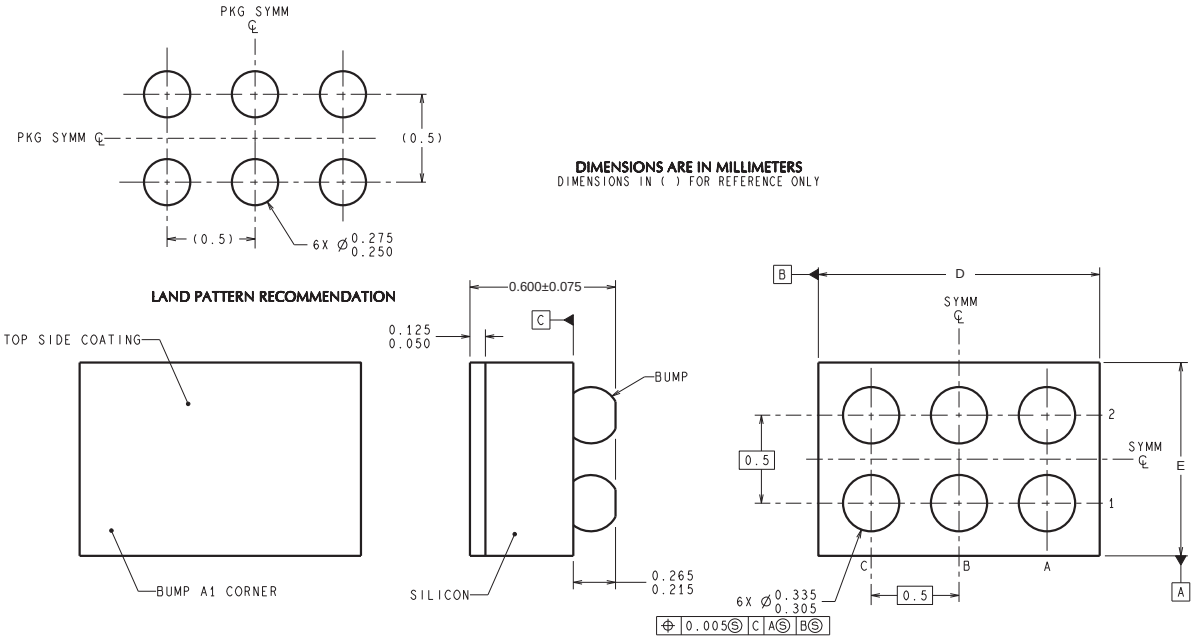


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3241TLE/NOPB	DSBGA	YZR	6	250	210.0	185.0	35.0
LM3241TLX/NOPB	DSBGA	YZR	6	3000	210.0	185.0	35.0

MECHANICAL DATA

YZR0006



TLA06XXX (Rev C)

D: Max = 1.51 mm, Min = 1.45 mm

E: Max = 1.12 mm, Min = 1.06 mm

4215044/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
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Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265