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Vishay/Siliconix
DG2599DN-T1-GE4

For any questions, you can email us directly:
sales@integrated-circuit.com

Low Voltage, Dual DPDT in miniQFN16

DESCRIPTION

The DG2599 is a C_{MOS} Dual DPDT (Dual Double Pole Double Throw) analog switch that operates over a wide voltage range of 1.65 V to 5 V. It is optimized for portable applications switching audio, SIM card signals, and other low power signals.

The DG2599 features low ON resistance of 2.8 Ω at 3 V power supply, fast switching speed, and low power consumption even when control logic signals are below V+ power supply voltage. The well matched dual DPDT switches conduct signals equally in both directions. The DG2599 is designed to guarantee break before make switching.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with lead (Pb)-free device terminations. DG2599 are offered in a miniQFN package. The miniQFN package has a nickel palladium- gold device termination and is represented by the lead (Pb)-free "-E4" suffix. The nickel-palladium-gold device terminations meet all JEDEC standards for reflow and MSL ratings.

FEATURES

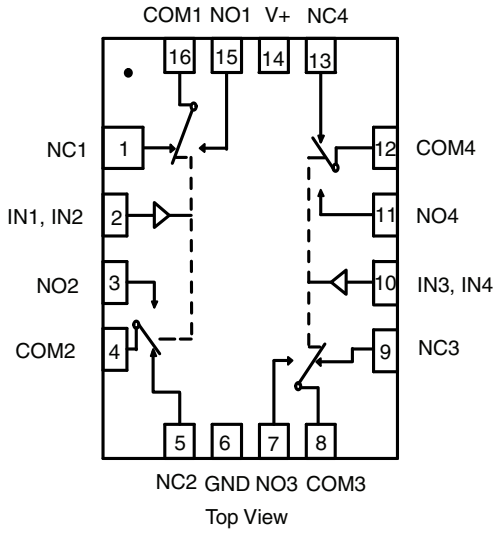
- **Halogen-free according to IEC 61249-2-21 definition**
- Low voltage operation - 1.65 V to 5 V
- Low on-resistance - 2.8 Ω at V+ = 3 V
- Power off protection on COM1 and COM2 pins
- Latch up current great than 300 mA per JESD78
- **Compliant to RoHS Directive 2002/95/EC**

Pb-free
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Cellular phones
- PMPs and PDAs
- Modems and peripherals
- Computers and ebooks
- Tablet devices
- Displays and gaming
- STB

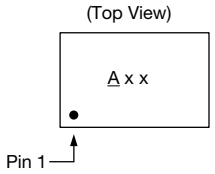
ORDERING INFORMATION	
Part Number	**Package**
DG2599DN-T1-GE4	miniQFN16 1.8 mm x 2.6 mm



Top View

TRUTH TABLE (DG2599)		
Logic	**NC1, 2, 3 and 4**	**NO 1, 2, 3 and 4**
0	ON	OFF
1	OFF	ON

Device Marking: A xx
xx = Date/Lot Traceability Code



Note: Pin 1 has long lead

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

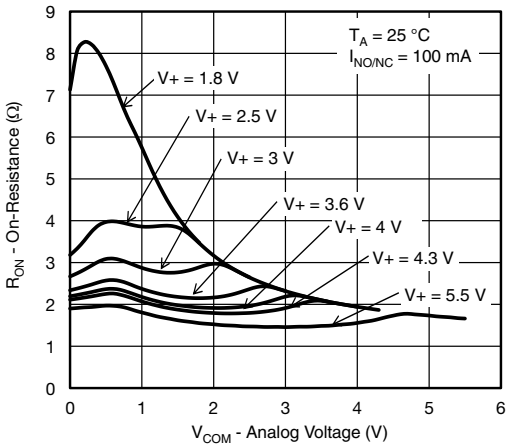
Parameter		Symbol	Limit	Unit
Reference to GND	V+		- 0.3 to 5	V
	IN, COM, NC, NO[a]		- 0.3 to (V+ + 0.3)	
Current (any terminal except NO, NC or COM)			30	mA
Continuous Current (NO, NC, or COM)			± 300	
Peak Current (pulsed at 1 ms, 10 % duty cycle)			± 500	
Storage Temperature (D Suffix)			- 65 to 150	°C
Package Solder Reflow Conditions[d]	miniQFN16		250	
Power Dissipation (Packages)[b]	miniQFN16[c]		525	mW

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 6.6 mW/°C above 70 °C.
d. Manual soldering with iron is not recommended for leadless components. The miniQFN-16 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

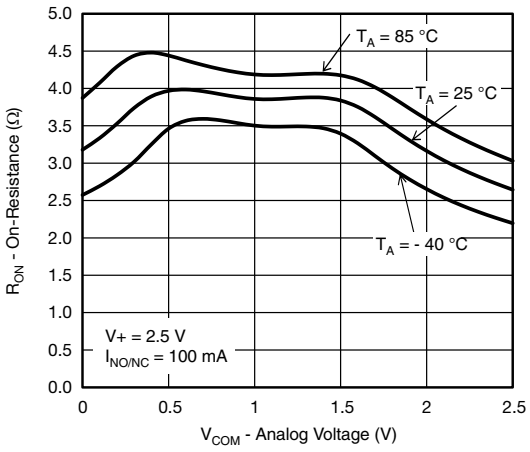
ELECTRICAL CHARACTERISTICS (V+ = 3 V)

Parameter	Test Conditions	Temp.	Min.	Typ.	Max.	Unit
Power Supply and Signal						
V+ Supply Voltage		Full	1.65		5	V
V+ Supply Current	V_{IN} = 0 or V+	Full		0.001	2	µA
Analog Signal Range		Full	0		V+	V
Switch On-Resistance and Leakage						
Drain-Source On-Resistance	V+ = 3 V, $I_{NO/NC}$ = 100 mA, V_{COM} = 0.9 V, 2.3 V	Room		2.8	3.3	Ω
		Full			3.6	
On-Resistance Flatness	V+ = 3 V, $I_{NO/NC}$ = 100 mA, V_{COM} = 0 to V+	Room		0.24	1.1	
		Full			1.3	
Switch Off Leakage Current	V+ = 4.3 V, $V_{NO/NC}$ = 0.3 V/4 V, V_{COM} = 4 V / 0.3 V	Room	- 10	0.1	10	nA
		Full	- 100		100	
Channel On-Leakage Current	V+ = 4.3 V, $V_{NO/NC}$ and V_{COM} = 0.3 V / 4 V	Room	- 10	0.1	10	
		Full	- 100		100	
Digital Control						
Input, High Voltage	V+ = 4.3 V	Full	1.6			V
	V+ = 3 V		1.3			
Input, Low Voltage	V+ = 4.3 V	Full			0.6	
	V+ = 3 V				0.5	
Input, Bias Current	V_{IN} = V+	Full	- 1	0.01	1	µA
Dynamic Characteristics						
Turn On-Time	V_{COM} or $V_{NO/NC}$ = 3 V, R_L = 50 Ω, C_L = 35 pF	Room			90	ns
		Full			115	
Turn Off-Time	V_{COM} or $V_{NO/NC}$ = 3 V, R_L = 50 Ω, C_L = 35 pF	Room			70	
		Full			85	
Break Before Make Time	V_{COM} or $V_{NO/NC}$ = 3 V, R_L = 50 Ω, C_L = 35 pF	Room	2			
		Full	2			
Charge Injection	C_L = 1 nF, R_{GEN} = 0 Ω	Room		± 10		pC
Off Isolation	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz			- 66		dB
Crosstalk	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz Non-adjacent channels			- 110		
3dB Bandwith	C_L = 5 pF, R_L = 50 Ω			186		MHz
Source Off Capacitance	V_{IN} = 0 or V+, f = 1 MHz			9		pF
Channel On Capacitance	V_{IN} = 0 or V+, f = 1 MHz			26		

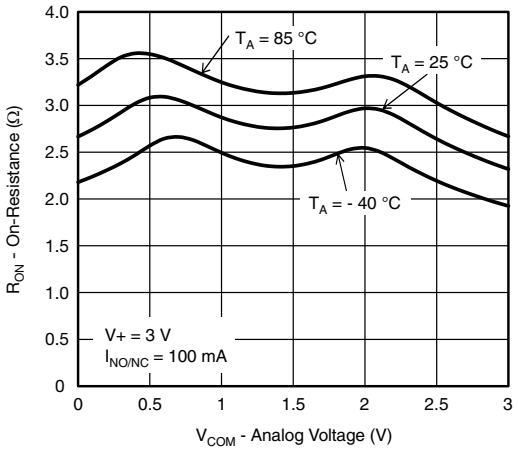
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



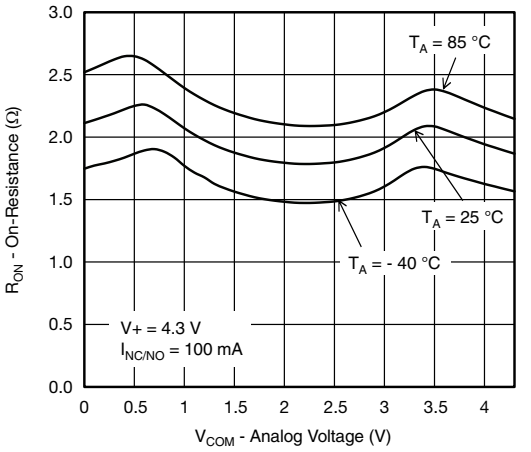
R_{ON} vs. V_{COM} and Single Supply Voltage



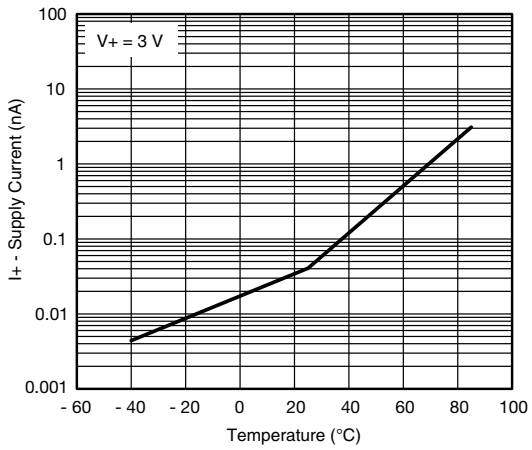
R_{ON} vs. Analog Voltage and Temperature



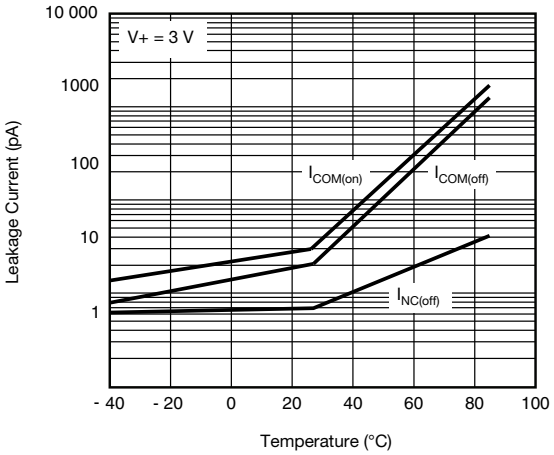
R_{ON} vs. Analog Voltage and Temperature



R_{ON} vs. Analog Voltage and Temperature

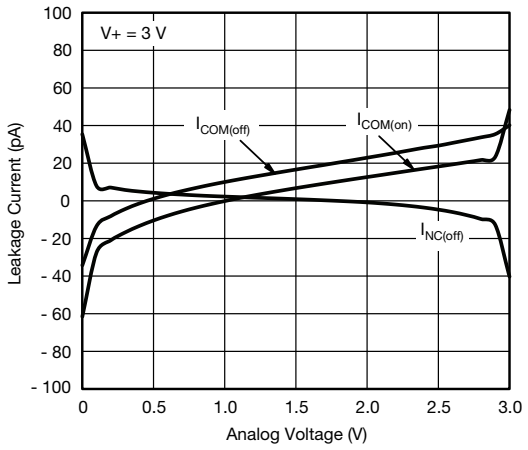


Supply Current vs. Temperature

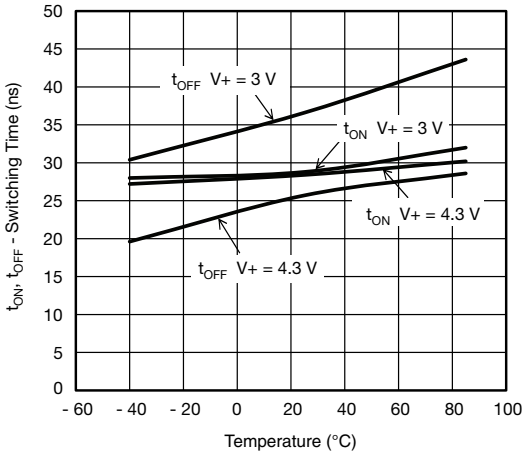


Leakage Current vs. Temperature

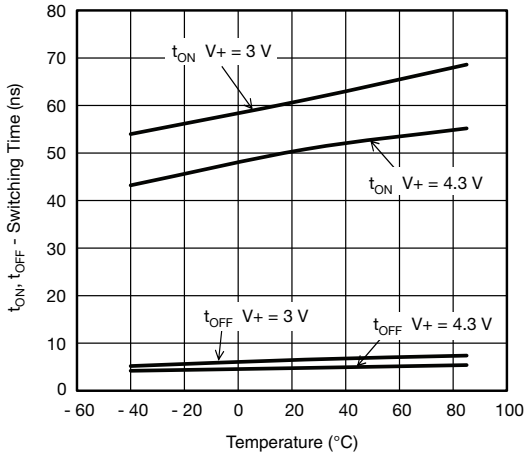
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



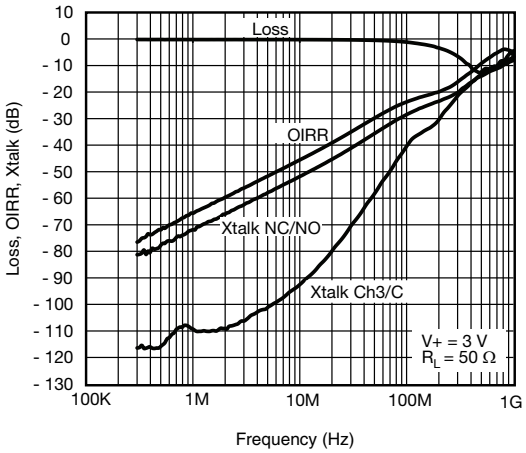
Leakage vs. Analog Voltage



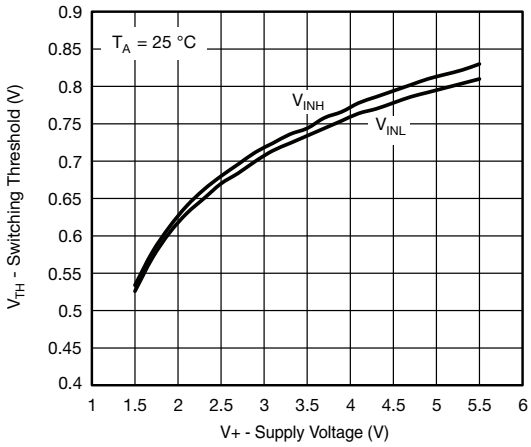
(NO) Switching Time vs. Temperature



(NC) Switching Time vs. Temperature

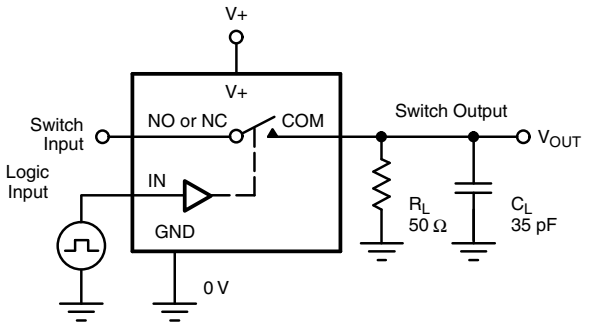


Insertion Loss, Off Isolation and Crosstalk



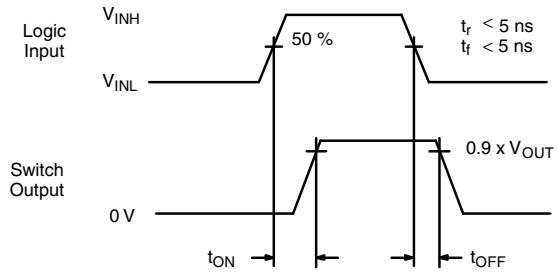
Switching Threshold vs. Supply Voltage

TEST CIRCUITS



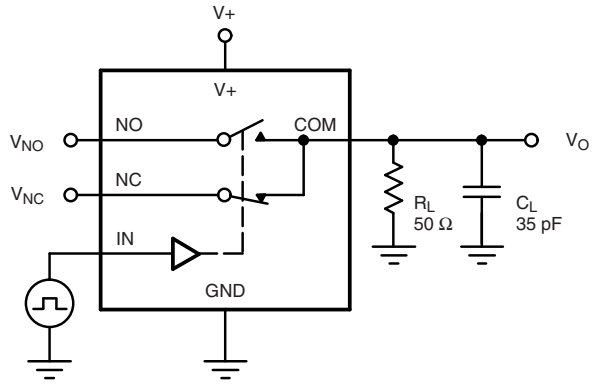
CL (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



CL (includes fixture and stray capacitance)

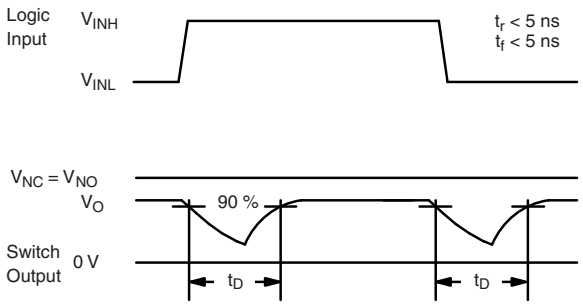
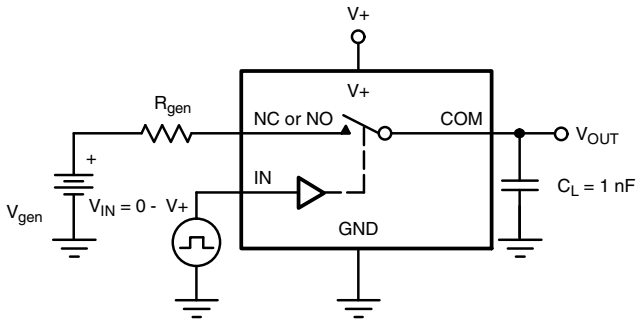
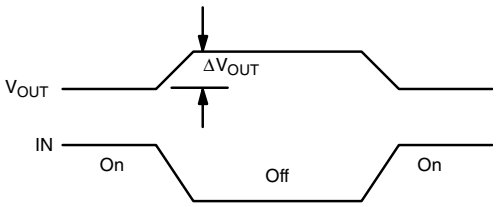


Figure 2. Break-Before-Make Interval





$$Q = \Delta V_{OUT} \times C_L$$

IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

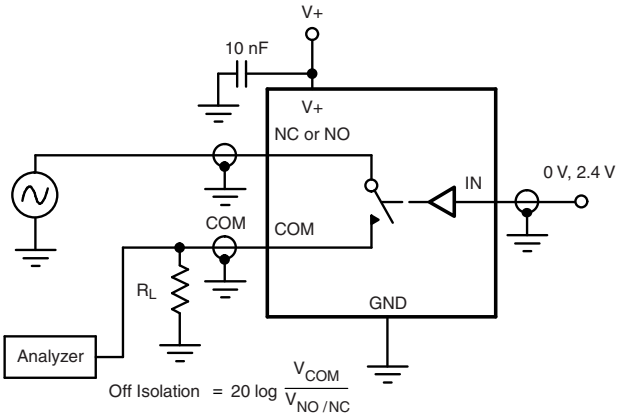


Figure 4. Off-Isolation

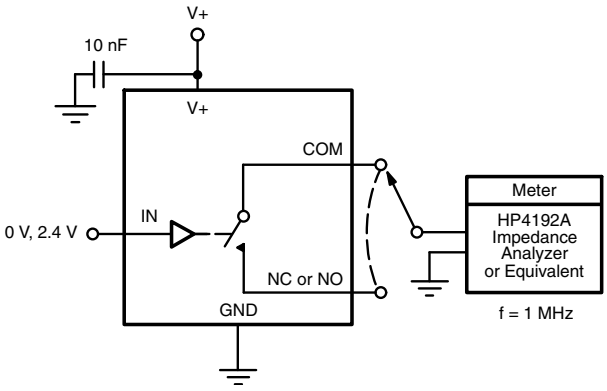
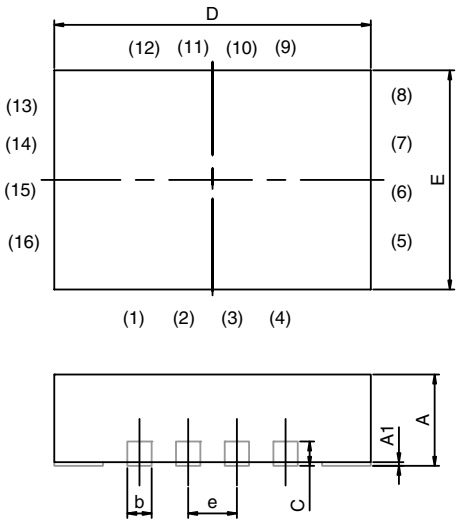
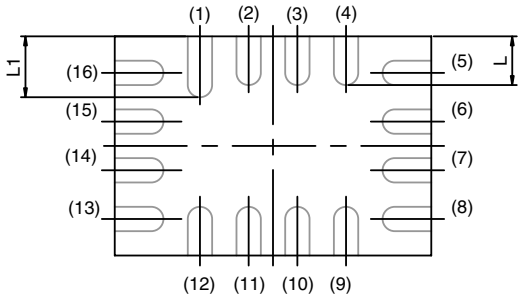


Figure 5. Channel Off/On Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67667.

miniQFN-16L



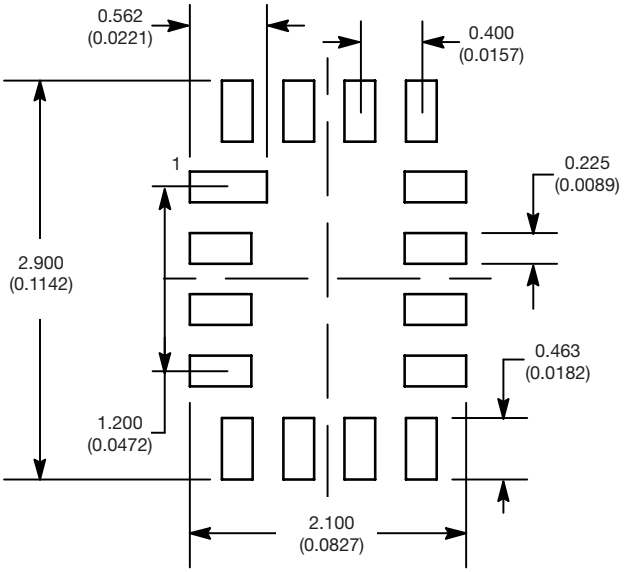


BACK SIDE VIEW

DIM	MILLIMETERS			INCHES		
	MIN.	NAM	MAX.	MIN.	NAM	MAX.
A	0.70	0.75	0.80	0.0275	0.0295	0.0315
A1	0	-	0.05	0	-	0.002
b	0.15	0.20	0.25	0.0059	0.0078	0.0098
C	0.15	0.20	0.25	0.0059	0.0078	0.0098
D	2.50	2.60	2.70	0.0984	0.1023	0.1063
E	1.70	1.80	1.90	0.0669	0.0708	0.0748
e	0.40 BSC			0.0157 BSC		
L	0.35	0.40	0.45	0.0137	0.0157	0.0177
L1	0.45	0.50	0.55	0.0177	0.0196	0.0216

ECN T16-0234-Rev. B, 09-May-16
DWG: 5954

RECOMMENDED MINIMUM PADS FOR MINI QFN 16L



Mounting Footprint
Dimensions in mm (inch)

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