

Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

[Fujitsu Semiconductor America Inc.](#)
[MB15E05SLPFV1-G-ER-6E1](#)

For any questions, you can email us directly:
sales@integrated-circuit.com

ASSP

Single Serial Input PLL Frequency Synthesizer On-chip 2.0 GHz Prescaler

MB15E05SL

DESCRIPTION

The Fujitsu MB15E05SL is a serial input Phase Locked Loop (PLL) frequency synthesizer with a 2.0 GHz prescaler. The 2.0 GHz prescaler has a dual modulus division ratio of 64/65 or 128/129 enabling pulse swallowing operation. The supply voltage range is between 2.4 V and 3.6 V. The MB15E05SL uses the latest BiCMOS process, as a result the supply current is typically 3.0 mA at 2.7 V. A refined charge pump supplies well-balanced output currents of 1.5 mA and 6 mA. The charge pump current is selectable by serial data.

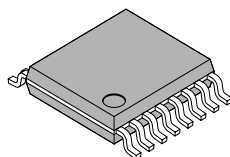
MB15E05SL is ideally suited for wireless mobile communications, such as GSM (Global System for Mobile Communications) and PCS.

FEATURES

- High frequency operation: 2.0 GHz max
- Low power supply voltage: $V_{CC} = 2.4$ to 3.6 V
- Ultra Low power supply current: $I_{CC} = 3.0$ mA typ. ($V_{CC} = V_p = 2.7$ V, $T_a = +25^\circ\text{C}$, in locking state)
 $I_{CC} = 3.5$ mA typ. ($V_{CC} = V_p = 3.0$ V, $T_a = +25^\circ\text{C}$, in locking state)
- Direct power saving function: Power supply current in power saving mode
 Typ. 0.1 μA ($V_{CC} = V_p = 3.0$ V, $T_a = +25^\circ\text{C}$), Max. 10 μA ($V_{CC} = V_p = 3.0$ V)
- Dual modulus prescaler: 64/65 or 128/129
- Serial input 14-bit programmable reference divider: $R = 3$ to 16,383
- Serial input programmable divider consisting of:
 - Binary 7-bit swallow counter: 0 to 127
 - Binary 11-bit programmable counter: 3 to 2,047
- Software selectable charge pump current
- On-chip phase control for phase comparator
- Operating temperature: $T_a = -40$ to $+85^\circ\text{C}$
- Pin compatible with MB15E05, MB15E05L

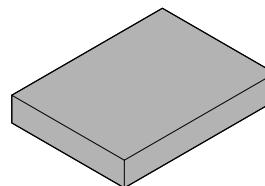
PACKAGES

16-pin plastic SSOP



(FPT-16P-M05)

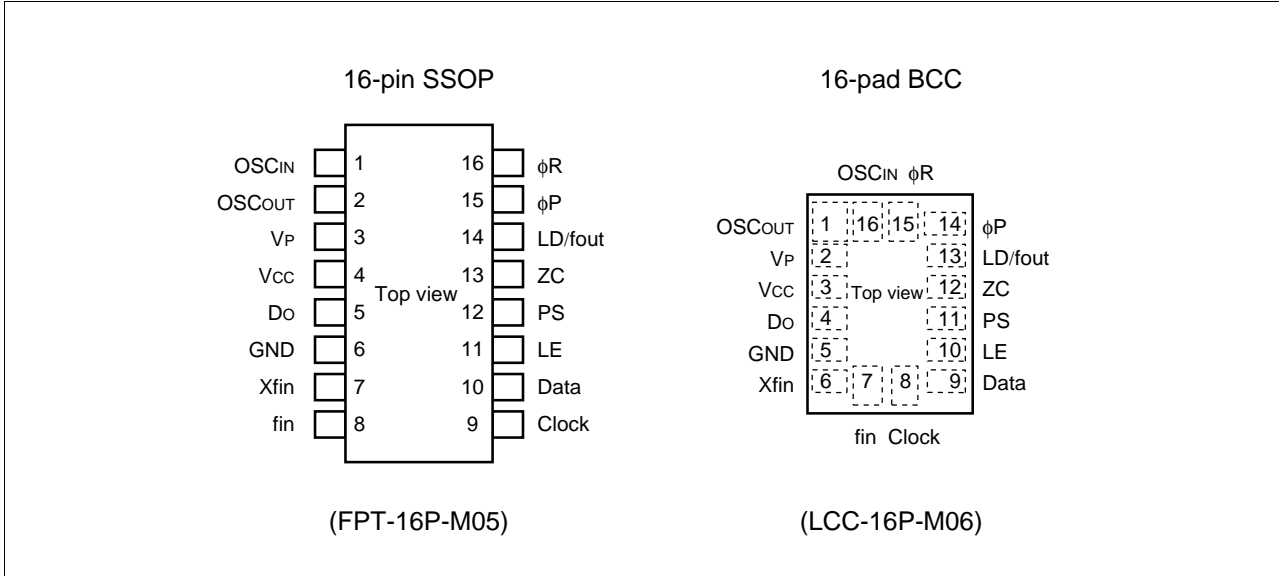
16-pad plastic BCC



(LCC-16P-M06)

MB15E05SL

■ PIN ASSIGNMENTS



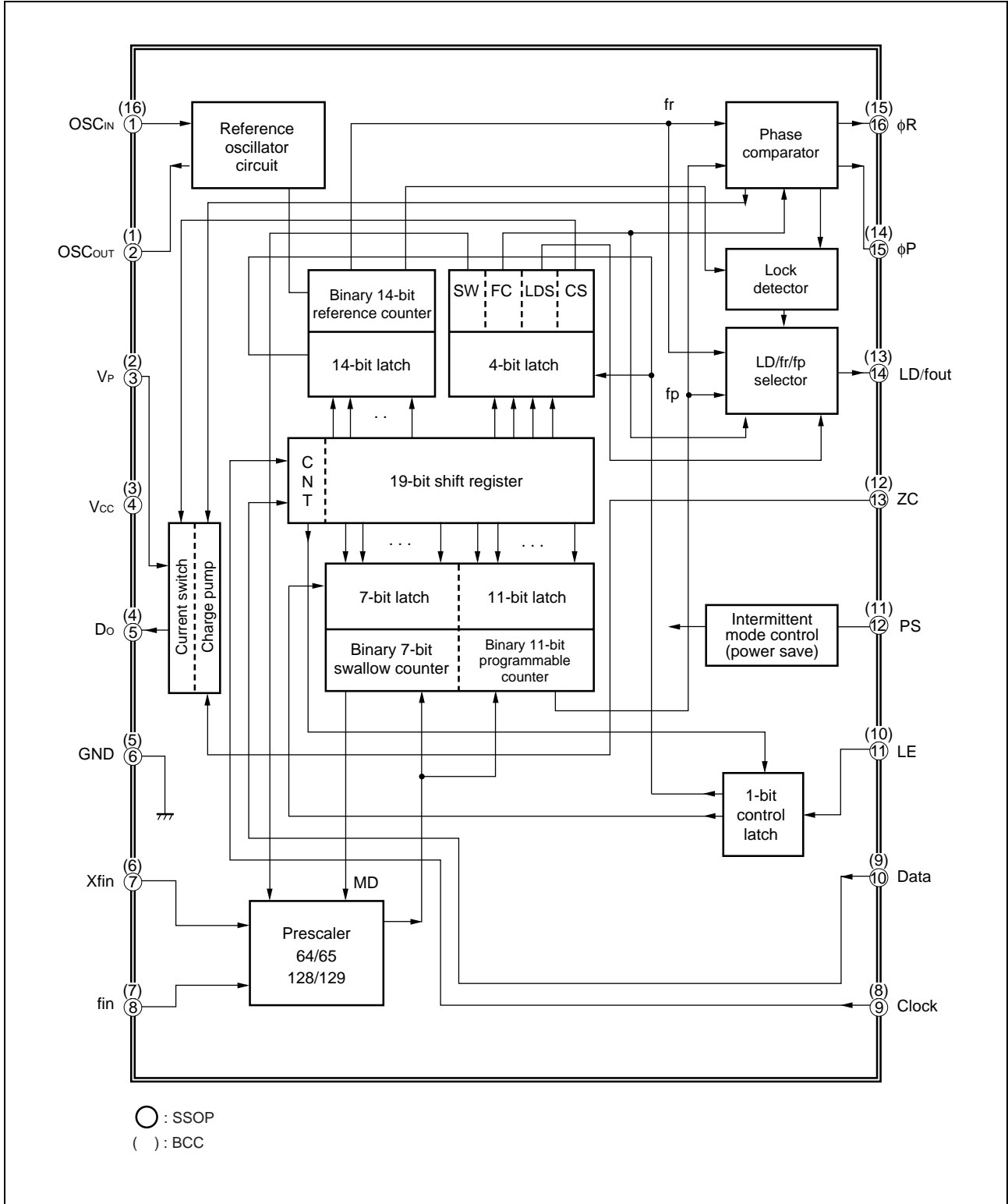
MB15E05SL

■ PIN DESCRIPTIONS

Pin no.		Pin name	I/O	Descriptions
SSOP	BCC			
1	16	OSC _{IN}	I	Programmable reference divider input. Connection to a TCXO.
2	1	OSC _{OUT}	O	Oscillator output.
3	2	V _P	–	Power supply voltage input for the charge pump.
4	3	V _{CC}	–	Power supply voltage input.
5	4	D _O	O	Charge pump output. Phase of the charge pump can be selected via programming of the FC bit.
6	5	GND	–	Ground.
7	6	Xfin	I	Prescaler complementary input, which should be grounded via a capacitor.
8	7	fin	I	Prescaler input. Connection to an external VCO should be done via AC coupling.
9	8	Clock	I	Clock input for the 19-bit shift register. Data is shifted into the shift register on the rising edge of the clock. (Open is prohibited.)
10	9	Data	I	Serial data input using binary code. The last bit of the data is a control bit. (Open is prohibited.)
11	10	LE	I	Load enable signal input. (Open is prohibited.) When LE is set high, the data in the shift register is transferred to a latch according to the control bit in the serial data.
12	11	PS	I	Power saving mode control. This pin must be set at “L” at Power-ON. (Open is prohibited.) PS = “H”; Normal mode PS = “L”; Power saving mode
13	12	ZC	I	Forced high-impedance control for the charge pump (with internal pull up resistor.) ZC = “H”; Normal D _O output. ZC = “L”; D _O becomes high impedance.
14	13	LD/fout	O	Lock detect signal output (LD)/phase comparator monitoring output (fout). The output signal is selected via programming of the LDS bit. LDS = “H”; outputs fout (fr/fp monitoring output) LDS = “L”; outputs LD (“H” at locking, “L” at unlocking.)
15	14	φP	O	Phase comparator N-channel open drain output for an external charge pump. Phase can be selected via programming of the FC bit.
16	15	φR	O	Phase comparator CMOS output for an external charge pump. Phase can be selected via programming of the FC bit.

MB15E05SL

■ BLOCK DIAGRAM



MB15E05SL

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit	Remark
			Min.	Max.		
Power supply voltage	V _{CC}	–	–0.5	4.0	V	
	V _P	–	V _{CC}	6.0	V	
Input voltage	V _I	–	–0.5	V _{CC} +0.5	V	
Output voltage	V _O	Except Do	GND	V _{CC}	V	
	V _O	Do	GND	V _P	V	
Storage temperature	T _{stg}	–	–55	+125	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
Power supply voltage	V _{CC}	2.4	3.0	3.6	V	
	V _P	V _{CC}	–	5.5	V	
Input voltage	V _I	GND	–	V _{CC}	V	
Operating temperature	T _a	–40	–	+85	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

MB15E05SL

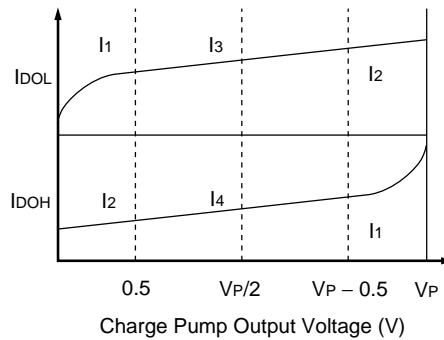
■ ELECTRICAL CHARACTERISTICS

($V_{CC} = 2.4$ to 3.6 V, $T_a = -40$ to $+85^\circ\text{C}$)

Parameter	Symbol	Condition	Value			Unit		
			Min.	Typ.	Max.			
Power supply current*1	I_{CC}	$f_{in} = 2000$ MHz, $V_{CC} = V_P = 2.7$ V ($V_{CC} = V_P = 3.0$ V)	–	3.0 (3.5)	–	mA		
Power saving current	I_{PS}	ZC = “H” or open	–	0.1 ²	10	μA		
Operating frequency	f_{in}	f_{in}	–	100	2000	MHz		
	OSC _{IN}	fosc	–	3	40	MHz		
Input sensitivity	f_{in}^{*3}	Pfin	50 Ω system (Refer to the measurement circuit.)	–15	–	+2	dBm	
	OSC _{IN} ^{*3}	V _{osc}	–	0.5	–	V_{CC}	Vp-p	
“H” level input voltage	Data, Clock, LE, PS, ZC	V_{IH}	–	$V_{CC} \times 0.7$	–	V		
“L” level input voltage		V_{IL}	–	–	$V_{CC} \times 0.3$			
“H” level input current	Data, Clock, LE, PS	I_{IH}^{*4}	–	–1.0	–	+1.0	μA	
“L” level input current		I_{IL}^{*4}	–	–1.0	–	+1.0		
“H” level input current	OSC _{IN}	I_{IH}	–	0	–	+100	μA	
“L” level input current		I_{IL}^{*4}	–	–100	–	0		
“H” level input current	ZC	I_{IH}^{*4}	–	–1.0	–	+1.0	μA	
“L” level input current		I_{IL}^{*4}	Pull up input	–100	–	0		
“L” level output voltage	ϕP	V_{OL}	Open drain output	–	–	0.4	V	
“H” level output voltage	ϕR , LD/fout	V_{OH}	$V_{CC} = V_P = 3.0$ V, $I_{OH} = -1$ mA	$V_{CC} - 0.4$	–	–	V	
“L” level output voltage		V_{OL}	$V_{CC} = V_P = 3.0$ V, $I_{OL} = 1$ mA	–	–	0.4		
“H” level output voltage	Do	V_{DOH}	$V_{CC} = V_P = 3.0$ V, $I_{DOH} = -0.5$ mA	$V_P - 0.4$	–	–	V	
“L” level output voltage		V_{DOL}	$V_{CC} = V_P = 3.0$ V, $I_{DOL} = 0.5$ mA	–	–	0.4		
High impedance cutoff current	Do	I_{OFF}	$V_{CC} = V_P = 3.0$ V, $V_{OFF} = 0.5$ V to $V_P - 0.5$ V	–	–	2.5	nA	
“L” level output current	ϕP	I_{OL}	Open drain output	1.0	–	–	mA	
“H” level output current	ϕR , LD/fout	I_{OH}	–	–	–	–1.0	mA	
“L” level output current		I_{OL}	–	1.0	–	–		
“H” level output current	Do	I_{DOH}^{*4}	$V_{CC} = 3$ V, $V_P = 3$ V, $V_{DO} = V_P/2$, $T_a = +25^\circ\text{C}$	CS bit = “H”	–	–6.0	–	mA
“L” level output current				I_{DOL}	CS bit = “L”	–	–1.5	
		CS bit = “H”			–	6.0	–	
				CS bit = “L”	–	1.5	–	
Charge pump current rate	I_{DOL}/I_{DOH}	I_{DOMT}^{*5}	$V_{DO} = V_P/2$	–	3	–	%	
	vs V_{DO}	I_{DOVD}^{*6}	0.5 V $\leq V_{DO} \leq V_P - 0.5$ V	–	10	–	%	
	vs T_a	I_{DOTA}^{*7}	$-40^\circ\text{C} \leq T_a \leq +85^\circ\text{C}$	–	10	–	%	

MB15E05SL

- *1: Conditions; $f_{osc} = 12 \text{ MHz}$, $T_a = +25^\circ\text{C}$, in locking state.
- *2: $V_{CC} = V_P = 3.0 \text{ V}$, $f_{osc} = 12.8 \text{ MHz}$, $T_a = +25^\circ\text{C}$, in power saving mode
- *3: AC coupling. 1000 pF capacitor is connected under the condition of min. operating frequency.
- *4: The symbol “-” (minus) means direction of current flow.
- *5: $V_{CC} = V_P = 3.0 \text{ V}$, $T_a = +25^\circ\text{C}$ $(|I_3| - |I_4|) / [(|I_3| + |I_4|) / 2] \times 100(\%)$
- *6: $V_{CC} = V_P = 3.0 \text{ V}$, $T_a = +25^\circ\text{C}$ $[(|I_2| - |I_1|) / 2] / [(|I_1| + |I_2|) / 2] \times 100(\%)$ (Applied to each I_{DOL} , I_{DOH})
- *7: $V_{CC} = V_P = 3.0 \text{ V}$, $V_{DO} = V_P/2$ $(|I_{DO(+85^\circ\text{C})} - I_{DO(-40^\circ\text{C})}| / 2) / (|I_{DO(+85^\circ\text{C})} + I_{DO(-40^\circ\text{C})}| / 2) \times 100(\%)$ (Applied to each I_{DOL} , I_{DOH})



MB15E05SL

FUNCTIONAL DESCRIPTION

1. Pulse Swallow Function

The divide ratio can be calculated using the following equation:

$$f_{vco} = [(M \times N) + A] \times f_{osc} \div R \quad (A < N)$$

- f_{vco} : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- f_{osc} : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)
- M : Preset divide ratio of modulus prescaler (64 or 128)

2. Serial Data Input

Serial data is processed using the Data, Clock, and LE pins. Serial data controls the programmable reference divider and the programmable divider separately.

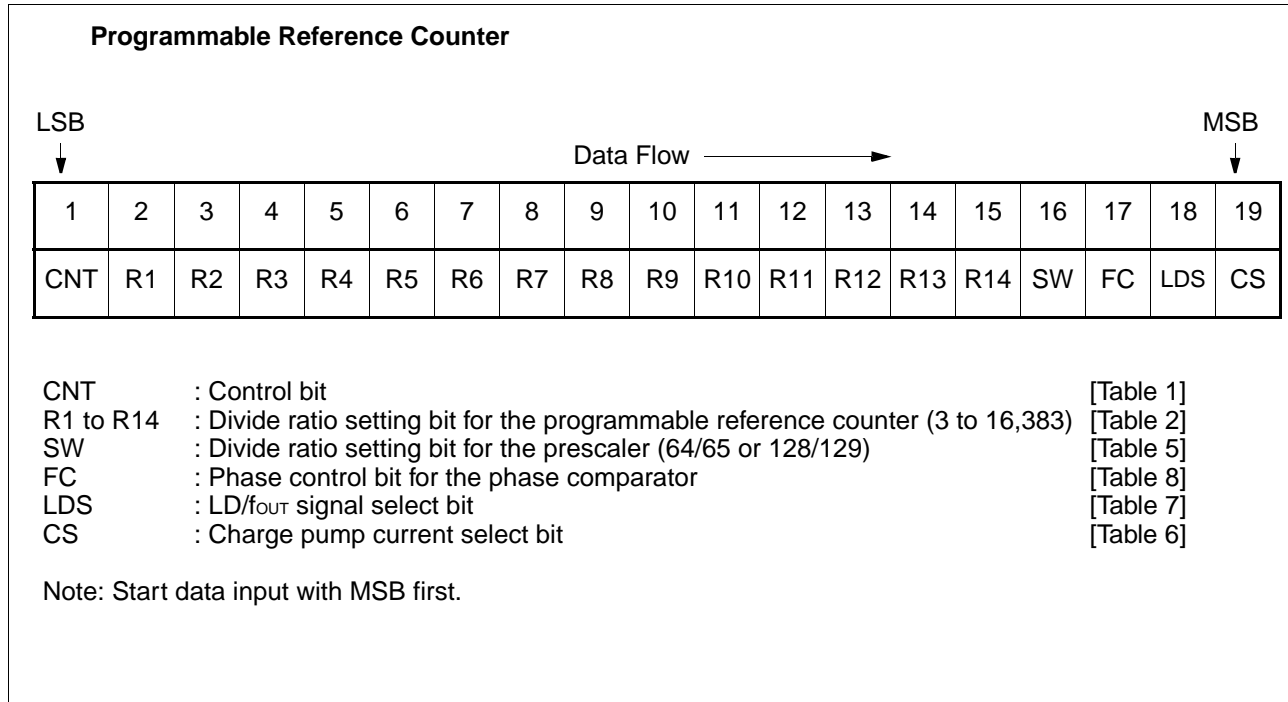
Binary serial data is entered through the Data pin.

One bit of data is shifted into the shift register on the rising edge of the Clock. When the LE signal pin is taken high, stored data is latched according to the control bit data as follows:

Table 1. Control Bit

Control bit (CNT)	Destination of serial data
H	For the programmable reference divider
L	For the programmable divider

(1) Shift Register Configuration



MB15E05SL

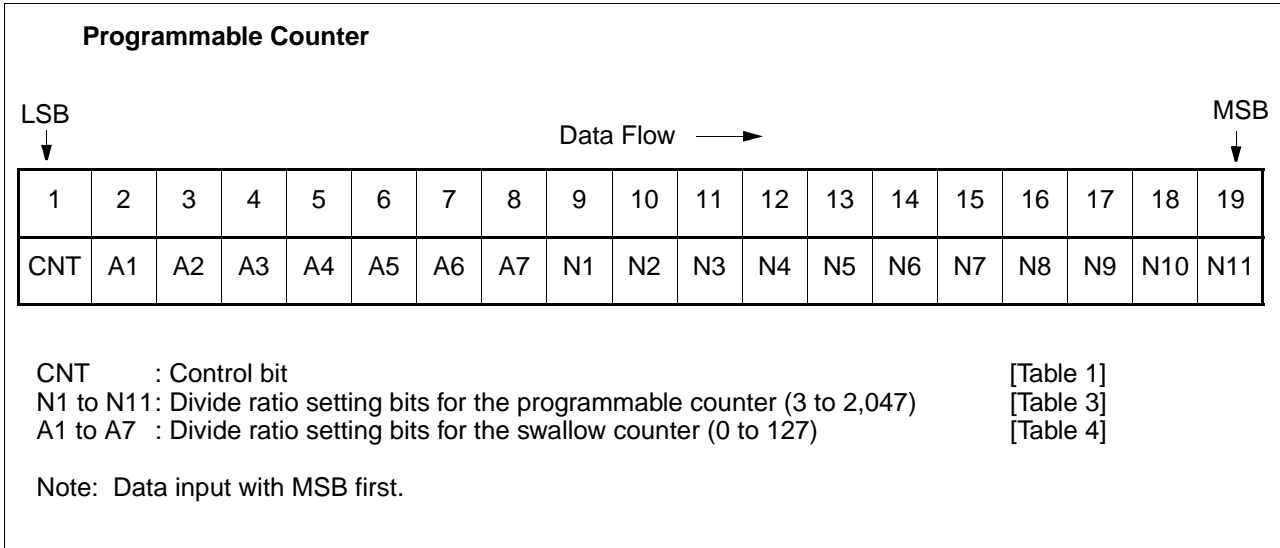


Table 2. Binary 14-bit Programmable Reference Counter Data Setting

Divide ratio(R)	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
.
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 3 is prohibited.

Table 3. Binary 11-bit Programmable Counter Data Setting

Divide ratio(N)	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
.
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 3 is prohibited.

MB15E05SL

Table 4. Binary 7-bit Swallow Counter Data Setting

Divide ratio(A)	A7	A6	A5	A4	A3	A2	A1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
·	·	·	·	·	·	·	·
127	1	1	1	1	1	1	1

Table 5. Prescaler Data Setting

SW	Prescaler divide ratio
H	64/65
L	128/129

Table 6. Charge Pump Current Setting

CS	Current value
H	±6.0 mA
L	±1.5 mA

Table 7. LD/fout Output Select Data Setting

LDS	LD/fout output signal
H	fout signal
L	LD signal

(2) Relation between the FC Input and Phase Characteristics

The FC bit changes the phase characteristics of the phase comparator. Both the internal charge pump output level (D_o) and the phase comparator output (φ_R, φ_P) are reversed according to the FC bit. Also, the monitor pin (fout) output is controlled by the FC bit. The relationship between the FC bit and each of D_o, φ_R, and φ_P is shown below.

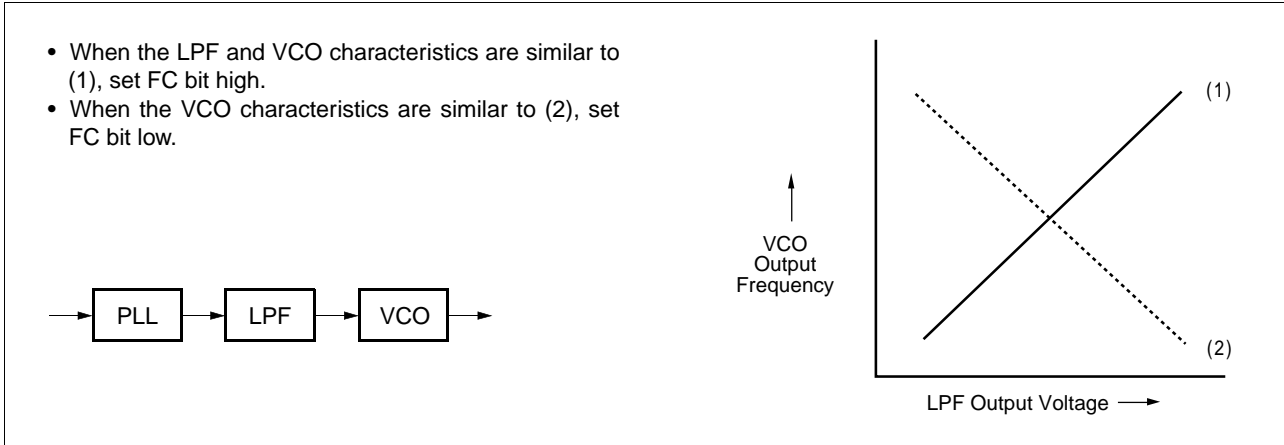
Table 8. FC Bit Data Setting (LDS = “H”)

	FC = High				FC = Low			
	D _o	φ _R	φ _P	LD/fout	D _o	φ _R	φ _P	LD/fout
fr > fp	H	L	L	fout = fr	L	H	Z*	fout = fp
fr < fp	L	H	Z*		H	L	L	
fr = fp	Z*	L	Z*		Z*	L	Z*	

* : High impedance

MB15E05SL

When designing a synthesizer, the FC pin setting depends on the VCO and LPF characteristics.



3. Do Output Control

Table 9. ZC Pin Setting

ZC pin	Do output
H	Normal output
L	High impedance

4. Power Saving Mode (Intermittent Mode Control Circuit)

Table 10. PS Pin Setting

PS pin	Status
H	Normal mode
L	Power saving mode

The intermittent mode control circuit reduces the PLL power consumption.

By setting the PS pin low, the device enters into the power saving mode, reducing the current consumption. See the Electrical Characteristics chart for the specific value.

The phase detector output, Do, becomes high impedance.

For the signal PLL, the lock detector, LD, remains high, indicating a locked condition.

Setting the PS pin high, releases the power saving mode, and the device works normally.

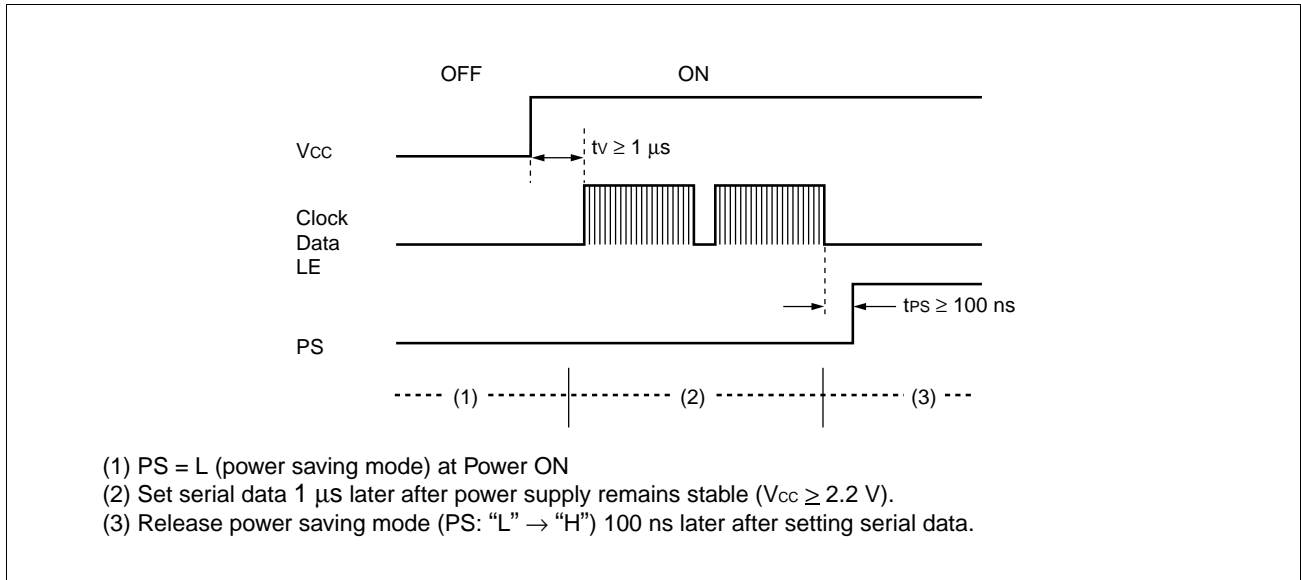
The intermittent mode control circuit also ensures a smooth startup when the device returns to normal operation. When the PLL is returned to normal operation, the phase comparator output signal is unpredictable. This is because of the unknown relationship between the comparison frequency (f_p) and the reference frequency (f_r) which can cause a major change in the comparator output, resulting in a VCO frequency jump and an increase in lockup time.

To prevent a major VCO frequency jump, the intermittent mode control circuit limits the magnitude of the error signal from the phase detector when it returns to normal operation.

Note: When power (V_{CC}) is first applied, the device must be in standby mode, PS = Low, for at least 1 μ s.

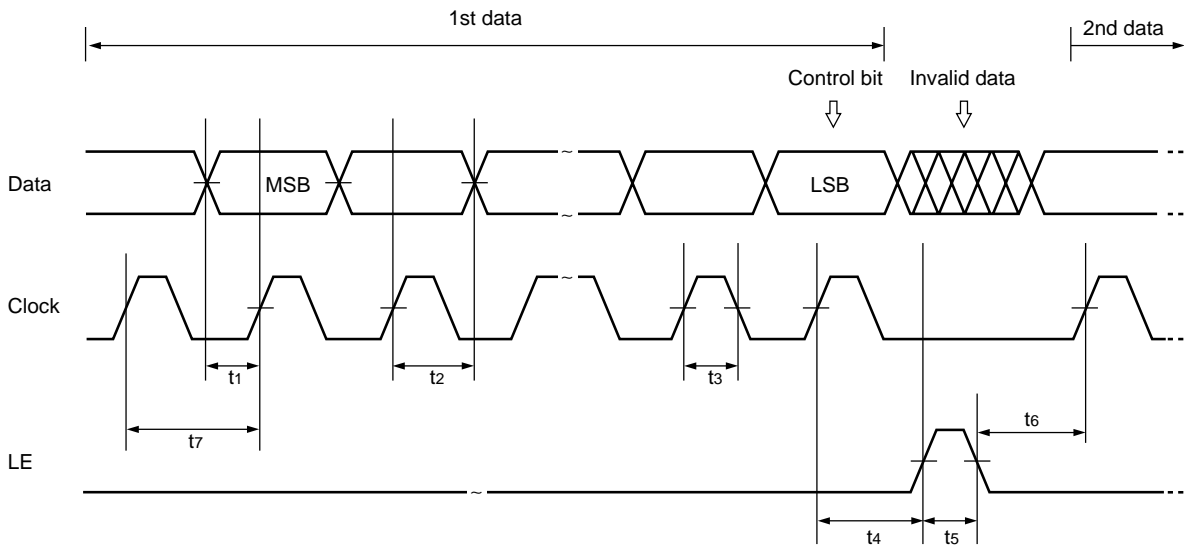
MB15E05SL

Note: • PS pin must be set "L" for Power-ON.



MB15E05SL

■ SERIAL DATA INPUT TIMING



On the rising edge of the clock, one bit of data is transferred into the shift register.

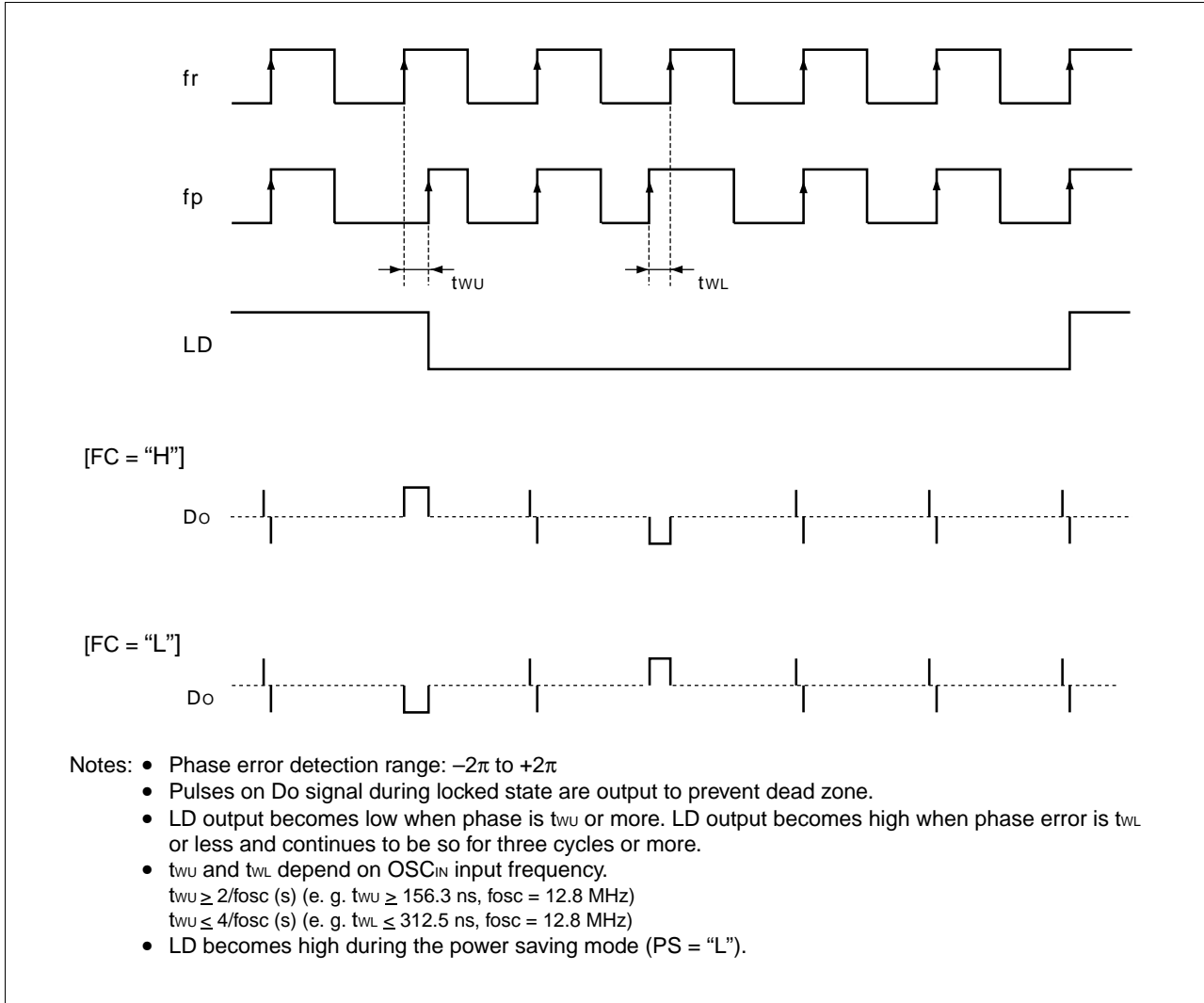
Parameter	Min.	Typ.	Max.	Unit
t_1	20	–	–	ns
t_2	20	–	–	ns
t_3	30	–	–	ns
t_4	30	–	–	ns

Parameter	Min.	Typ.	Max.	Unit
t_5	100	–	–	ns
t_6	20	–	–	ns
t_7	100	–	–	ns

Note: LE should be “L” when the data is transferred into the shift register.

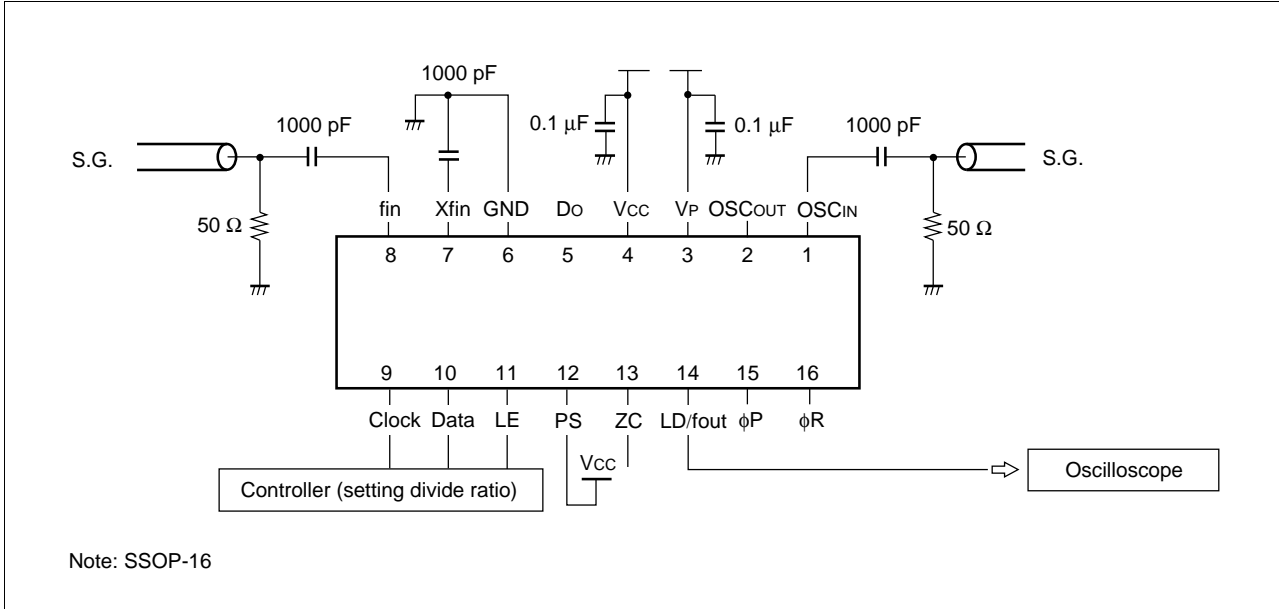
MB15E05SL

■ PHASE COMPARATOR OUTPUT WAVEFORM



MB15E05SL

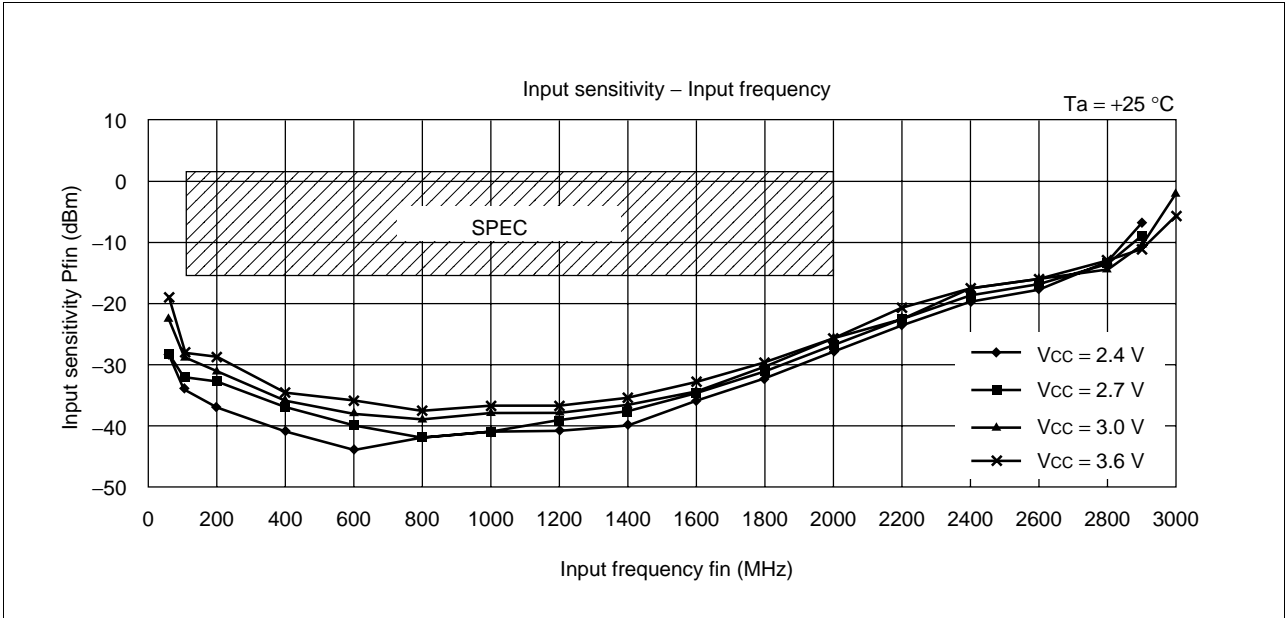
MEASUREMENT CIRCUIT (for Measuring Input Sensitivity fin/OSCIN)



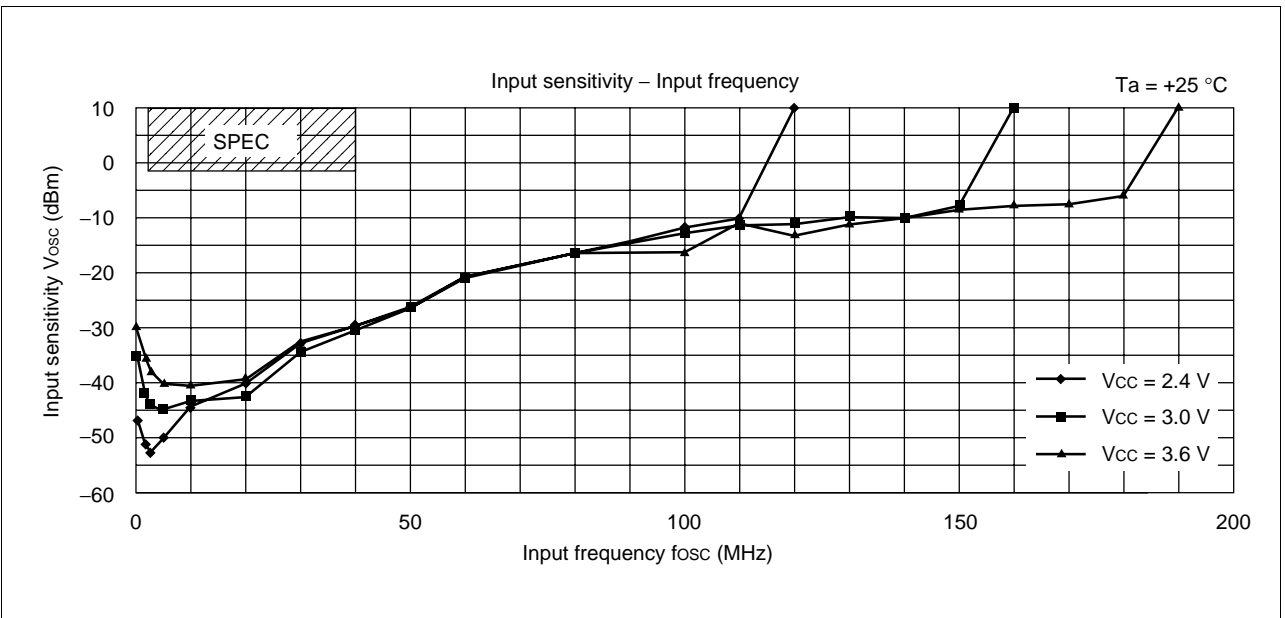
MB15E05SL

■ TYPICAL CHARACTERISTICS

1. fin input sensitivity



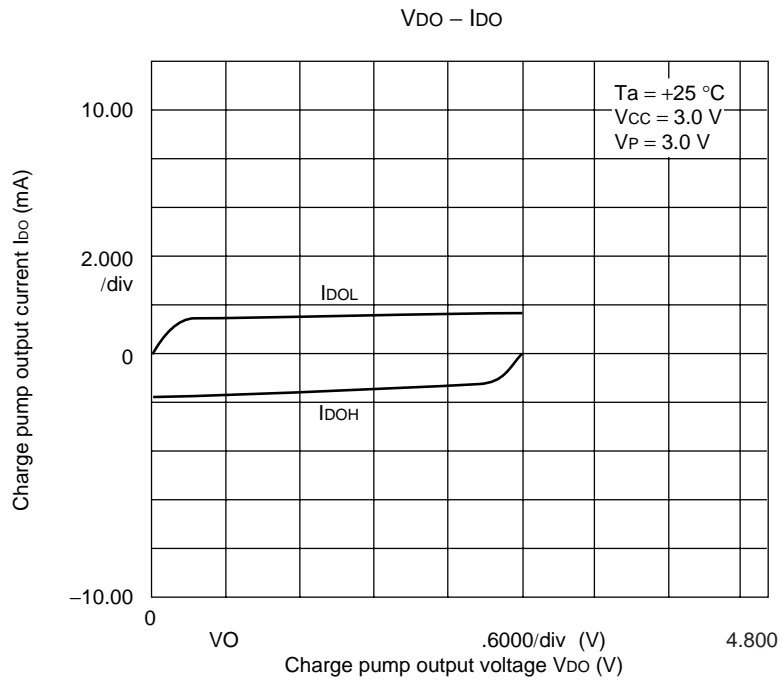
2. OSC_{IN} input sensitivity



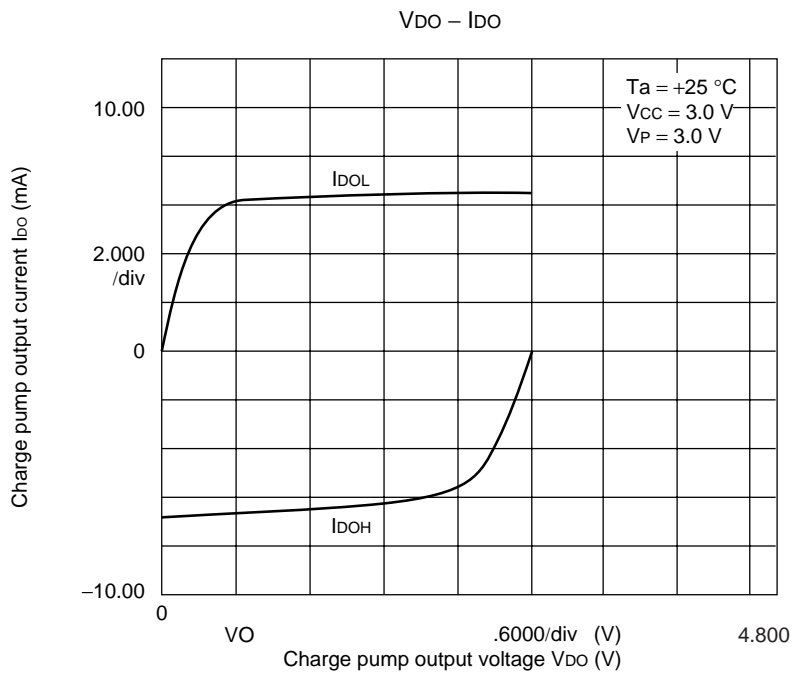
MB15E05SL

3. Do output current

1.5 mA mode

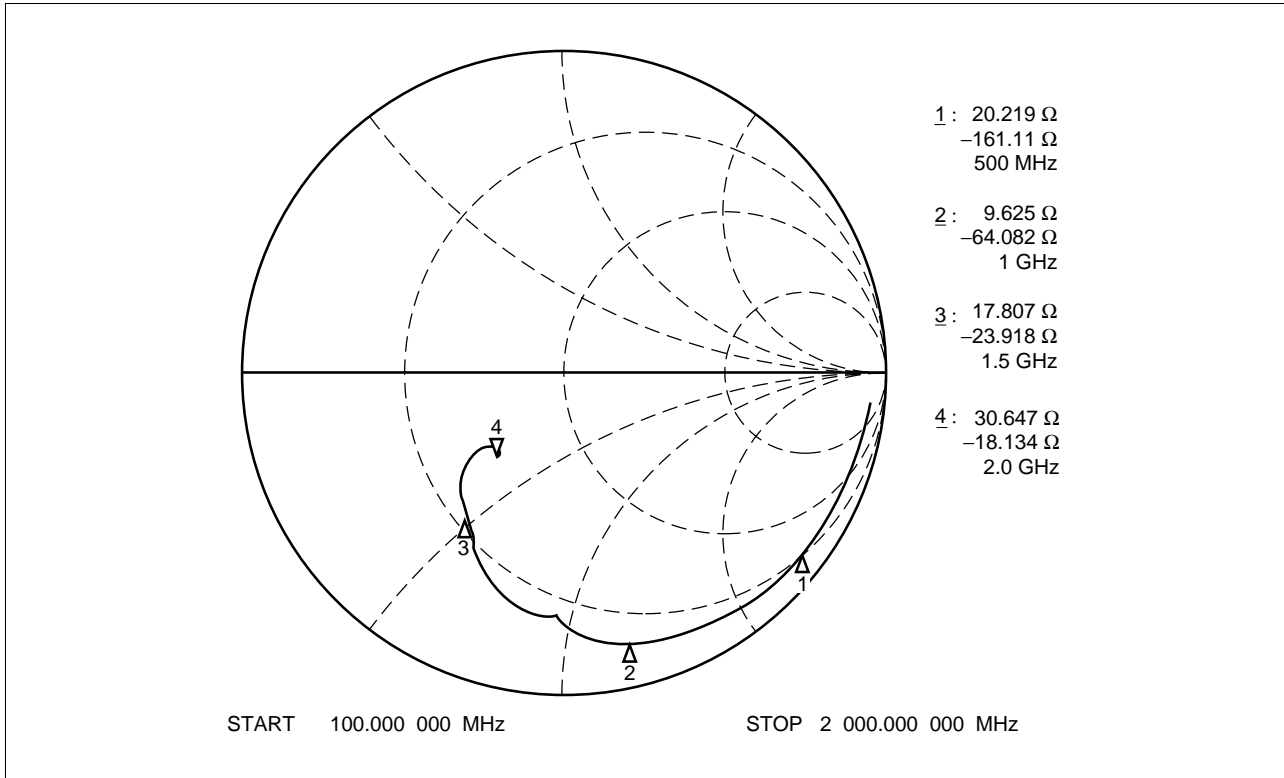


6.0 mA mode

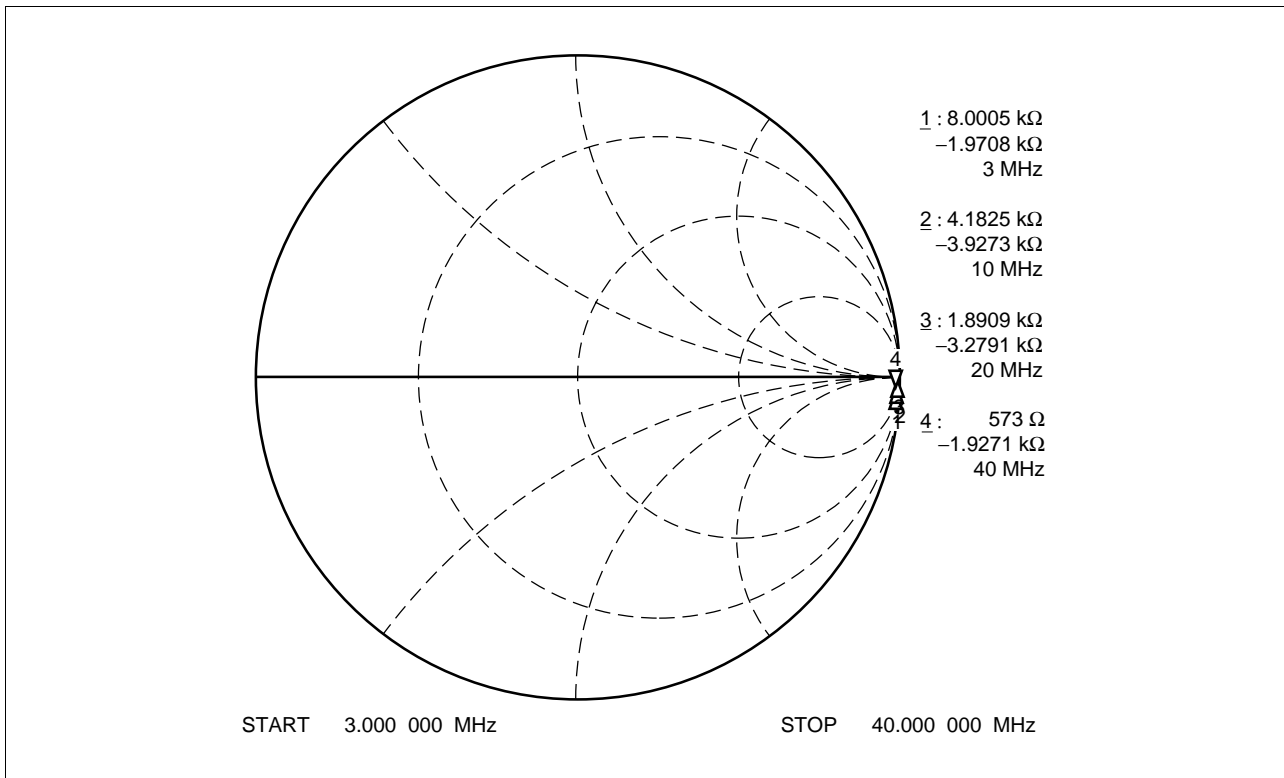


MB15E05SL

4. fin input impedance

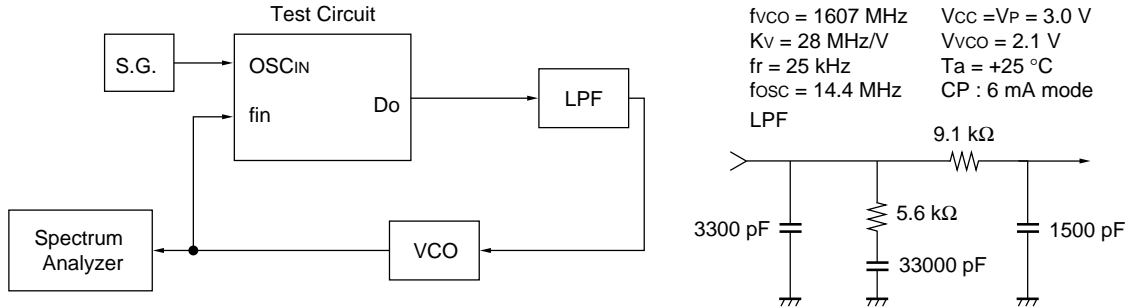


5. OSC_{IN} input impedance

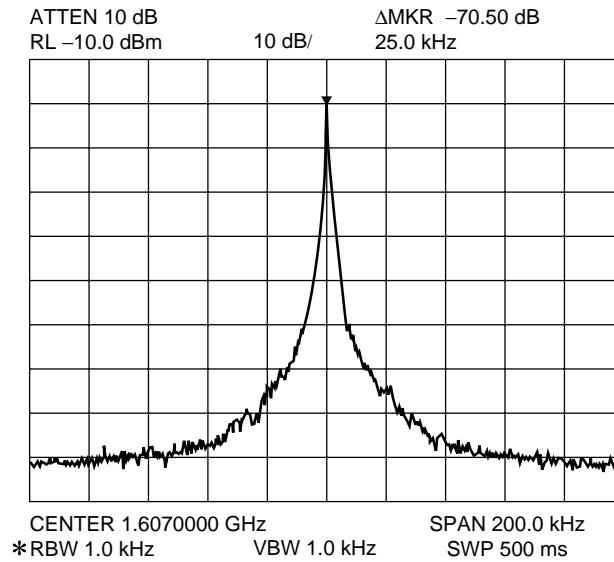


MB15E05SL

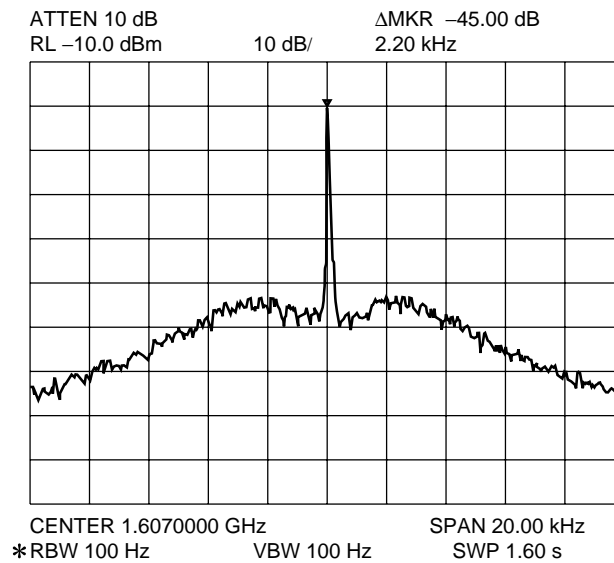
REFERENCE INFORMATION



PLL Reference Leakage



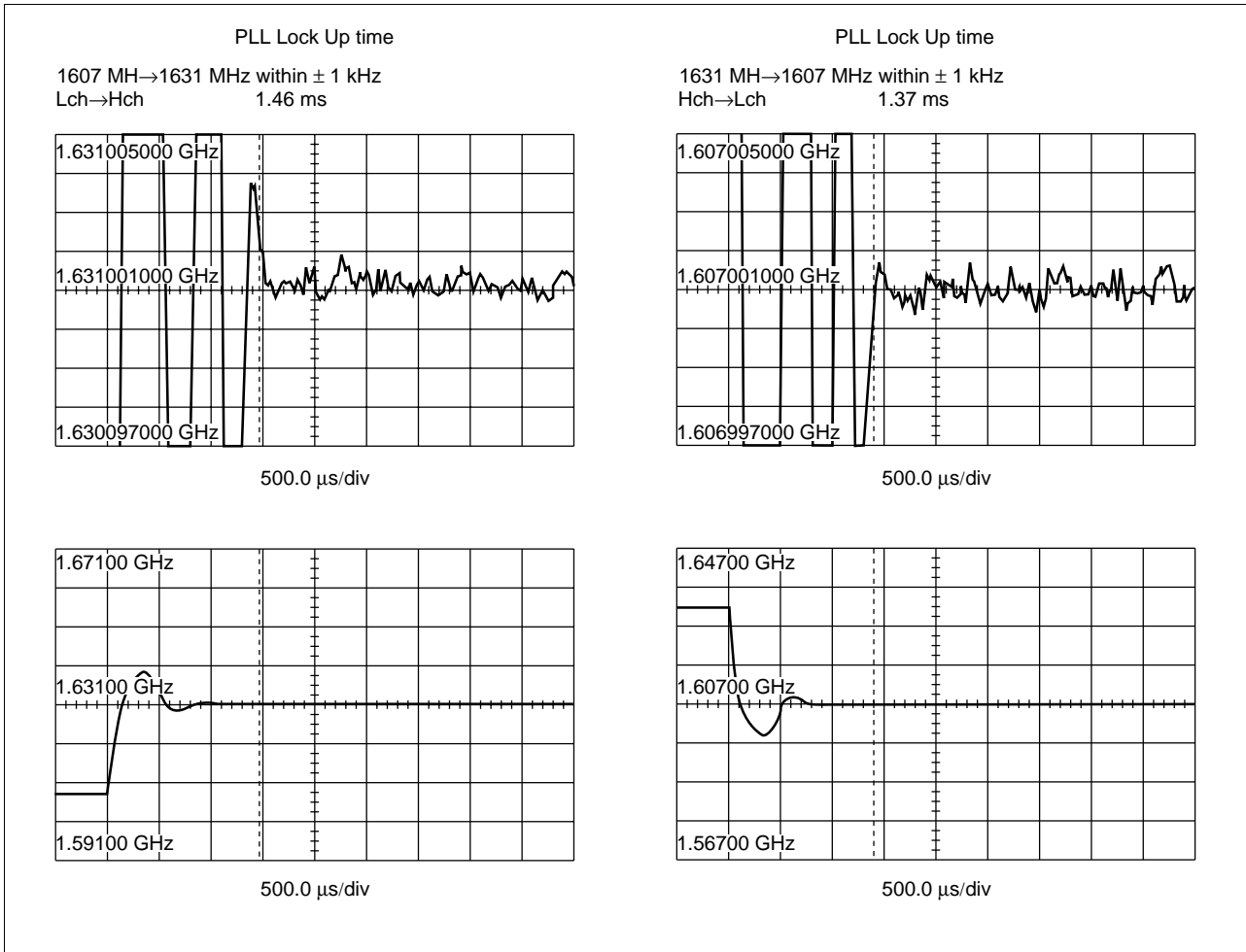
PLL Phase Noise



(Continued)

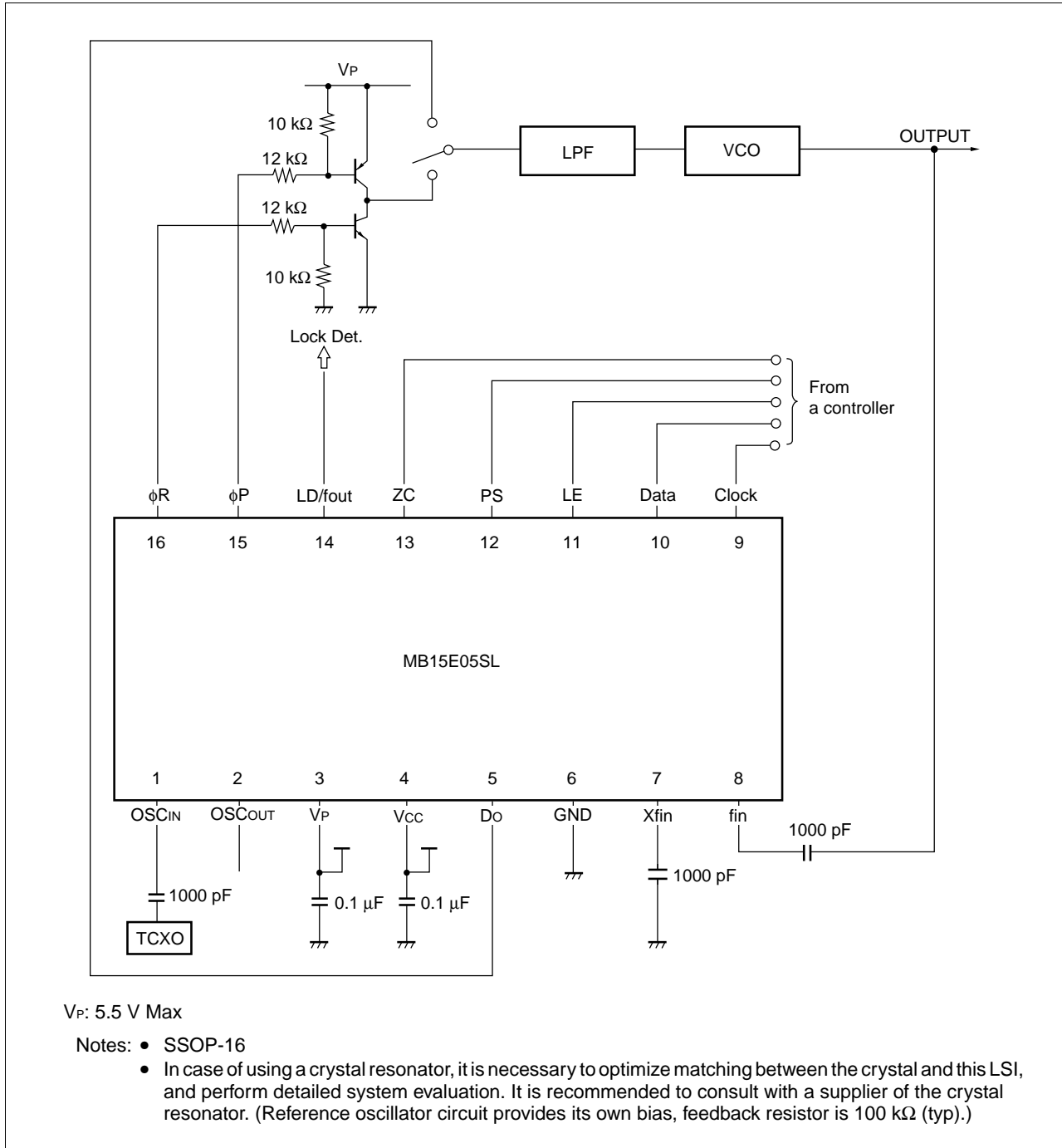
MB15E05SL

(Continued)



MB15E05SL

APPLICATION EXAMPLE



USAGE PRECAUTIONS

To protect against damage by electrostatic discharge, note the following handling precautions:

- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting device into or removing device from a socket.
- Protect leads with a conductive sheet when transporting a board-mounted device.

MB15E05SL

■ ORDERING INFORMATION

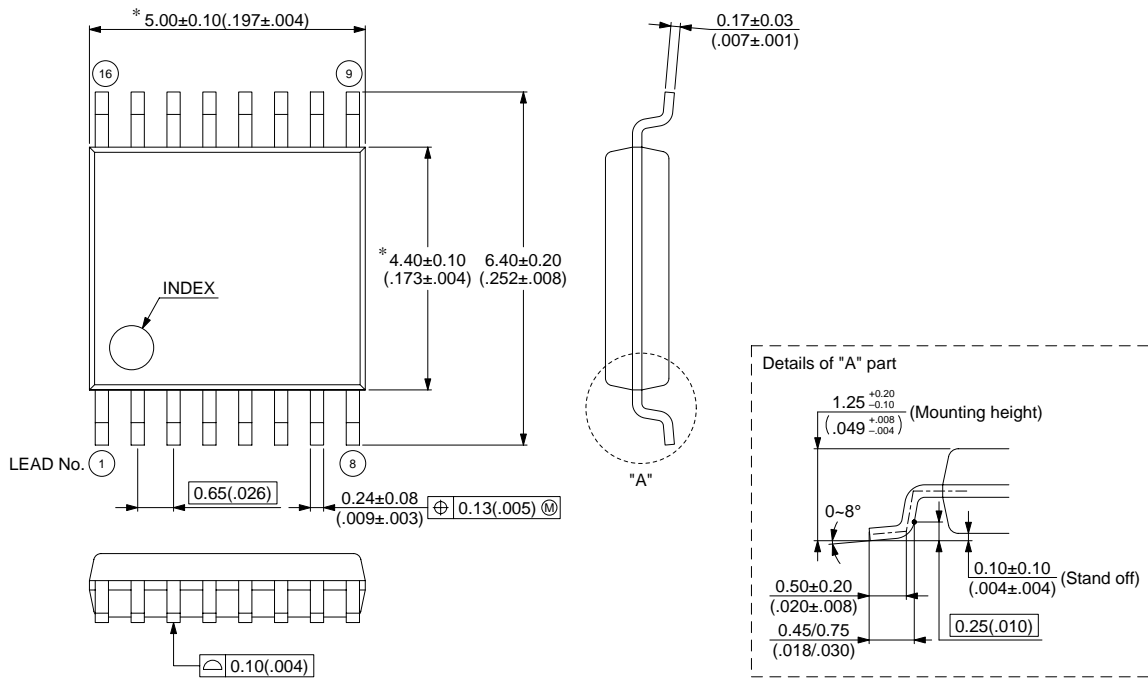
Part number	Package	Remarks
MB15E05SLPFV1	16-pin, Plastic SSOP (FPT-16P-M05)	
MB15E05SLPV1	16-pad, Plastic BCC (LCC-16P-M06)	

MB15E05SL

PACKAGE DIMENSIONS

16-pin, Plastic SSOP
 (FPT-16P-M05)

Note 1) * : These dimensions do not include resin protrusion.
 Note 2) Pins width and pins thickness include plating thickness.



© 1999 FUJITSU LIMITED F16013S-3C-5

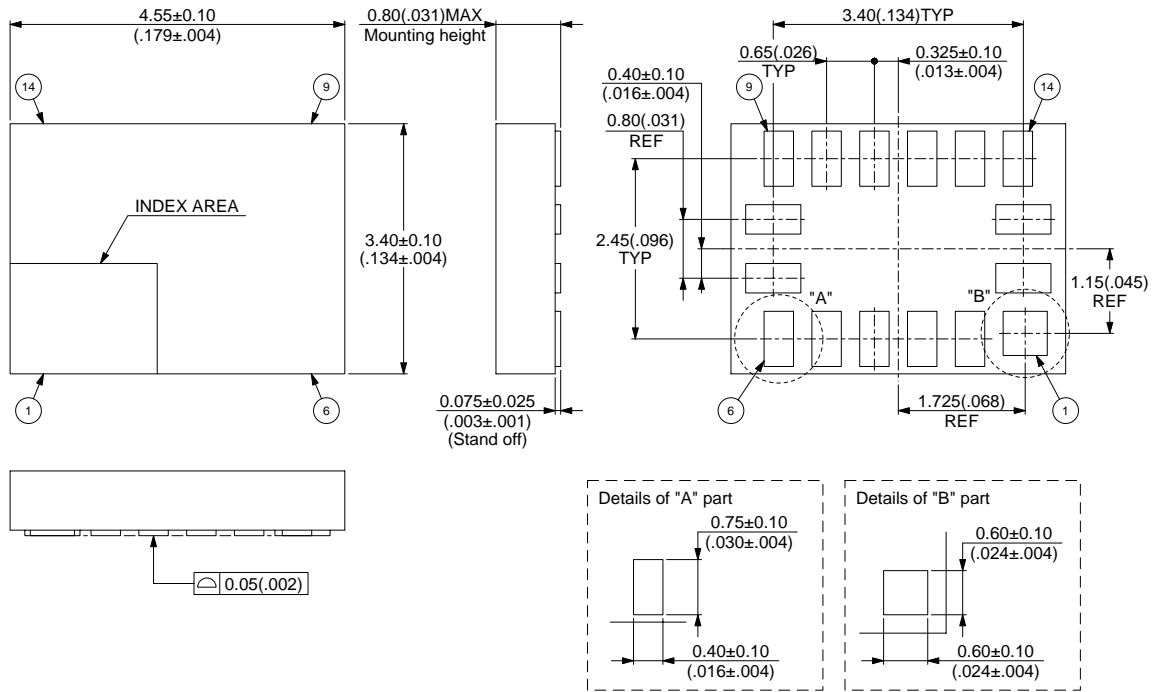
Dimensions in mm (inches)

(Continued)

MB15E05SL

(Continued)

16-pad plastic BCC
 (LCC-16P-M06)



© 1999 FUJITSU LIMITED C16017S-1C-1

Dimensions in mm (inches)

MB15E05SL

FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka,
Nakahara-ku, Kawasaki-shi,
Kanagawa 211-8588, Japan
Tel: +81-44-754-3763
Fax: +81-44-754-3329

<http://www.fujitsu.co.jp/>

North and South America

FUJITSU MICROELECTRONICS, INC.
3545 North First Street,
San Jose, CA 95134-1804, USA
Tel: +1-408-922-9000
Fax: +1-408-922-9179

Customer Response Center
Mon. - Fri.: 7 am - 5 pm (PST)
Tel: +1-800-866-8608
Fax: +1-408-922-9179

<http://www.fujitsumicro.com/>

Europe

FUJITSU MICROELECTRONICS EUROPE GmbH
Am Siebenstein 6-10,
D-63303 Dreieich-Buchsschlag,
Germany
Tel: +49-6103-690-0
Fax: +49-6103-690-122

<http://www.fujitsu-fme.com/>

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE LTD
#05-08, 151 Lorong Chuan,
New Tech Park,
Singapore 556741
Tel: +65-281-0770
Fax: +65-281-0220

<http://www.fmap.com.sg/>

F0002

© FUJITSU LIMITED Printed in Japan

All Rights Reserved.

The contents of this document are subject to change without notice.
Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document are presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

The contents of this document may not be reproduced or copied without the permission of FUJITSU LIMITED.

FUJITSU semiconductor devices are intended for use in standard applications (computers, office automation and other office equipments, industrial, communications, and measurement equipments, personal or household devices, etc.).

CAUTION:

Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Control Law of Japan, the prior authorization by Japanese government should be required for export of those products from Japan.