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Texas Instruments
SN74HC00DR

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# SNx4HC00 Quadruple 2-Input Positive-NAND Gates

## 1 Features

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up to 10 LSTTL Loads
- Low Power Consumption: $I_{CC}$ 20-µA (Maximum)
- Typical $t_{pd}$: 8 ns
- ±4-mA Output Drive at 5 V
- Low Input Current: 1 µA (Maximum)
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

## 2 Applications

- AV Receivers
- Portable Audio Docks
- Blu-ray Players and Home Theater
- MP3 Players or Recorders
- Personal Digital Assistants (PDAs)
- Power: Telecom or Server AC/DC Supply (Single Controller: Analog and Digital)
- Solid State Drives (SSDs): Client and Enterprise
- TVs: LCD, Digital, and High-Definition (HDTV)
- Tablets: Enterprise
- Video Analytics: Server
- Wireless Headsets, Keyboards, and Mice

## 3 Description

The SN54HC00 and SN74HC00 devices contain four independent, 2-input NAND gates. They perform the Boolean function $Y = \overline{A} \times \overline{B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

**Device Information(1)**

| PART NUMBER | PACKAGE (PINS) | BODY SIZE (NOM) |
|---|---|---|
| SN54HC00 | CDIP (14) | 6.92 mm × 19.94 mm |
| | CFP (14) | 6.20 mm × 9.41 mm |
| | LCCC (20) | 8.89 mm × 8.89 mm |
| SN74HC00D | SOIC (14) | 8.65 mm × 3.91 mm |
| SN74HC00DB | SSOP (14) | 6.20 mm × 5.30 mm |
| SN74HC00N | PDIP (14) | 19.30 mm × 6.35 mm |
| SN74HC00NS | SOP (14) | 10.30 mm × 5.30 mm |
| SN74HC00PW | TSSOP (14) | 5.00 mm × 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Logic Diagram (Positive Logic)**

## Table of Contents



## 4 Revision History

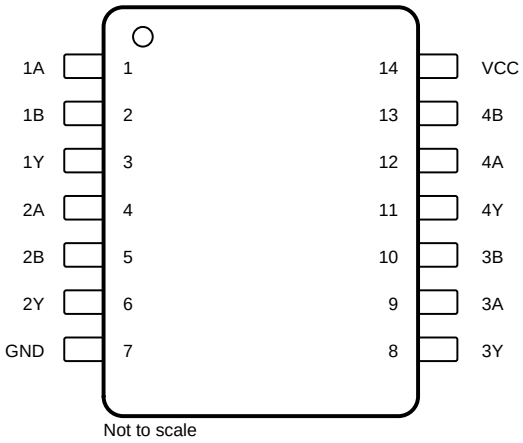
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision E (August 2003) to Revision F** **Page**

- Added *Applications* section, *Device Information* table, *ESD Ratings* table, *Typical Characteristics* section, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added Military Disclaimer to Features list ... 1
- Removed *Ordering Information* table; see POA at the end of data sheet ... 1
- Changed values in the *Thermal Information* table to align with JEDEC standards ... 5
- Deleted *Operating Characteristics* table; moved Cpd row to *Electrical Characteristics* ... 5

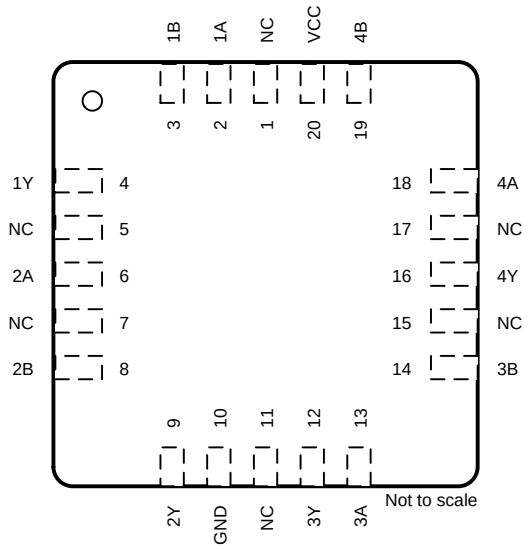
## 5 Pin Configuration and Functions

**D, DB, J, N, NS, PW, and W Package**
**14-Pin SOIC, SSOP, CDIP, PDIP, SOP, TSSOP, and CFP**
**Top View**




Not to scale

**FK Package**
**20-Pin LCCC**
**Top View**

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**Pin Functions**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | SOIC, SSOP, CDIP, PDIP, SOP, TSSOP, CFP | LCCC | | |
| 1A | 1 | 2 | I | Gate 1 input |
| 1B | 2 | 3 | I | Gate 1 input |
| 1Y | 3 | 4 | O | Gate 1 output |
| 2A | 4 | 6 | I | Gate 2 input |
| 2B | 5 | 8 | I | Gate 2 input |
| 2Y | 6 | 9 | O | Gate 2 output |
| 3A | 9 | 13 | I | Gate 3 input |
| 3B | 10 | 14 | I | Gate 3 input |
| 3Y | 8 | 12 | O | Gate 3 output |
| 4A | 12 | 18 | I | Gate 4 input |
| 4B | 13 | 19 | I | Gate 4 input |
| 4Y | 11 | 16 | O | Gate 4 output |
| GND | 7 | 10 | — | Ground pin |
| NC | — | 1, 5, 7, 11, 15,17 | — | No internal connection |
| $V_{CC}$ | 14 | 20 | — | Power pin |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply voltage, $V_{CC}$ | –0.5 | 7 | V |
| Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{CC}$)(2) | | ±20 | mA |
| Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$)(2) | | ±20 | mA |
| Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) | | ±25 | mA |
| Continuous current through $V_{CC}$ or GND | | ±50 | mA |
| Storage temperature, $T_{stg}$ | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5 | 6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | | | |
| | | $V_{CC}$ = 6 V | 4.2 | | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | | 0.5 | V |
| | | $V_{CC}$ = 4.5 V | | | 1.35 | |
| | | $V_{CC}$ = 6 V | | | 1.8 | |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | | $V_{CC}$ | V |
| $\Delta t/\Delta v$ | Input transition rise and fall time | $V_{CC}$ = 2 V | | | 1000 | ns |
| | | $V_{CC}$ = 4.5 V | | | 500 | |
| | | $V_{CC}$ = 6 V | | | 400 | |
| $T_A$ | Operating free-air temperature | SN54HC00 | –55 | | 125 | °C |
| | | SN74HC00 | –40 | | 85 | |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to *Implications of Slow or Floating CMOS Inputs* application report.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | SN74HC00 | | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | D (SOIC) | DB (SSOP) | N (PDIP) | NS (SOP) | PW (TSSOP) | |
| | | 14 PINS | 14 PINS | 14 PINS | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 94.7 | 108.3 | 57.5 | 91 | 122.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 54.6 | 60.3 | 45.1 | 48.8 | 51.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 49 | 55.7 | 37.3 | 49.8 | 64.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 21.1 | 25 | 30.3 | 18.4 | 6.6 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 48.7 | 55.2 | 37.2 | 49.5 | 64 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –20 µA | $V_{CC}$ = 2 V | 1.9 | 1.998 | | V |
| | | | $V_{CC}$ = 4.5 V | 4.4 | 4.499 | | |
| | | | $V_{CC}$ = 6 V | 5.9 | 5.999 | | |
| | | $I_{OH}$ = –4 mA, $V_{CC}$ = 4.5 V | $T_A$ = 25°C | 3.98 | 4.3 | | |
| | | | SN54HC00 | 3.7 | | | |
| | | | SN74HC00 | 3.84 | | | |
| | | $I_{OH}$ = –5.2 mA, $V_{CC}$ = 6 V | $T_A$ = 25°C | 5.48 | 5.8 | | |
| | | | SN54HC00 | 5.2 | | | |
| | | | SN74HC00 | 5.34 | | | |
| $V_{OL}$ | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 µA | $V_{CC}$ = 2 V | | 0.002 | 0.1 | V |
| | | | $V_{CC}$ = 4.5 V | | 0.001 | 0.1 | |
| | | | $V_{CC}$ = 6 V | | 0.001 | 0.1 | |
| | | $I_{OL}$ = 4 mA, $V_{CC}$ = 4.5 V | $T_A$ = 25°C | | 0.17 | 0.26 | |
| | | | SN54HC00 | | | 0.4 | |
| | | | SN74HC00 | | | 0.33 | |
| | | $I_{OL}$ = 5.2 mA, $V_{CC}$ = 6 V | $T_A$ = 25°C | | 0.15 | 0.26 | |
| | | | SN54HC00 | | | 0.4 | |
| | | | SN74HC00 | | | 0.33 | |
| $I_I$ | $V_I = V_{CC}$ or 0, $V_{CC}$ = 6 V | $T_A$ = 25°C | | | ±0.1 | ±100 | nA |
| | | SNx4HC00 | | | | ±1000 | |
| $I_{CC}$ | $V_I = V_{CC}$ or 0, $I_O$ = 0, $V_{CC}$ = 6 V | $T_A$ = 25°C | | | | 2 | µA |
| | | SN54HC00 | | | | 40 | |
| | | SN74HC00 | | | | 20 | |
| $C_i$ | $V_{CC}$ = 2 V to 6 V | | | | 3 | 10 | pF |
| $C_{pd}$ Power dissipation capacitance per gate | No load, $T_A$ = 25°C | | | | 20 | | pF |

## 6.6 Switching Characteristics

over recommended operating free-air temperature range, $C_L$ = 50 pF, see Figure 2 (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{pd}$ | From A or B (input) to Y (output) | $V_{CC}$ = 2 V | $T_A$ = 25°C | | 45 | 90 | ns |
| | | | SN54HC00 | | | 135 | |
| | | | SN74HC00 | | | 115 | |
| | | $V_{CC}$ = 4.5 V | $T_A$ = 25°C | | 9 | 18 | |
| | | | SN54HC00 | | | 27 | |
| | | | SN74HC00 | | | 23 | |
| | | $V_{CC}$ = 6 V | $T_A$ = 25°C | | 8 | 15 | |
| | | | SN54HC00 | | | 23 | |
| | | | SN74HC00 | | | 20 | |
| $t_t$ | To Y (output) | $V_{CC}$ = 2 V | $T_A$ = 25°C | | 38 | 75 | ns |
| | | | SN54HC00 | | | 110 | |
| | | | SN74HC00 | | | 95 | |
| | | $V_{CC}$ = 4.5 V | $T_A$ = 25°C | | 8 | 15 | |
| | | | SN54HC00 | | | 22 | |
| | | | SN74HC00 | | | 19 | |
| | | $V_{CC}$ = 6 V | $T_A$ = 25°C | | 6 | 13 | |
| | | | SN54HC00 | | | 19 | |
| | | | SN74HC00 | | | 16 | |

## 6.7 Typical Characteristics

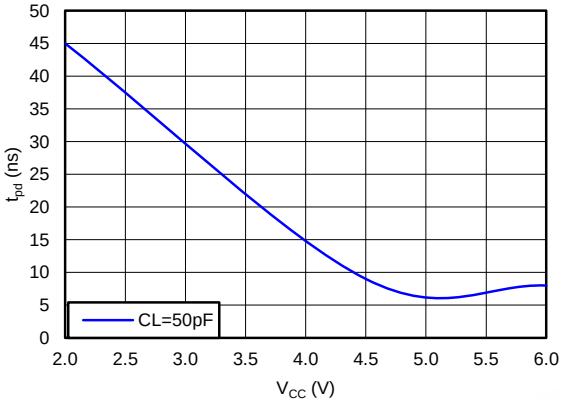
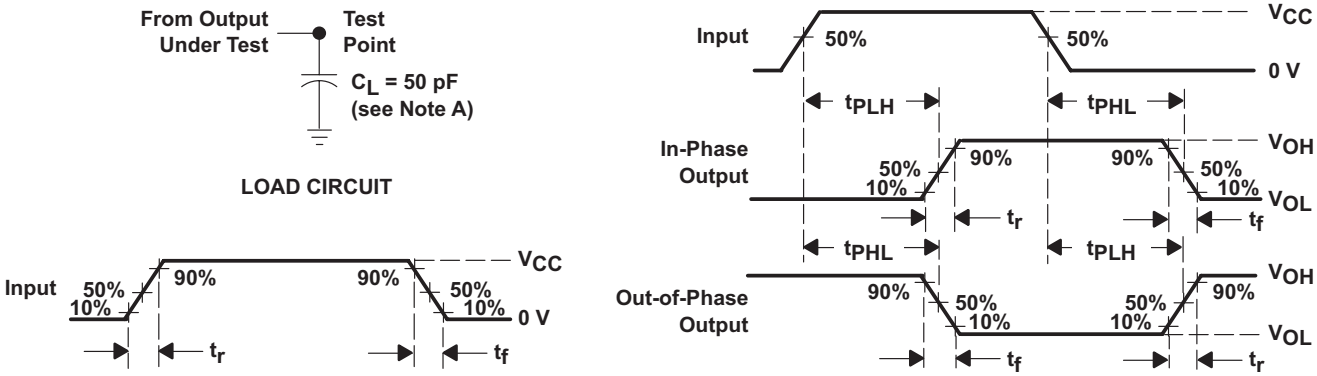



**Figure 1. Propagation Delay vs $V_{CC}$**

## 7 Parameter Measurement Information




NOTES: A. CL includes probe and test-fixture capacitance.

B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 6 ns, $t_f$ = 6 ns.

C. The outputs are measured one at a time with one input transition per measurement.

D. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

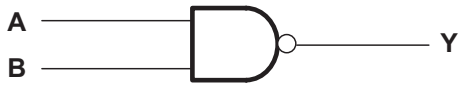
**Figure 2. Load Circuit and Voltage Waveforms**

# 8 Detailed Description

## 8.1 Overview

The SNx4HC00 devices perform the NAND Boolean function $Y = \overline{A} \times \overline{B}$ or $Y = \overline{A} + \overline{B}$ in positive logic. The devices have a wide operating range of $V_{CC}$ from 2 V to 6 V.

## 8.2 Functional Block Diagram






## 8.3 Feature Description

The SNx4HC00 devices have a wide operating voltage range that operates from 2 V to 6 V. They allow inputs and outputs up to $V_{CC}$. The devices can drive outputs at 4 mA at 5-V $V_{CC}$.

## 8.4 Device Functional Modes

Table 1 lists the functional modes for the SNx4HC00.

**Table 1. Function Table**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| H | H | L |
| L | X | H |
| X | L | H |

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The SNx4HC00 is a low-power, wide-operating-voltage NAND gate. This device can drive up to 10 LSTTL loads and can drive 4-mA outputs at 5-V $V_{CC}$.

## 9.2 Typical Application

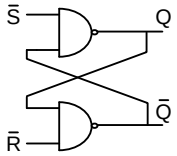





**Figure 3. Typical NAND Gate Application and Supply Voltage**

### 9.2.1 Design Requirements

The SNx4HC00 devices use CMOS technology and have balanced output drive. Take care to avoid bus contention because it drives currents that would exceed maximum limits. The high drive also creates fast edges into light loads. Routing and load conditions must be considered to prevent ringing.

### 9.2.2 Detailed Design Procedure

- Recommended input conditions:
  - Specified high and low levels. See $V_{IH}$ and $V_{IL}$ in *Recommended Operating Conditions*.
- Recommended output conditions:
  - Load currents must not exceed 25 mA per output and 50 mA total for the part.
  - Outputs must not be pulled above $V_{CC}$.

### 9.2.3 Application Curve

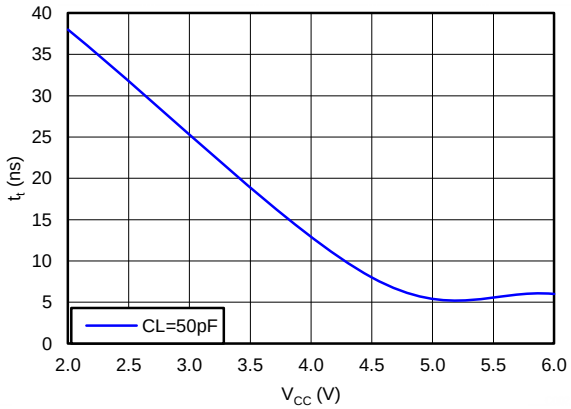



**Figure 4. Transition Time vs $V_{CC}$**

## 10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in *Recommended Operating Conditions*.

Each $V_{CC}$ pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF bypass capacitor; if there are multiple $V_{CC}$ pins, then TI recommends 0.01-µF or 0.022-µF bypass capacitors for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 µF and a 1 µF are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices inputs must never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input and gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 5 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or $V_{CC}$, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver.

### 11.2 Layout Example

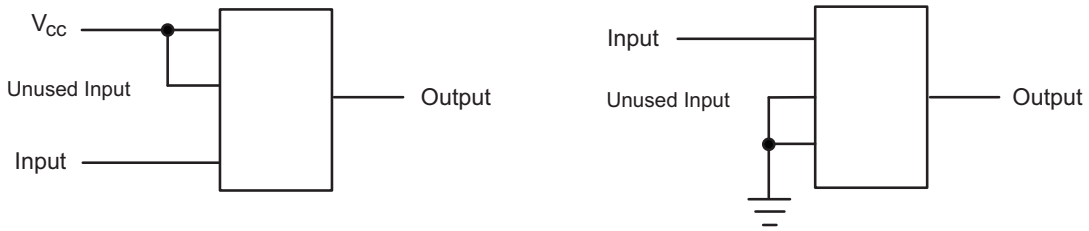



**Figure 5. Layout Diagram**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

*Implications of Slow or Floating CMOS Inputs* (SCBA004)

## 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN54HC00 | Click here | Click here | Click here | Click here | Click here |
| SN74HC00 | Click here | Click here | Click here | Click here | Click here |

## 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-8403701VCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8403701VC A SNV54HC00J | Samples |
| 5962-8403701VDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8403701VD A SNV54HC00W | Samples |
| 84037012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 84037012A SNJ54HC 00FK | Samples |
| 8403701CA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8403701CA SNJ54HC00J | Samples |
| 8403701DA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8403701DA SNJ54HC00W | Samples |
| JM38510/65001B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 65001B2A | Samples |
| JM38510/65001BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 65001BCA | Samples |
| JM38510/65001BDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 65001BDA | Samples |
| M38510/65001B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 65001B2A | Samples |
| M38510/65001BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 65001BCA | Samples |
| M38510/65001BDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 65001BDA | Samples |
| SN54HC00J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54HC00J | Samples |
| SN74HC00D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC00 | Samples |
| SN74HC00DBR | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC00 | Samples |
| SN74HC00DE4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC00 | Samples |
| SN74HC00DG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC00 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74HC00DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU SN | Level-1-260C-UNLIM | -40 to 85 | HC00 | Samples |
| SN74HC00DRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC00 | Samples |
| SN74HC00DRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC00 | Samples |
| SN74HC00DT | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC00 | Samples |
| SN74HC00DTE4 | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC00 | Samples |
| SN74HC00DTG4 | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC00 | Samples |
| SN74HC00N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU \| CU SN | N / A for Pkg Type | -40 to 85 | SN74HC00N | Samples |
| SN74HC00N3 | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74HC00NE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HC00N | Samples |
| SN74HC00NSLE | OBSOLETE | SO | NS | 14 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74HC00NSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC00 | Samples |
| SN74HC00PW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC00 | Samples |
| SN74HC00PWG4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC00 | Samples |
| SN74HC00PWLE | OBSOLETE | TSSOP | PW | 14 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74HC00PWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU SN | Level-1-260C-UNLIM | -40 to 85 | HC00 | Samples |
| SN74HC00PWRE4 | ACTIVE | TSSOP | PW | 14 | | TBD | Call TI | Call TI | -40 to 85 | | Samples |
| SN74HC00PWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC00 | Samples |
| SN74HC00PWT | ACTIVE | TSSOP | PW | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC00 | Samples |
| SNJ54HC00FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 84037012A SNJ54HC 00FK | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SNJ54HC00J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8403701CA SNJ54HC00J | Samples |
| SNJ54HC00W | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8403701DA SNJ54HC00W | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54HC00, SN54HC00-SP, SN74HC00 :**

- Catalog: SN74HC00, SN54HC00
- Automotive: SN74HC00-Q1, SN74HC00-Q1
- Military: SN54HC00
- Space: SN54HC00-SP

NOTE: Qualified Version Definitions:

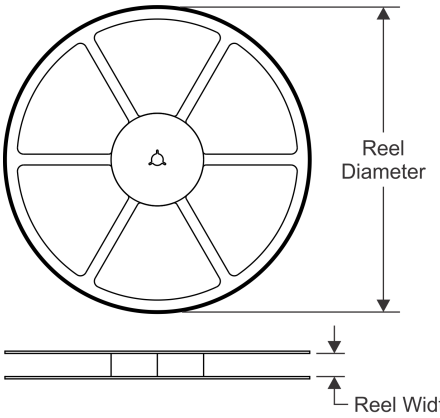
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

# PACKAGE MATERIALS INFORMATION

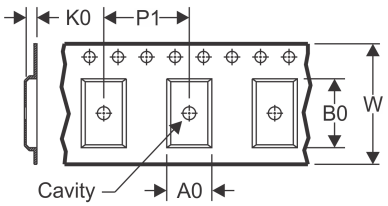


## TAPE AND REEL INFORMATION

REEL DIMENSIONS

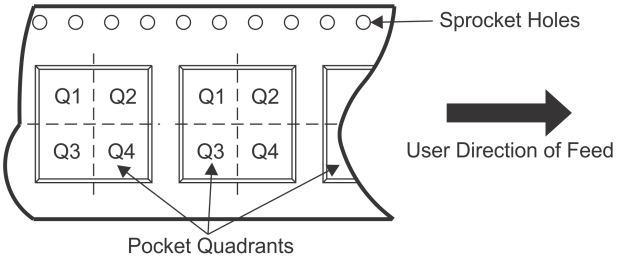



TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



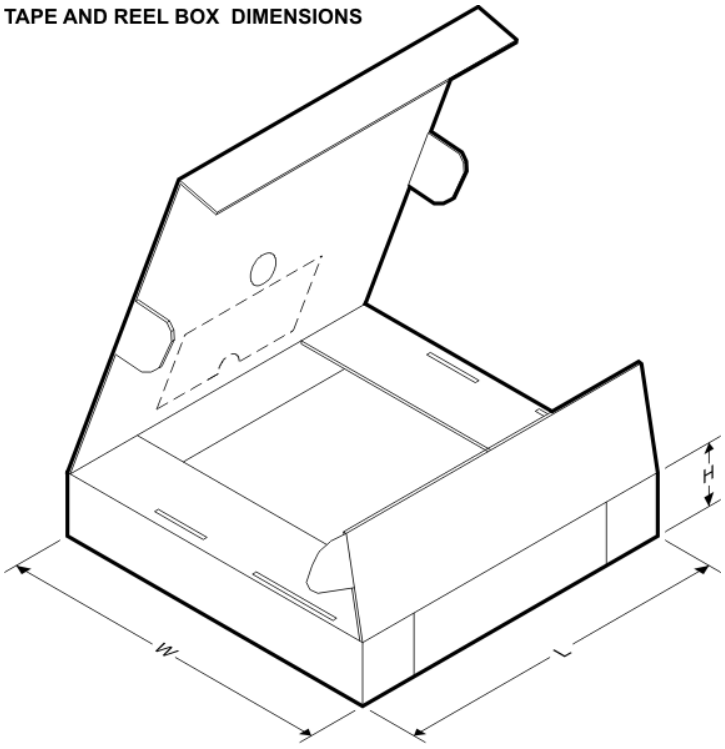

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74HC00DBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74HC00DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC00DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC00DR | SOIC | D | 14 | 2500 | 330.0 | 16.8 | 6.5 | 9.5 | 2.3 | 8.0 | 16.0 | Q1 |
| SN74HC00DRG4 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC00DT | SOIC | D | 14 | 250 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC00PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HC00PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HC00PWRG4 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HC00PWT | TSSOP | PW | 14 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

# PACKAGE MATERIALS INFORMATION



**TAPE AND REEL BOX DIMENSIONS**

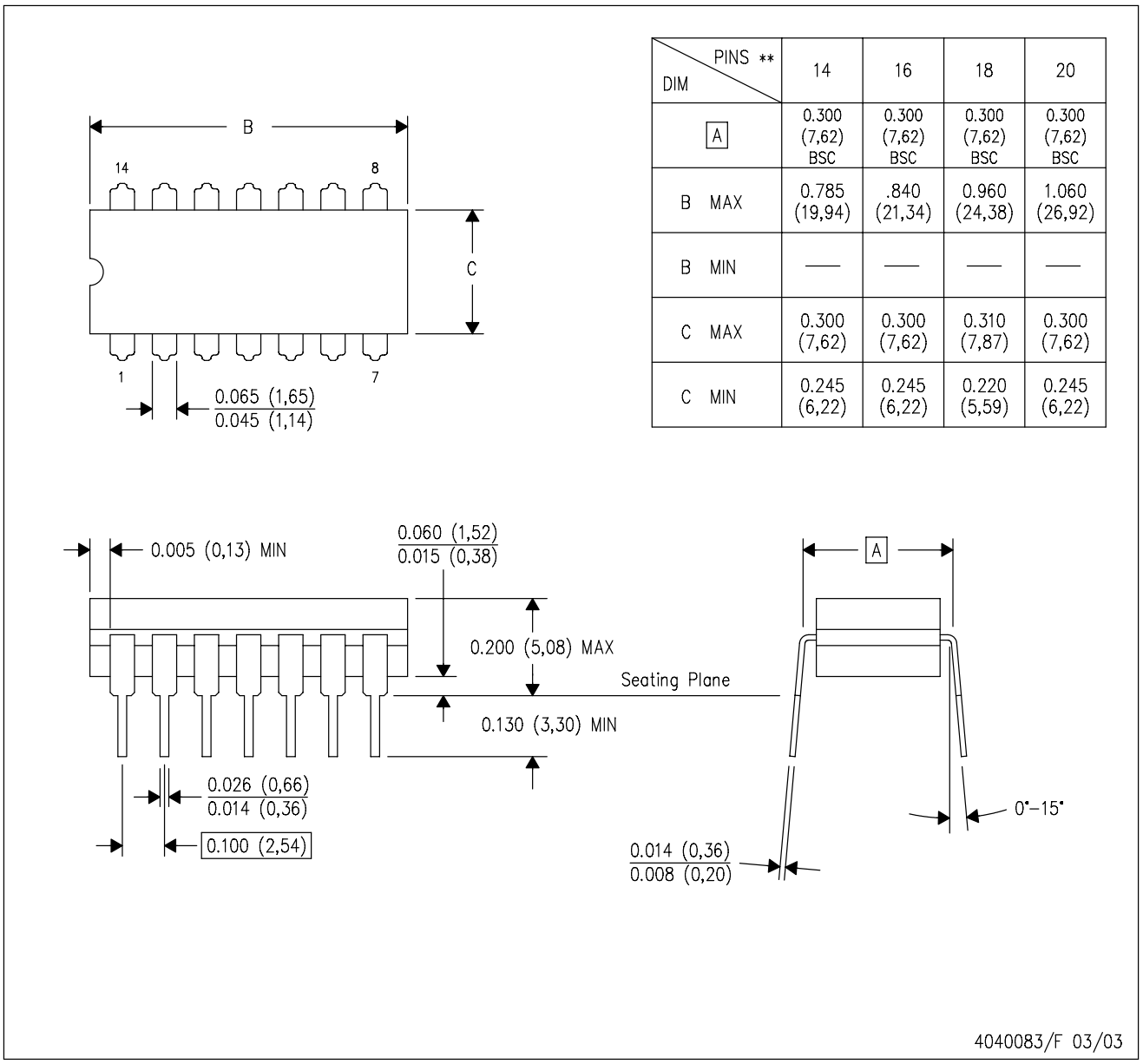



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74HC00DBR | SSOP | DB | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74HC00DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74HC00DR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74HC00DR | SOIC | D | 14 | 2500 | 364.0 | 364.0 | 27.0 |
| SN74HC00DRG4 | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74HC00DT | SOIC | D | 14 | 250 | 367.0 | 367.0 | 38.0 |
| SN74HC00PWR | TSSOP | PW | 14 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74HC00PWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74HC00PWRG4 | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74HC00PWT | TSSOP | PW | 14 | 250 | 367.0 | 367.0 | 35.0 |

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



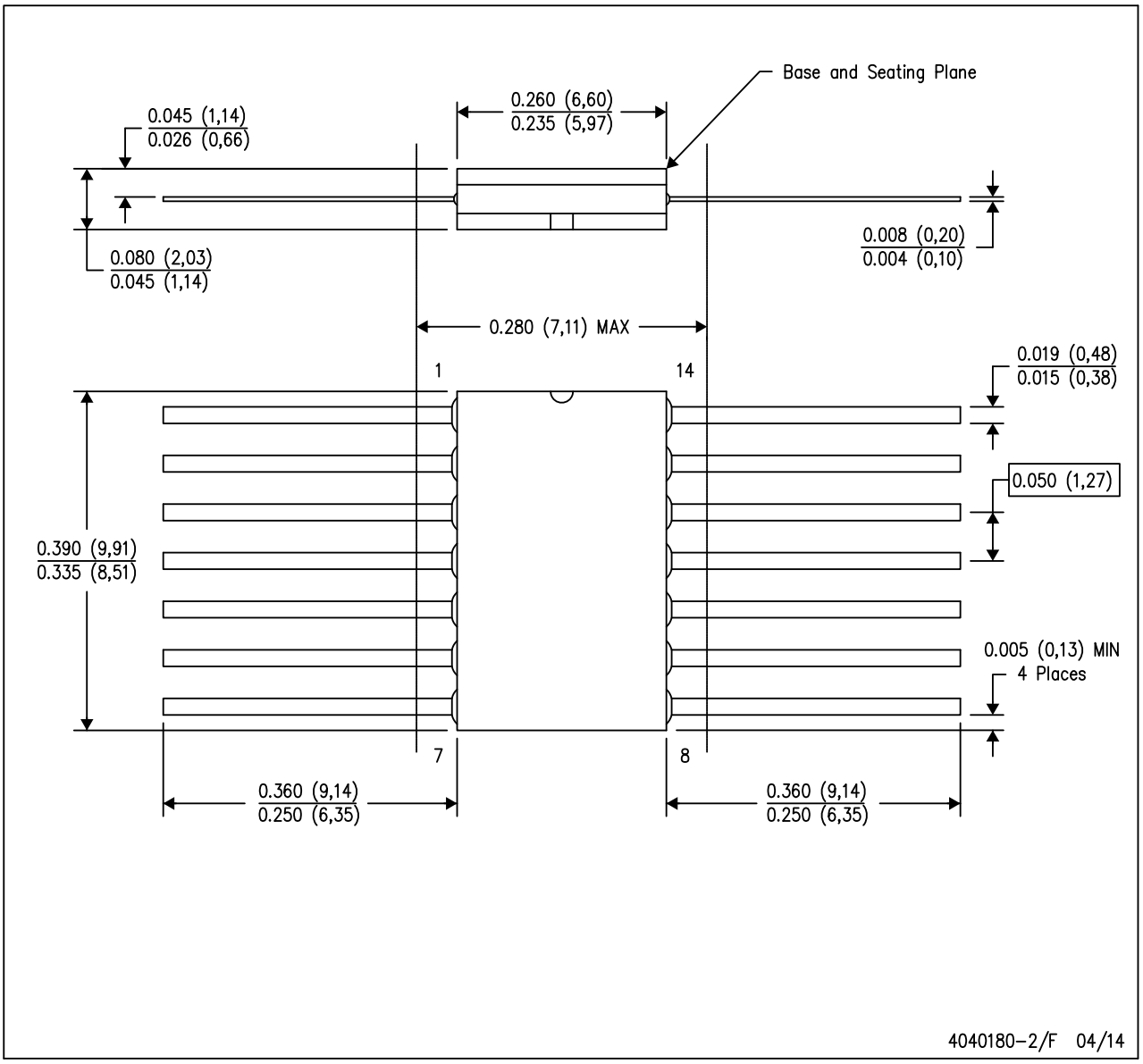

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

## MECHANICAL DATA

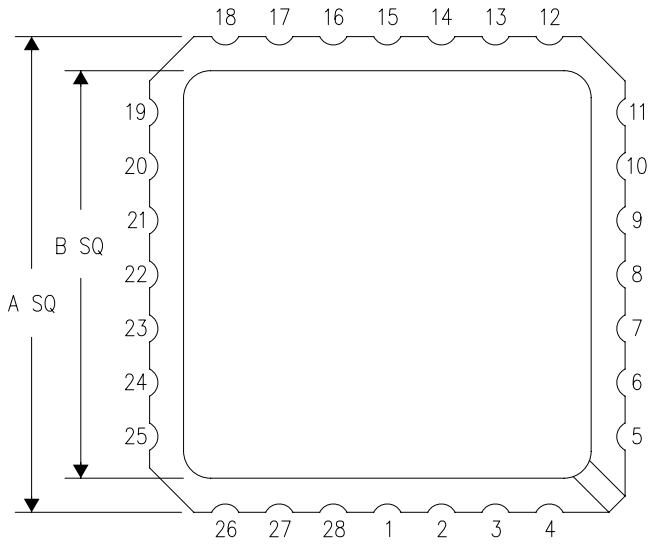
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



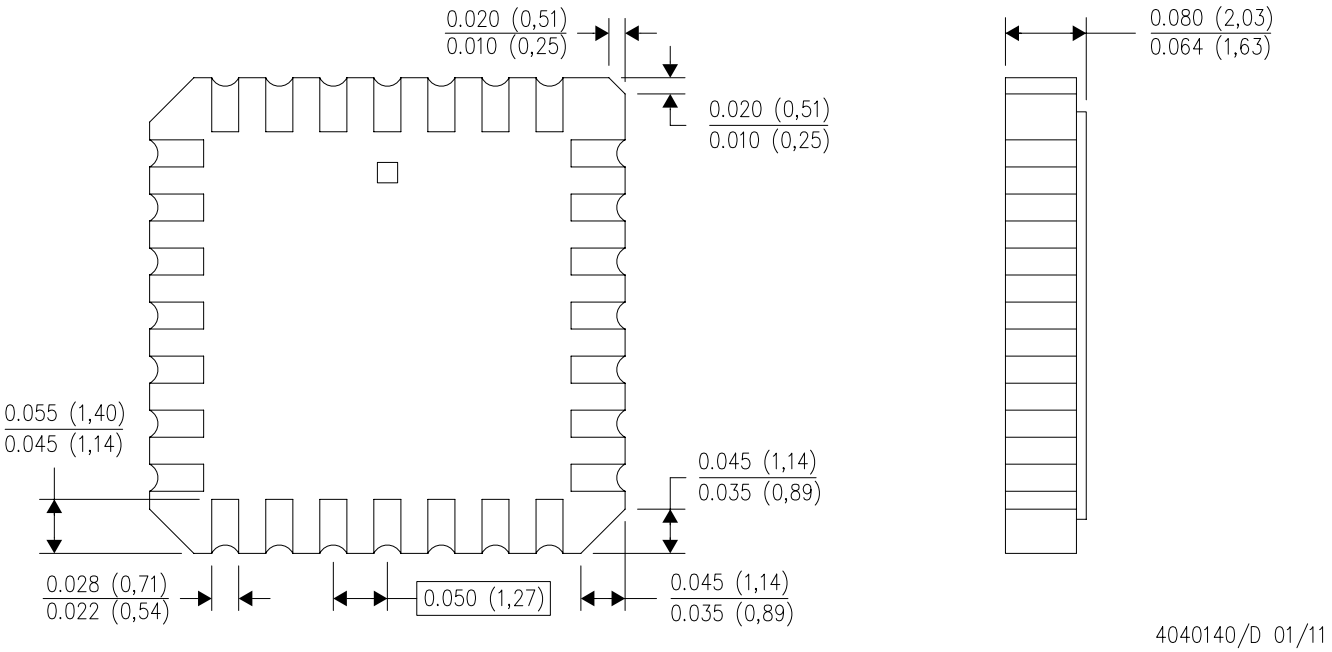

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN




| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



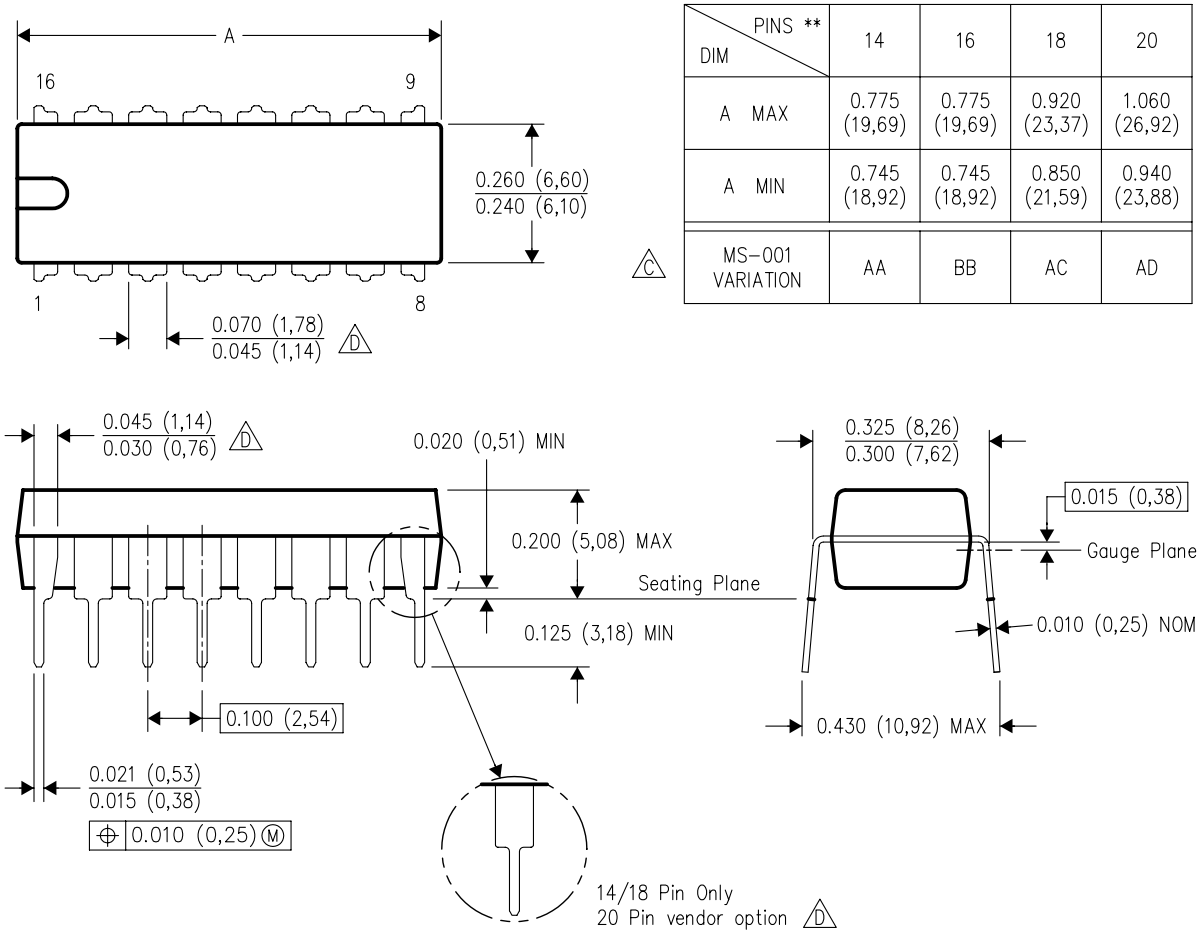

4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

## MECHANICAL DATA

### N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



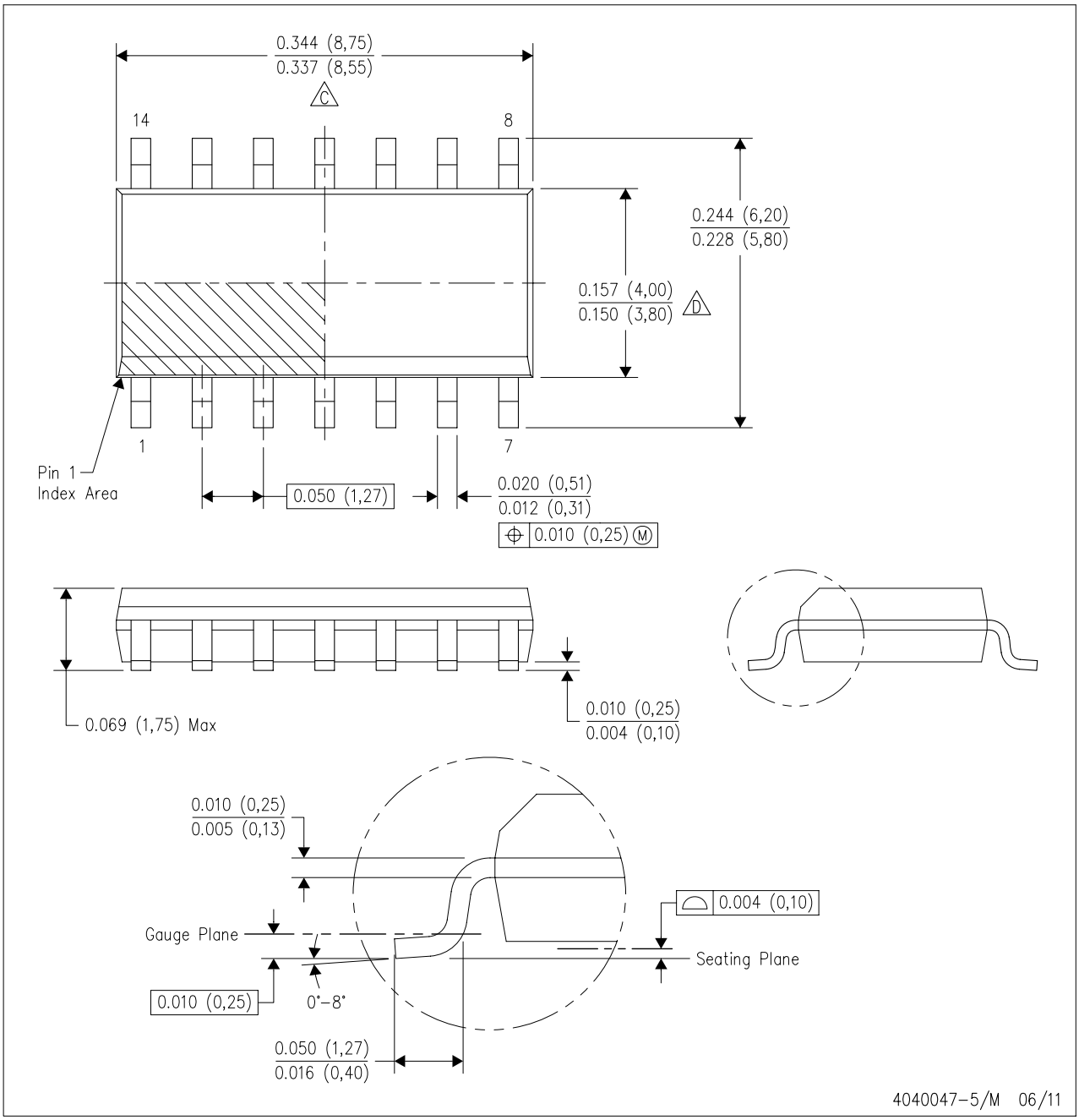

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION | AA | BB | AC | AD |

4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

## MECHANICAL DATA

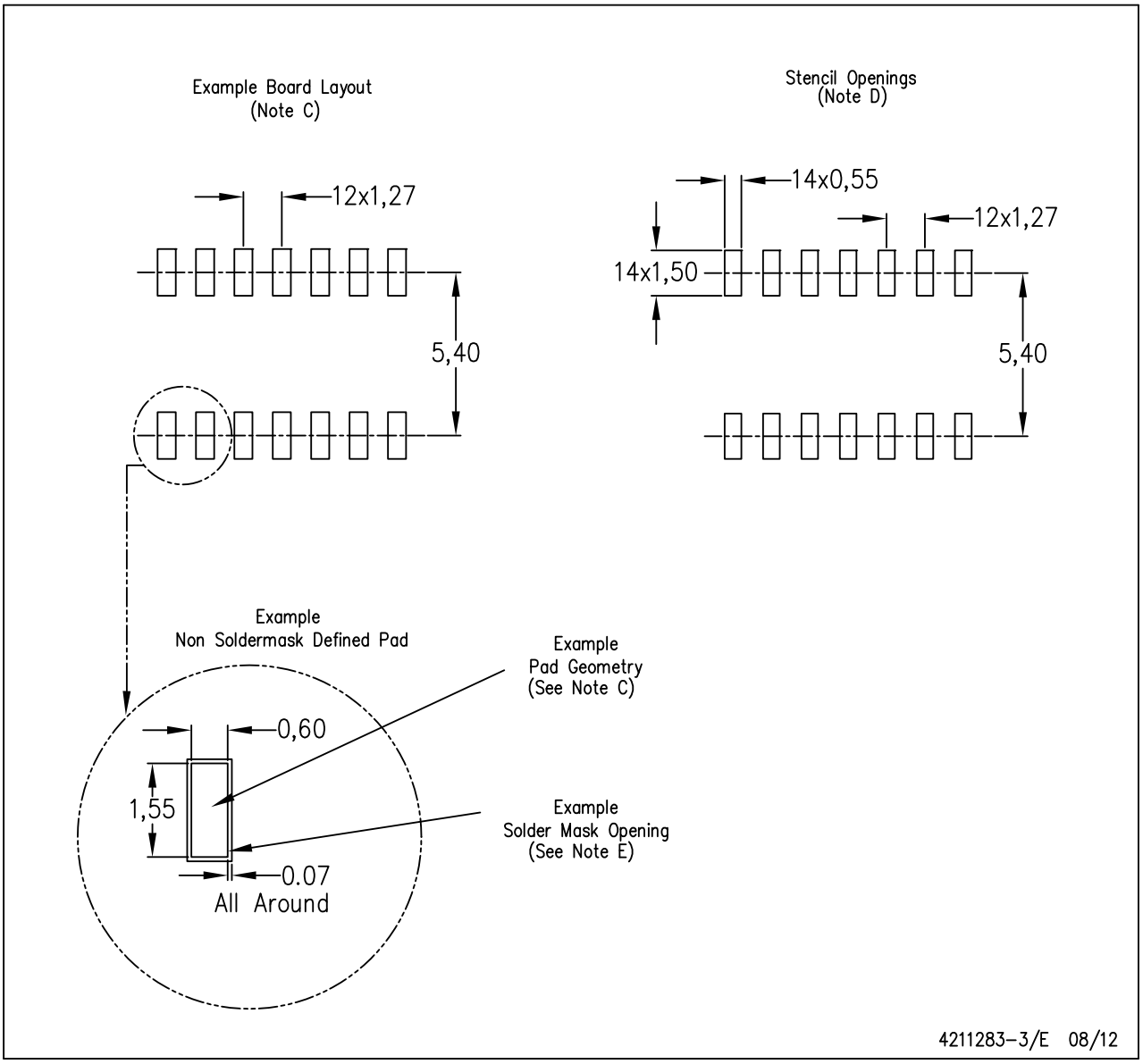
D (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

## LAND PATTERN DATA

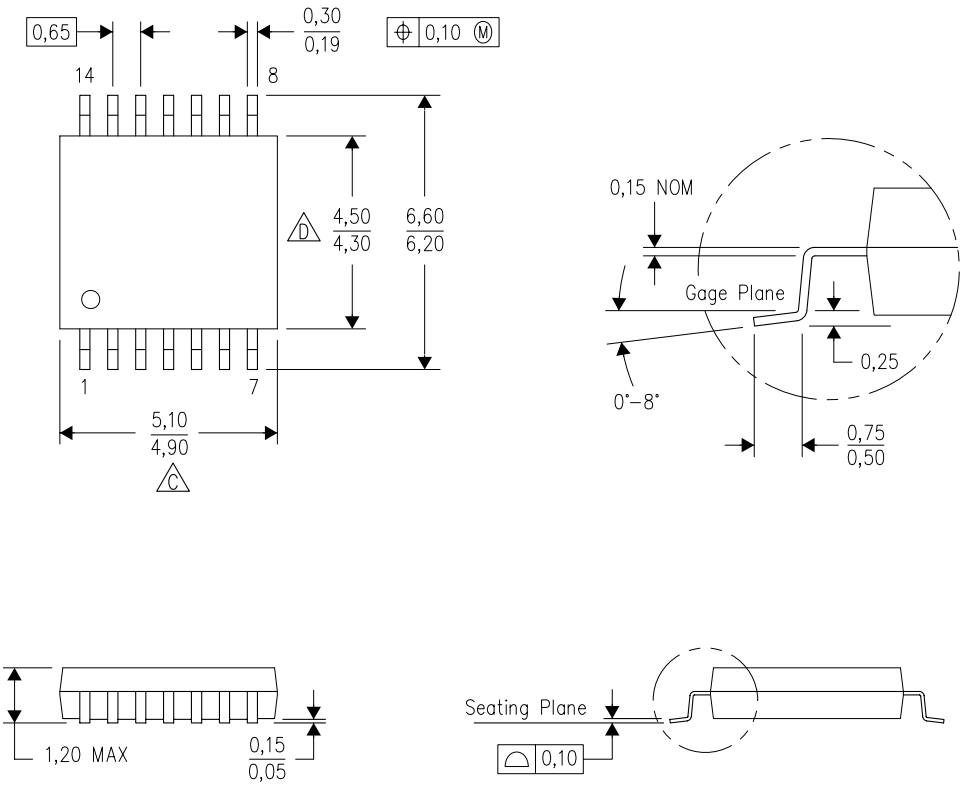
D (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

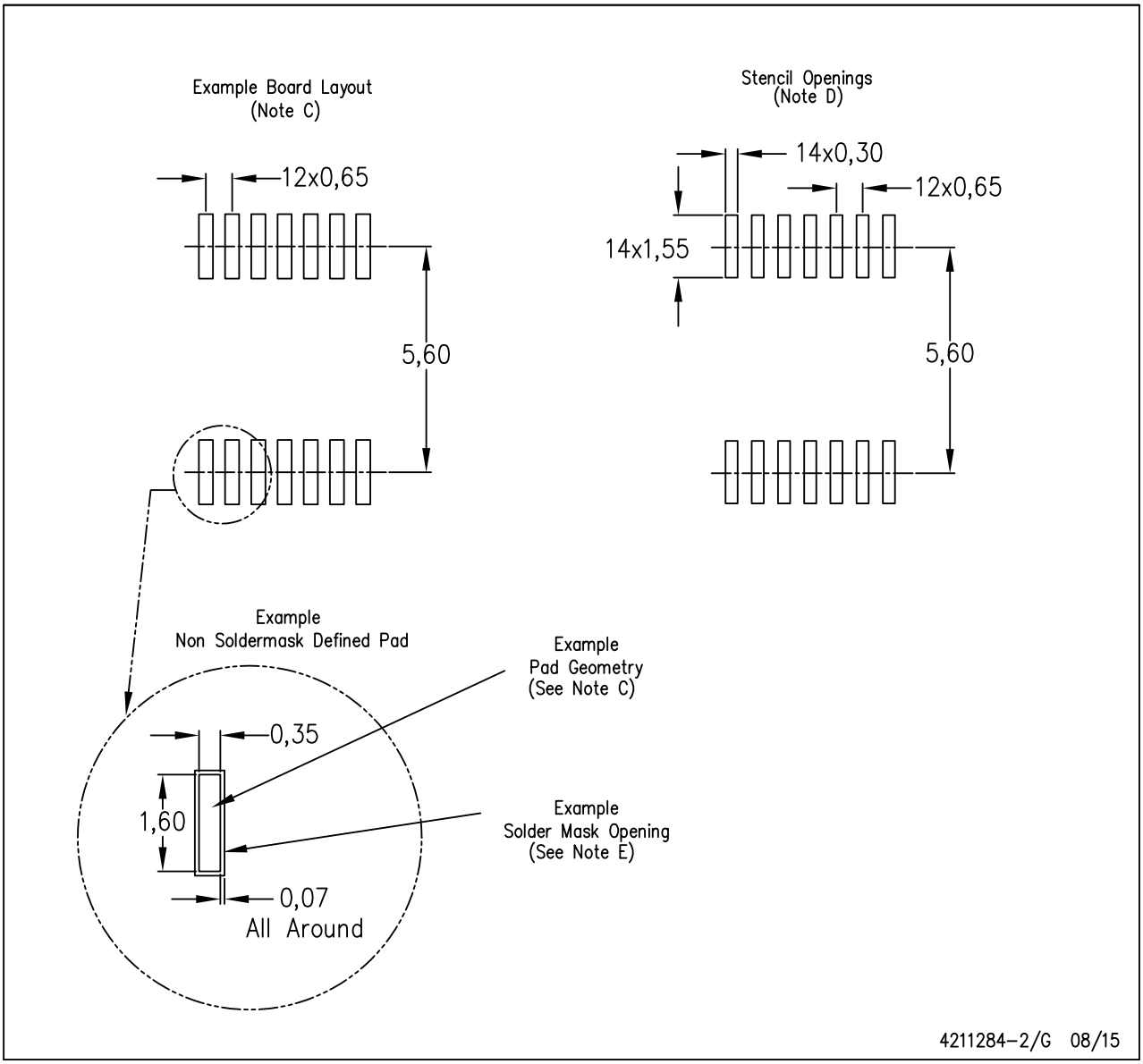



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

## LAND PATTERN DATA

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

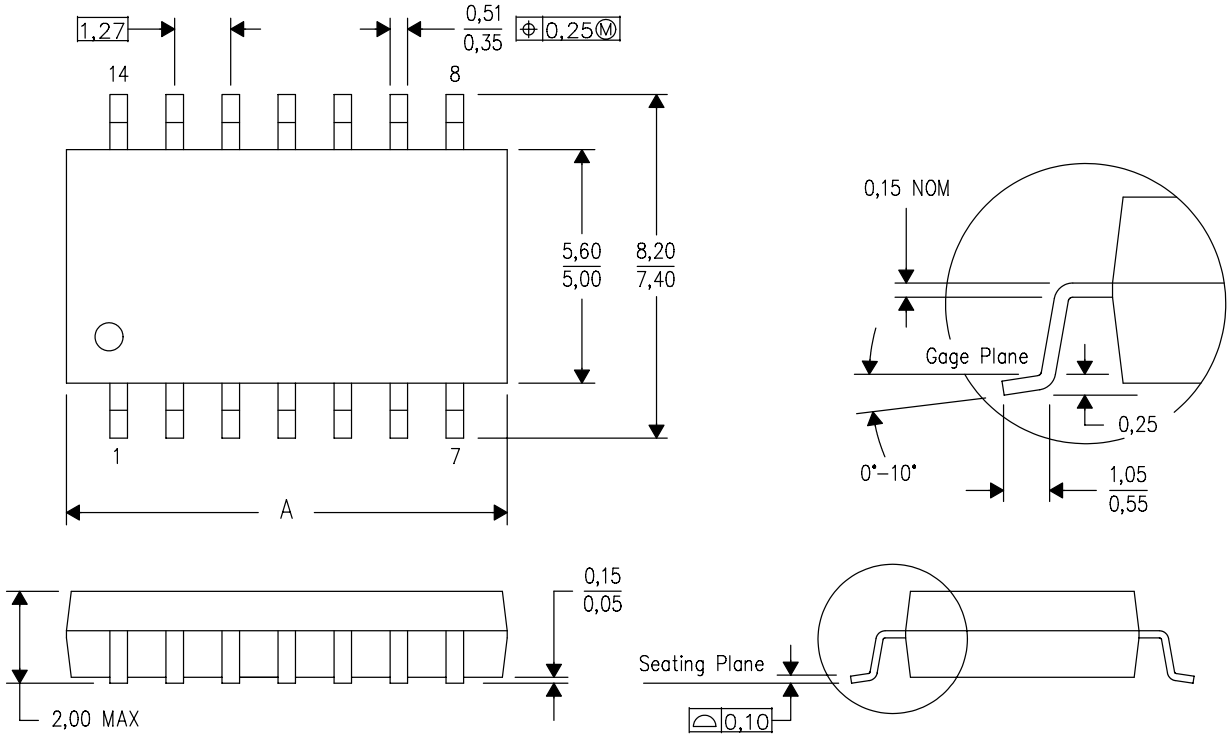



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

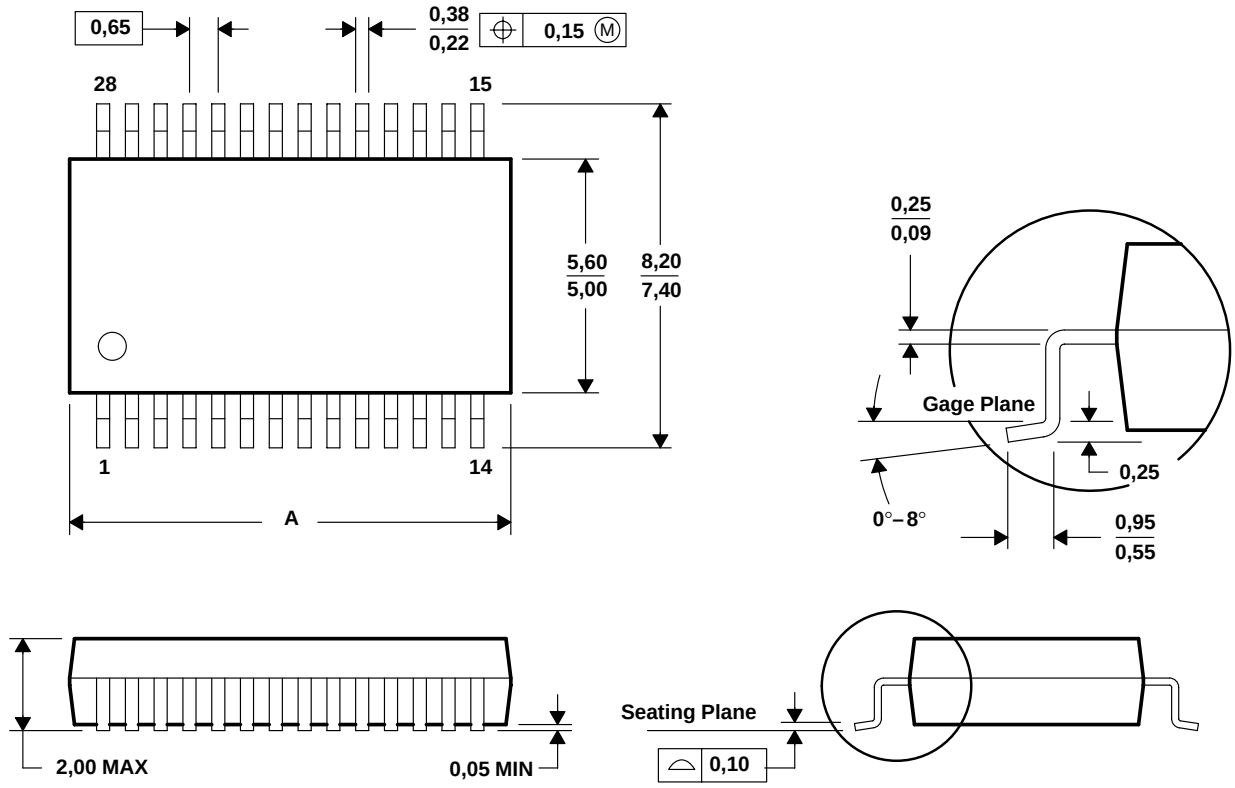
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## DB (R-PDSO-G**)

## PLASTIC SMALL-OUTLINE

**28 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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| DSP | dsp.ti.com | Energy and Lighting | www.ti.com/energy |
| Clocks and Timers | www.ti.com/clocks | Industrial | www.ti.com/industrial |
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