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SN74HC32DR

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SNx4HC32 Quadruple 2-Input Positive-OR Gates

1 Features

- Wide Operating Voltage Range: 2 V to 6 V
- Outputs Can Drive Up to 10 LSTTL Loads
- Low Power Consumption I_{CC}: 20 µA (Maximum)
- Typical t_{pd}: 8 ns
- ±4-mA Output Drive at 5 V
- Low Input Current: 1 µA (Maximum)

2 Applications

- Education
- Toys
- Musical Instruments
- Medical Healthcare and Fitness
- Grid Infrastructure
- Electronic Point of Sale
- Test and Measurement
- Factory Automation and Control
- Building Automation

3 Description

The SNx4HC32 devices contain four independent 2-input OR gates. They perform the boolean function $Y = \overline{A} \bullet \overline{B}$ or $Y = A + B$ in positive logic.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN54HC32J	CDIP (14)	19.94 mm × 7.62 mm
SN54HC32W	CFP (14)	9.21 mm × 7.11 mm
SN54HC32FK	LCCC (20)	8.89 mm × 8.89 mm
SN74HC32D	SOIC (14)	4.90 mm × 3.91 mm
SN74HC32DB	SSOP (14)	6.20 mm × 5.30 mm
SN74HC32N	PDIP (14)	19.30 mm × 6.35 mm
SN74HC32NS	SO (14)	10.30 mm × 5.30 mm
SN74HC32PW	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)

Table of Contents

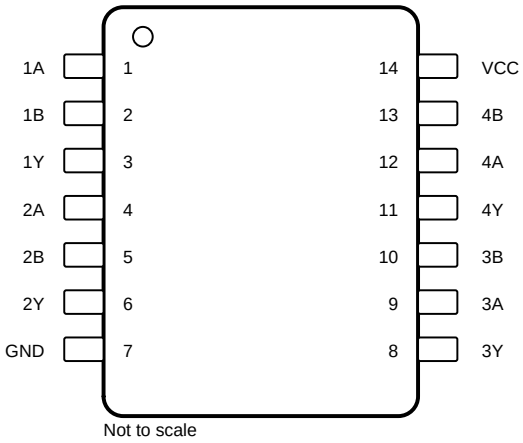
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August 2003) to Revision E	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Removed Ordering Information table	1
• Updated values in the *Thermal Information* tables to align with JEDEC standards	5

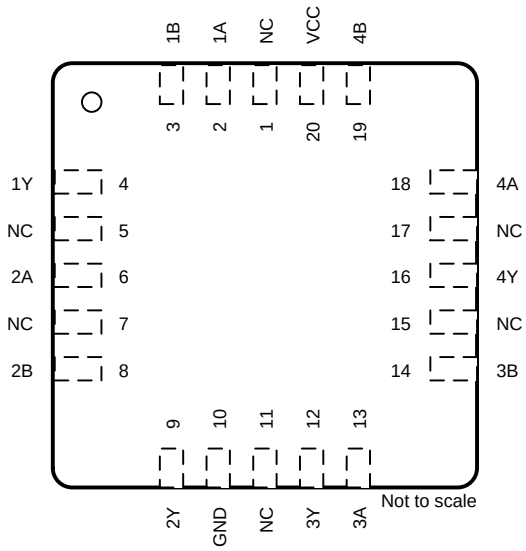
5 Pin Configuration and Functions

D, DB, J, N, NS, PW, W Package
14-Pin SOIC, SSOP, CDIP, PDIP, SOP, TSSOP, CFP
Top View



Not to scale

FK Package
20-Pin LCCC
Top View



Not to scale

Pin Functions

PIN			I/O	DESCRIPTION
NAME	D, DB, J, N, NS, PW, W	FK		
1A	1	2	I	Gate 1 input A
1B	2	3	I	Gate 1 input B
1Y	3	4	O	Gate 1 output
2A	4	6	I	Gate 2 input A
2B	5	8	I	Gate 2 input B
2Y	6	9	O	Gate 2 output
3A	9	13	I	Gate 3 input A
3B	10	14	I	Gate 3 input B
3Y	8	12	O	Gate 3 output
4A	12	18	I	Gate 4 input A
4B	13	19	I	Gate 4 input B
4Y	11	16	O	Gate 4 output
GND	7	10	—	Ground
NC	—	1, 5, 7, 11, 15, 17	—	No internal connection
V_{CC}	14	20	—	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current(2)	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings: SN74HC32

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 6 V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 6 V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall time	V_{CC} = 2 V			1000	ns
		V_{CC} = 4.5 V			500	
		V_{CC} = 6 V			400	
T_A	Operating free-air temperature	SN54HC32	–55		125	°C
		SN74HC32	–40		85	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to *Implications of Slow or Floating CMOS Inputs* application report.

6.4 Thermal Information: SN54HC32

THERMAL METRIC(1)		SN54HC32			UNIT
		CDIP (J)	CFP (W)	LCCC (FK)	
		14 PINS	14 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	—	—	—	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.9	88.3	61	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	80.1	156	59.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	—	—	—	°C/W
ψ_{JB}	Junction-to-board characterization parameter	—	—	—	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	25.1	15.2	11.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: SN74HC32

THERMAL METRIC(1)		SN74HC32					UNIT
		SOIC (D)	SSOP (DB)	PDIP (N)	SOP (NS)	TSSOP (PW)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.1	105.4	54.9	88.8	119.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.3	57.3	42.5	46.5	48.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.4	52.7	34.7	47.6	61.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.9	22.6	27.9	16.8	5.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44.1	52.2	34.6	47.2	60.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 µA	V_{CC} = 2 V	1.9	1.998		V
			V_{CC} = 4.5 V	4.4	4.499		
			V_{CC} = 6 V	5.9	5.999		
		I_{OH} = –4 mA, V_{CC} = 4.5 V	T_A = 25°C	3.98	4.3		
			SN54HC32	3.7			
			SN74HC32	3.84			
		I_{OH} = –5.2 mA, V_{CC} = 6 V	T_A = 25°C	5.48	5.8		
			SN54HC32	5.2			
			SN74HC32	5.34			

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	V_{CC} = 2 V		0.002	0.1	V
			V_{CC} = 4.5 V		0.001	0.1	
			V_{CC} = 6 V		0.001	0.1	
		I_{OL} = 4 mA, V_{CC} = 4.5 V	T_A = 25°C		0.17	0.26	
			SN54HC32			0.4	
			SN74HC32			0.33	
		I_{OL} = 5.2 mA, V_{CC} = 6 V	T_A = 25°C		0.15	0.26	
			SN54HC32			0.4	
			SN74HC32			0.33	
I_I	$V_I = V_{CC}$ or 0, V_{CC} = 6 V		T_A = 25°C		±0.1	±100	nA
			SNx4HC32			±1000	
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0, V_{CC} = 6 V		T_A = 25°C			2	µA
			SN54HC32			40	
			SN74HC32			20	
C_i	V_{CC} = 2 V to 6 V				3	10	pF
C_{pd} Power dissipation capacitance per gate	T_A = 25°C, no load				20		pF

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted; see Figure 4)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{pd}	C_L = 50 pF, from A or B (input) to Y (output)	V_{CC} = 2 V	T_A = 25°C		50	100	ns
			SN54HC32			150	
			SN74HC32			125	
		V_{CC} = 4.5 V	T_A = 25°C		10	20	
			SN54HC32			30	
			SN74HC32			25	
		V_{CC} = 6 V	T_A = 25°C		8	17	
			SN54HC32			25	
			SN74HC32			21	
t_t	C_L = 50 pF, to Y (output)	V_{CC} = 2 V	T_A = 25°C		38	75	ns
			SN54HC32			110	
			SN74HC32			95	
		V_{CC} = 4.5 V	T_A = 25°C		8	15	
			SN54HC32			22	
			SN74HC32			19	
		V_{CC} = 6 V	T_A = 25°C		6	13	
			SN54HC32			19	
			SN74HC32			16	

6.8 Typical Characteristics

T_A = 25°C and C_L = 50 pF

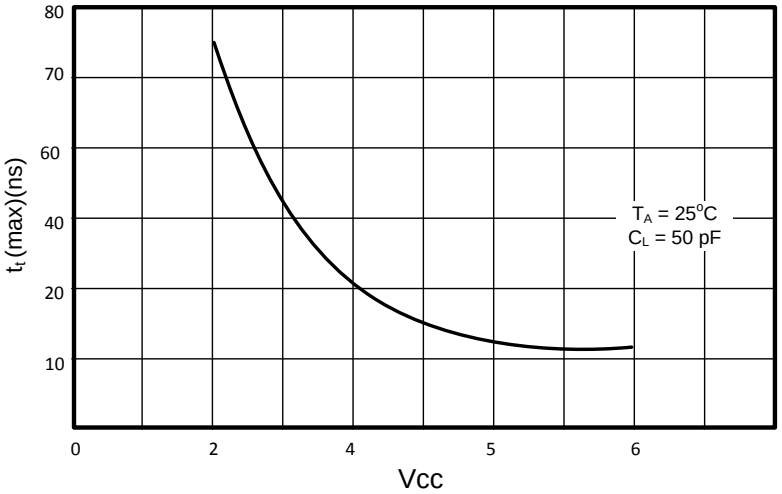


Figure 1. t_t vs V_{CC}

7 Parameter Measurement Information

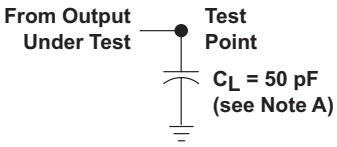


Figure 2. Load Current

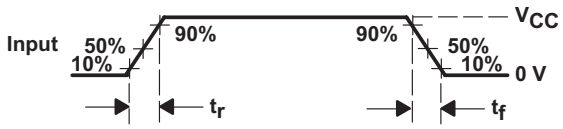
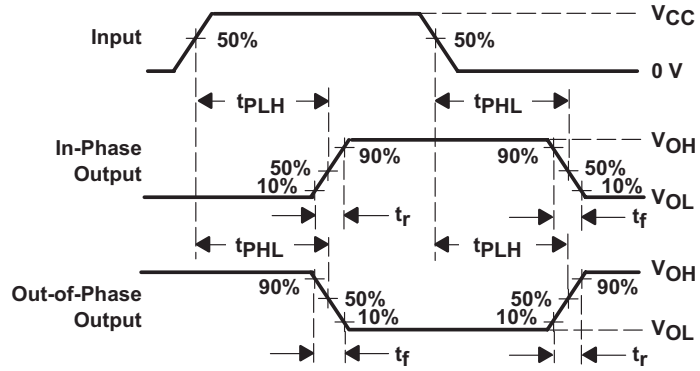


Figure 3. Input Rise and Fall Times



NOTES: A. C_L includes probe and test-fixture capacitance.

B. Phase relationship between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:
PRR ≤ 1 MHz, ZO = 50 Ω, t_r = 6 ns, t_f = 6 ns.

C. The outputs are measured one at a time with one input transition per measurements.

D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 4. Propagation Delay and Output Transition Times

8 Detailed Description

8.1 Overview

The SNx4HC32 devices are quad 2-input OR gates. These devices are members of the High-Speed CMOS (HC) logic family. The HC family of logic is optimized to operate with a 5-V supply, is low noise without characteristic overshoot and undershoot, has low power consumption, small propagation delay, balanced propagation delay and transition times, and operates over a wide temperature range.

8.2 Functional Block Diagram

Figure 5. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 Operating Voltage Range

The SNx4HC series of devices offer a wide operating voltage range from 2 V to 6 V.

8.3.2 LSTTL Loads

The outputs of the SNx4HC series can drive up to 10 LSTTL loads.

8.3.3 Low Power Consumption

The SNx4HC32 offers low power consumption of 20 μA (maximum).

8.3.4 Output Drive Capability

At 5 V, the outputs have ±4 mA of output drive capability.

8.3.5 Low Input Current Leakage

Inputs have low input current leakage of 1 μA (maximum).

8.4 Device Functional Modes

Table 1 lists the functional modes of SNx4HC32.

Table 1. Function Table (Each Gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

9 Application and Implementation

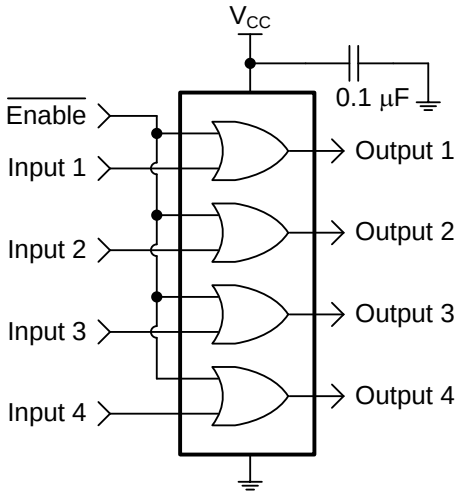
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SNx4HC32 is an extremely versatile device with far more available applications than could be listed here. The application chosen as an example is using all four OR gates in a single package to provide a four channel output enable from a single active low enable signal ($\overline{\text{Enable}}$). This circuit outputs a logic HIGH on all channels when disabled ($\overline{\text{Enable}}$ is HIGH), and passes the input signals when enabled ($\overline{\text{Enable}}$ is LOW).

9.2 Typical Application



Using a quad OR gate as a 4-channel active low enable with high output off state.

Figure 6. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

The minimum output pulse time is approximately three times t_{pd} from *Switching Characteristics* for the selected V_{CC}, device, and temperature range.

9.2.2 Detailed Design Procedure

Logic

- All four input channels are to be enabled or disabled simultaneously
- The enable signal is active low (LOW = enabled, HIGH = disabled)
- All four outputs are to output logic HIGH while disabled

Inputs

- Each input must follow requirements specified in *Absolute Maximum Ratings*:
  - Avoid exceeding input voltages

Typical Application (continued)

- If input voltages ratings must be exceeded, ensure that the maximum input current ratings are not exceeded.
- Ensure that the input signals have edge rates that are equal to or faster than that listed in *Recommended Operating Conditions*. Slower signals can cause incorrect behavior and possibly damage to the part.

• Each output must also follow requirements in *Absolute Maximum Ratings*:

- Avoid bus contention by only connecting outputs together when inputs are tied together directly.
- Avoid forcing output voltages outside those specified in *Absolute Maximum Ratings.*
- If output voltage ratings must be exceeded, ensure that the maximum output current ratings are not exceeded.
- Ensure that the total current output does not exceed the continuous current through V_{CC} or GND listed in *Absolute Maximum Ratings.*

9.2.3 Application Curves

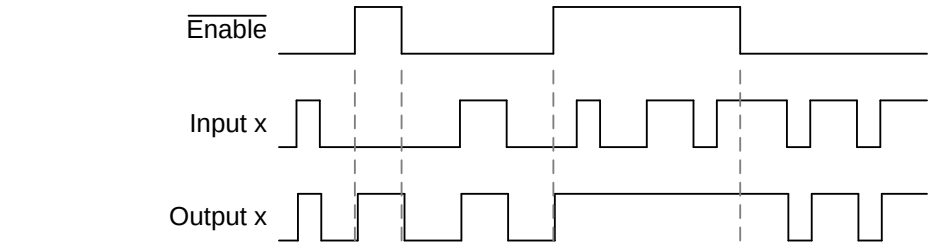


Figure 7. Application Timing Diagram

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions*. Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-μF bypass capacitor. If there are multiple V_{CC} pins, TI recommends a 0.01-μF or 0.022-μF bypass capacitors for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. Two bypass capacitors of value 0.1-μF and 1-μF are commonly used in parallel. For best results, install the bypass capacitor(s) as close to the power pin as possible.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs must not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in *Absolute Maximum Ratings* are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it disables the outputs section of the part when asserted. This does not disable the input section of the I/Os so they also cannot float when disabled.

11.2 Layout Example

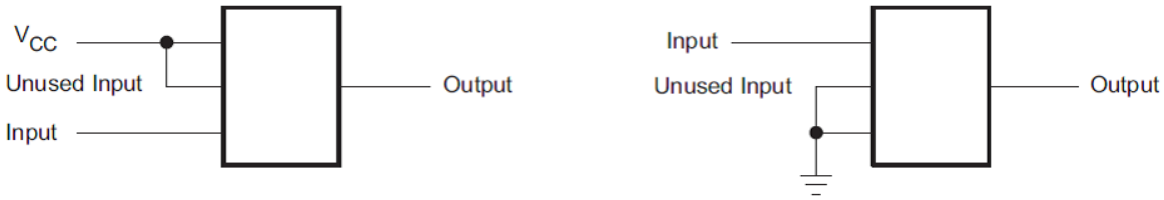


Figure 8. Layout Recommendation

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Implications of Slow or Floating CMOS Inputs* (SCBA004)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HC32	Click here	Click here	Click here	Click here	Click here
SN74HC32	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8404501VCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8404501VC A SNV54HC32J	Samples
5962-8404501VDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8404501VD A SNV54HC32W	Samples
84045012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84045012A SNJ54HC 32FK	Samples
8404501CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8404501CA SNJ54HC32J	Samples
8404501DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8404501DA SNJ54HC32W	Samples
JM38510/65201B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 65201B2A	Samples
JM38510/65201BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65201BCA	Samples
JM38510/65201BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65201BDA	Samples
M38510/65201B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 65201B2A	Samples
M38510/65201BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65201BCA	Samples
M38510/65201BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65201BDA	Samples
SN54HC32J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54HC32J	Samples
SN74HC32D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC32	Samples
SN74HC32DBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI	-40 to 85		
SN74HC32DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC32	Samples
SN74HC32DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC32	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC32DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC32	Samples
SN74HC32DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	HC32	Samples
SN74HC32DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC32	Samples
SN74HC32DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC32	Samples
SN74HC32DT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC32	Samples
SN74HC32N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC32N	Samples
SN74HC32N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	-40 to 85		
SN74HC32NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC32N	Samples
SN74HC32NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC32	Samples
SN74HC32PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC32	Samples
SN74HC32PWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC32	Samples
SN74HC32PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC32	Samples
SN74HC32PWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85		
SN74HC32PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	HC32	Samples
SN74HC32PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC32	Samples
SN74HC32PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC32	Samples
SN74HC32PWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC32	Samples
SN74HC32PWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC32	Samples
SNJ54HC32FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84045012A SNJ54HC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										32FK	
SNJ54HC32J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8404501CA SNJ54HC32J	Samples
SNJ54HC32W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8404501DA SNJ54HC32W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54HC32, SN54HC32-SP, SN74HC32 :

- Catalog: SN74HC32, SN54HC32
- Military: SN54HC32
- Space: SN54HC32-SP

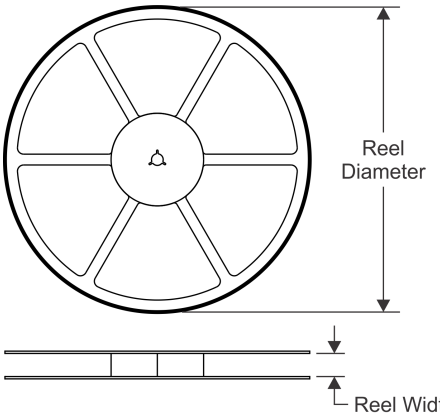
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

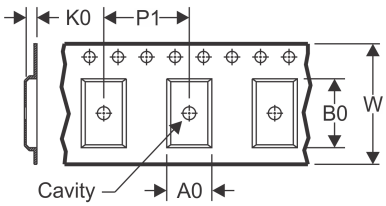
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

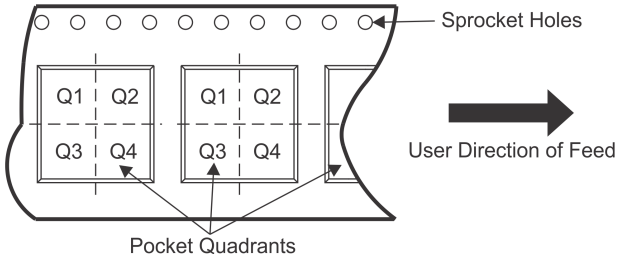


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

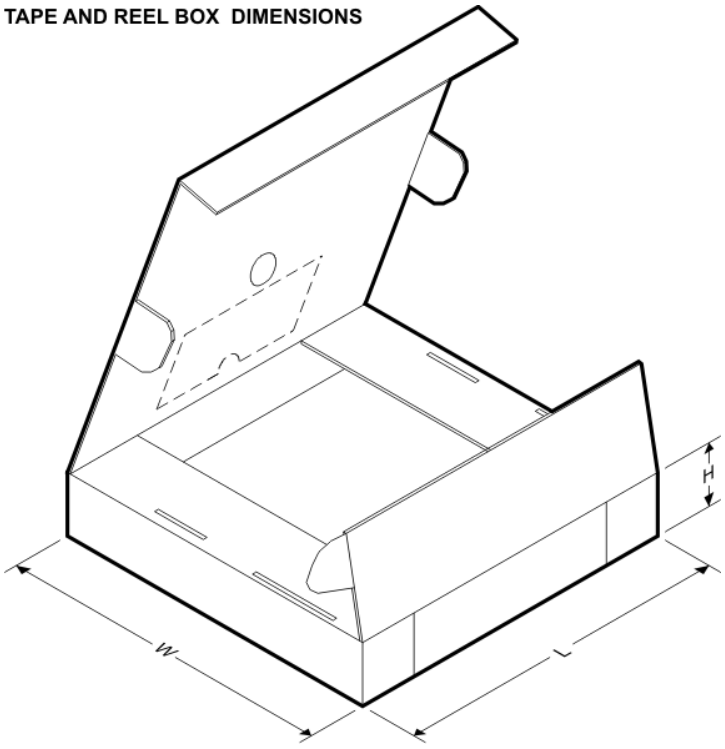


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC32DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74HC32DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC32DR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.3	8.0	16.0	Q1
SN74HC32DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC32DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC32DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC32DT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC32PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC32PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC32PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC32PWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

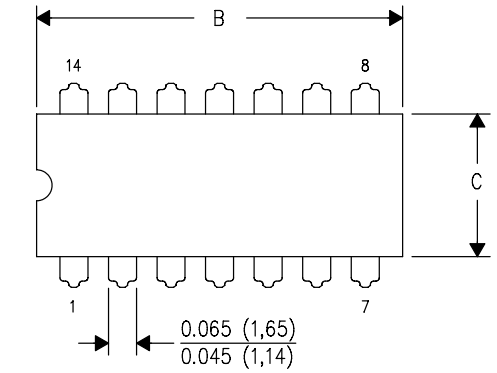


*All dimensions are nominal

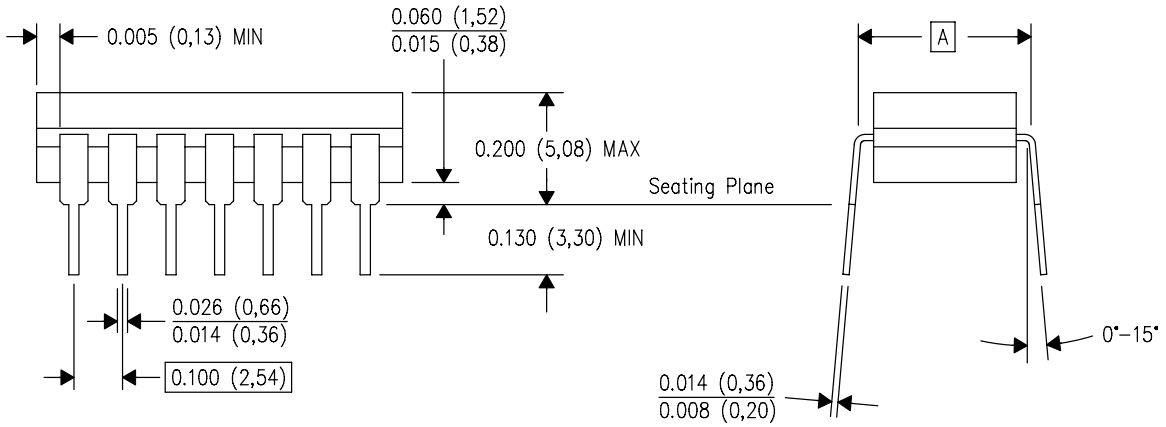
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC32DBR	SSOP	DB	14	2000	367.0	367.0	38.0
SN74HC32DR	SOIC	D	14	2500	333.2	345.9	28.6
SN74HC32DR	SOIC	D	14	2500	364.0	364.0	27.0
SN74HC32DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74HC32DRG4	SOIC	D	14	2500	333.2	345.9	28.6
SN74HC32DRG4	SOIC	D	14	2500	367.0	367.0	38.0
SN74HC32DT	SOIC	D	14	250	367.0	367.0	38.0
SN74HC32PWR	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74HC32PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74HC32PWRG4	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74HC32PWT	TSSOP	PW	14	250	367.0	367.0	35.0

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

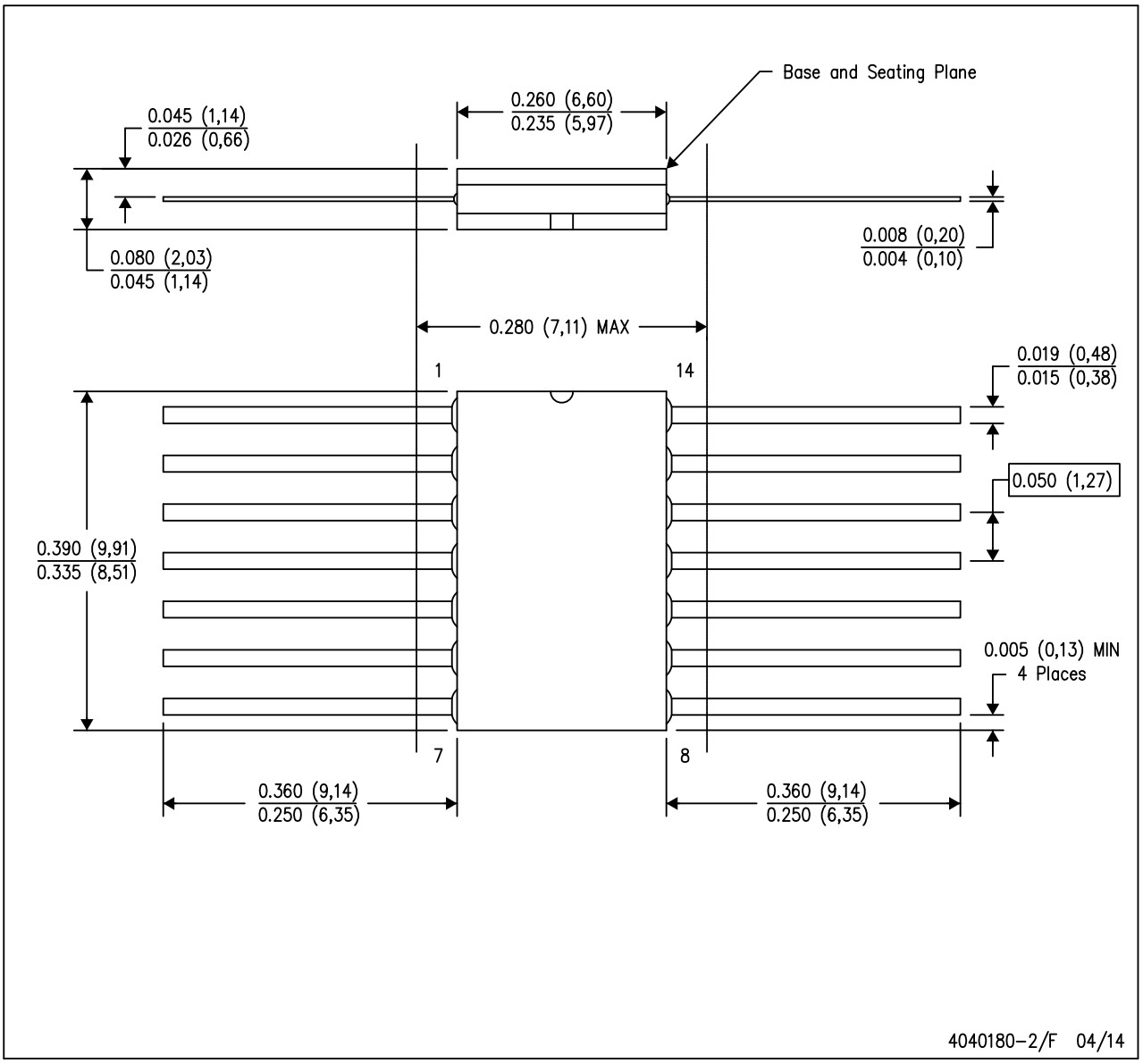


4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

MECHANICAL DATA

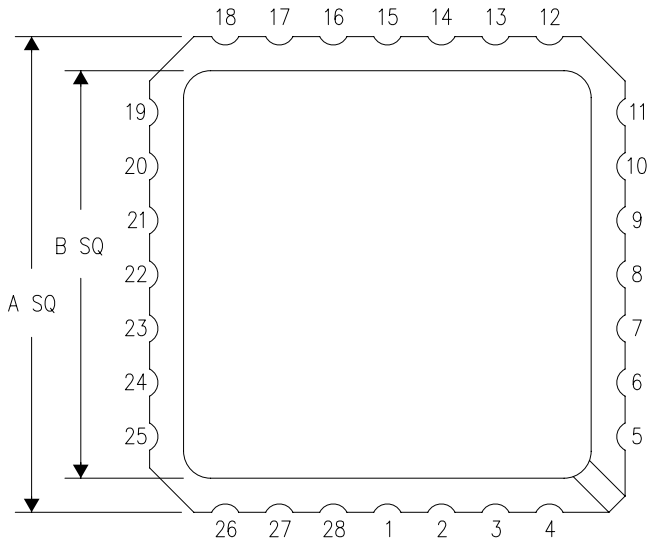
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



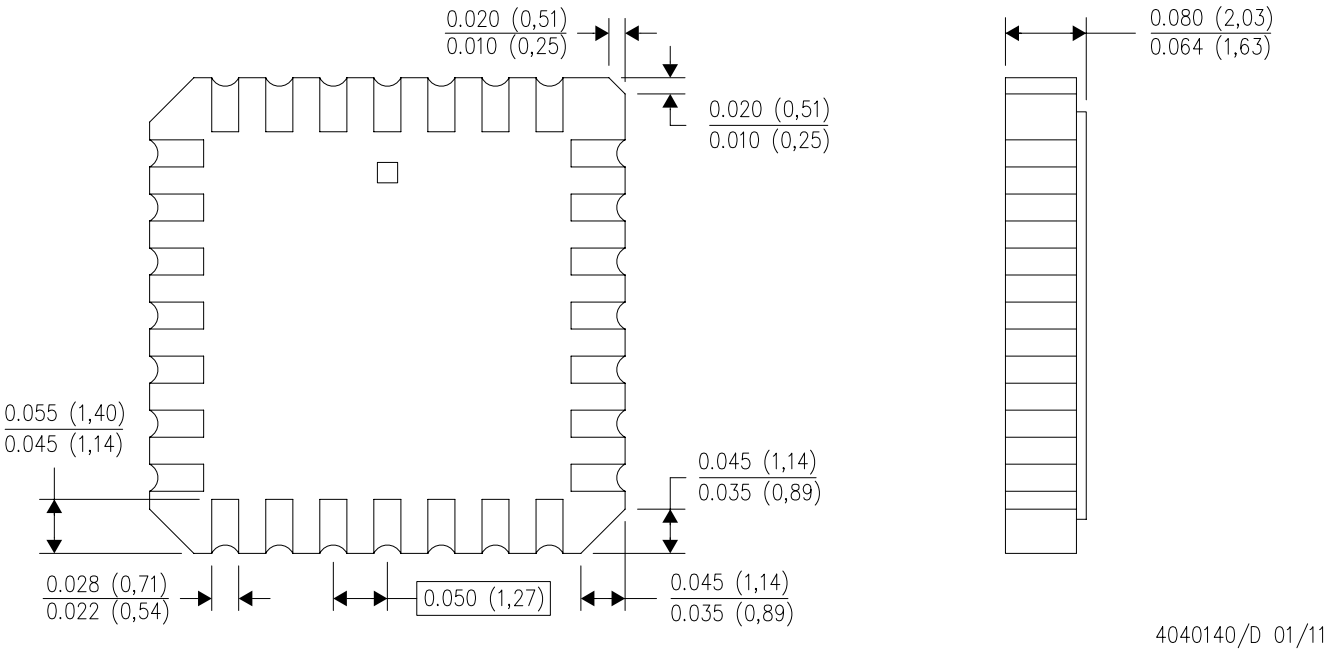
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



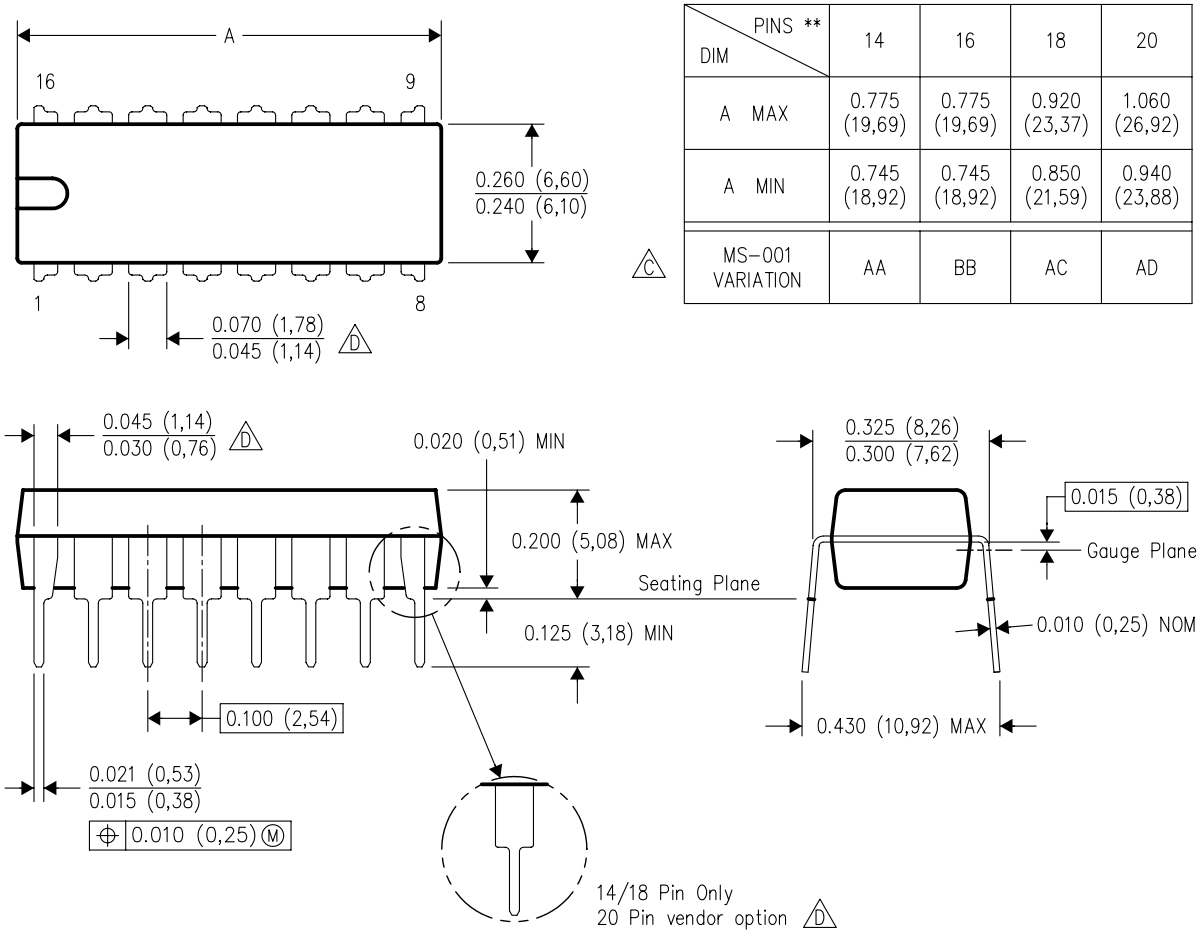
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

MECHANICAL DATA

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



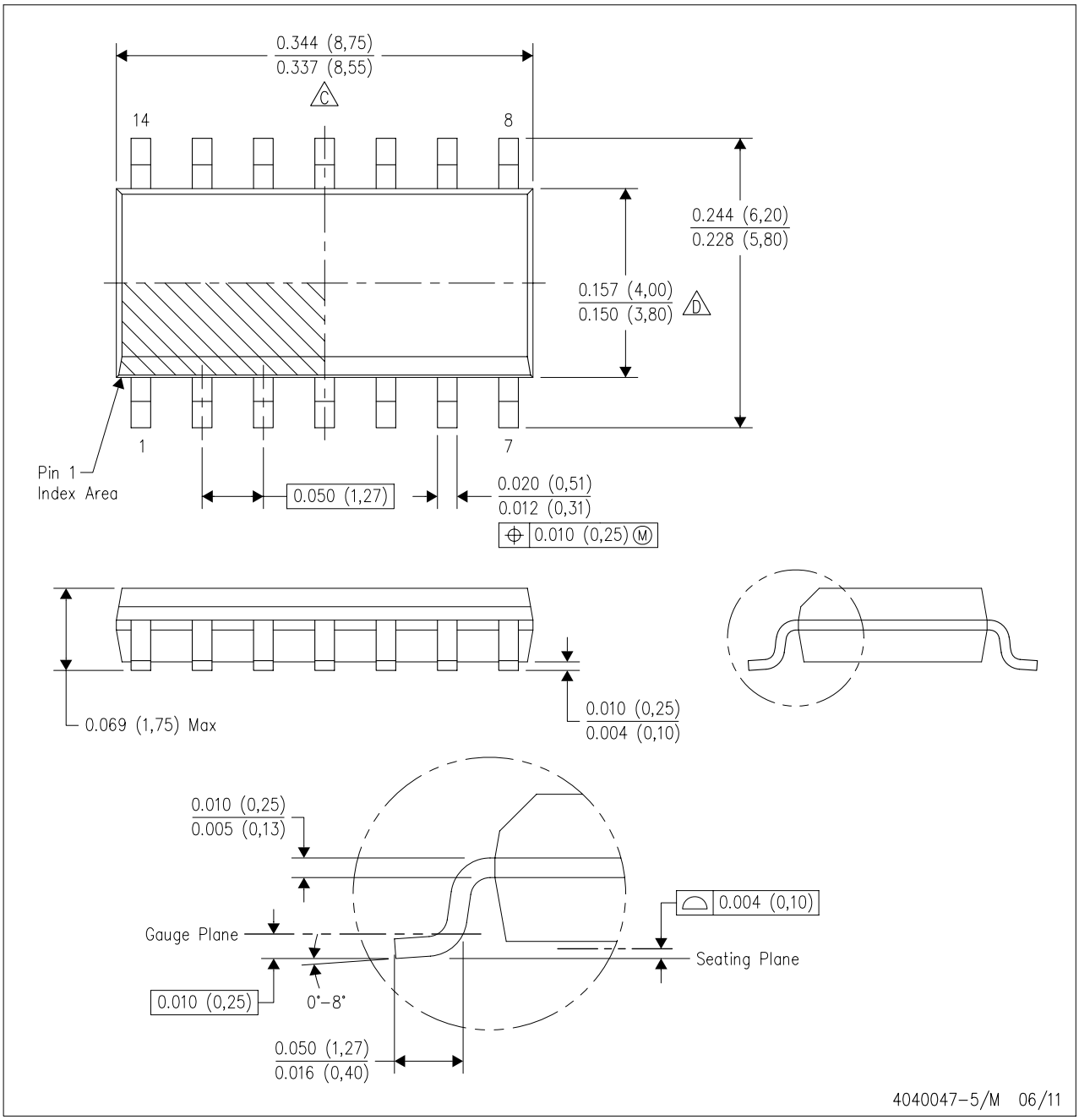
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

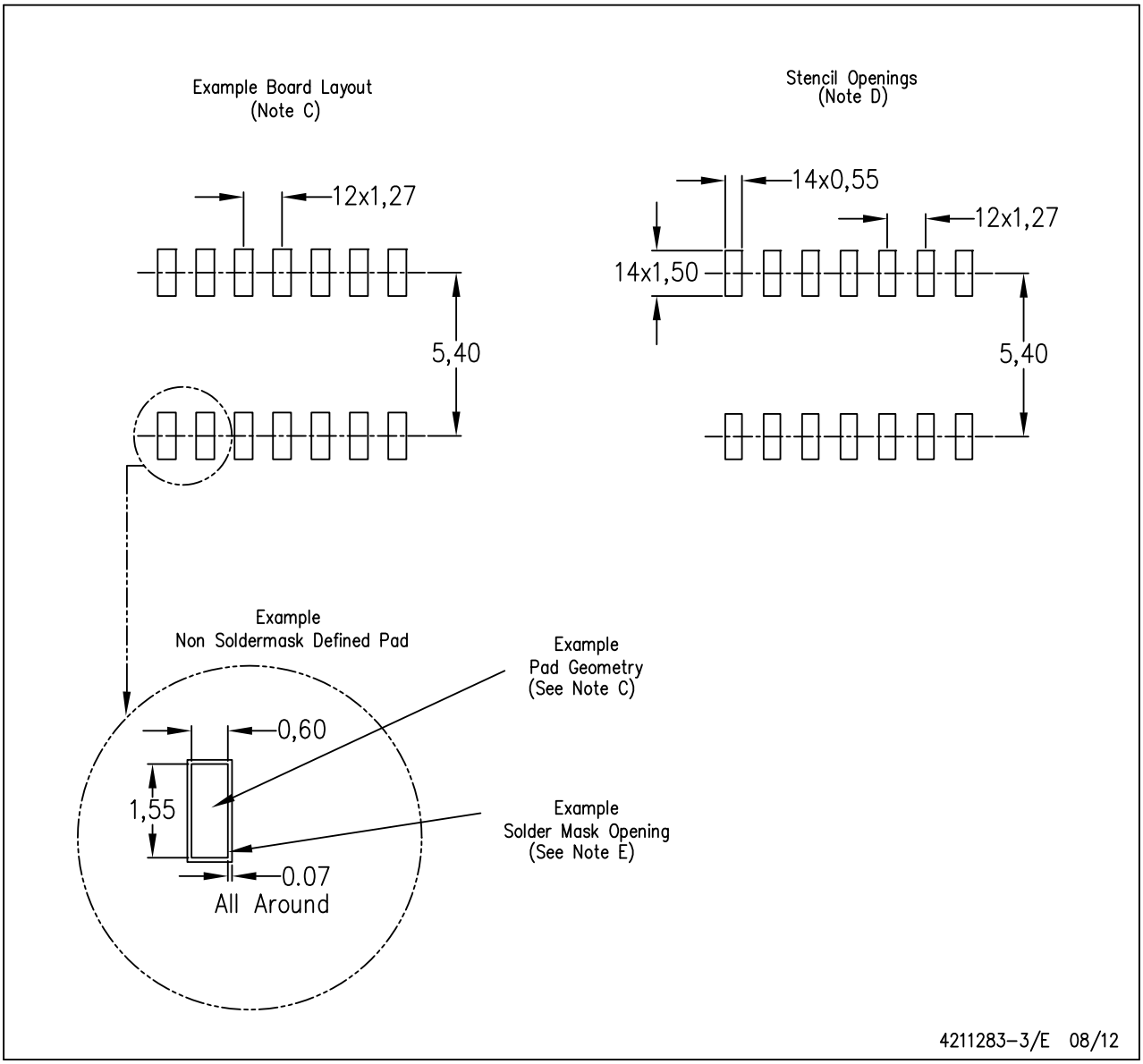
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

LAND PATTERN DATA

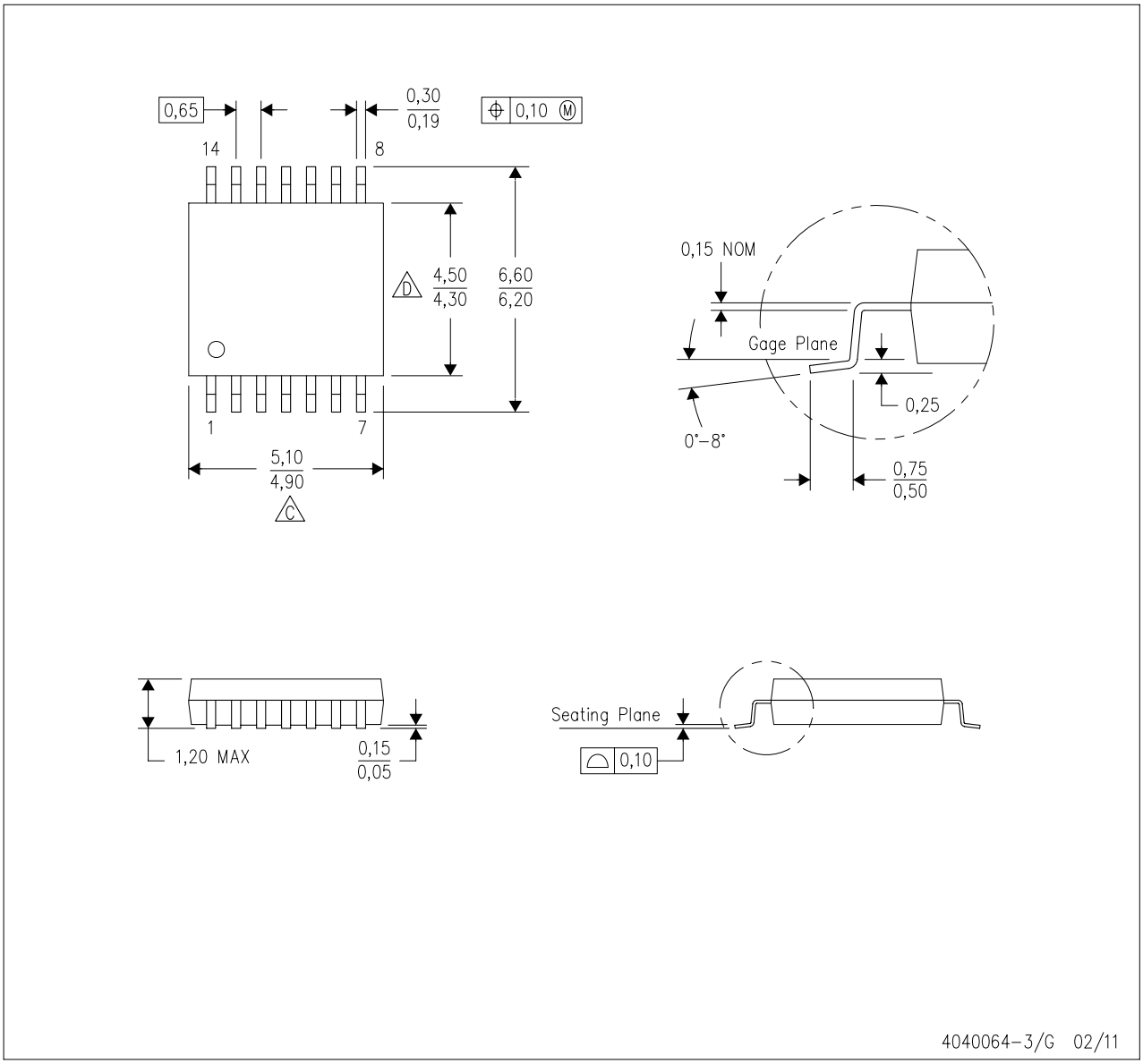
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

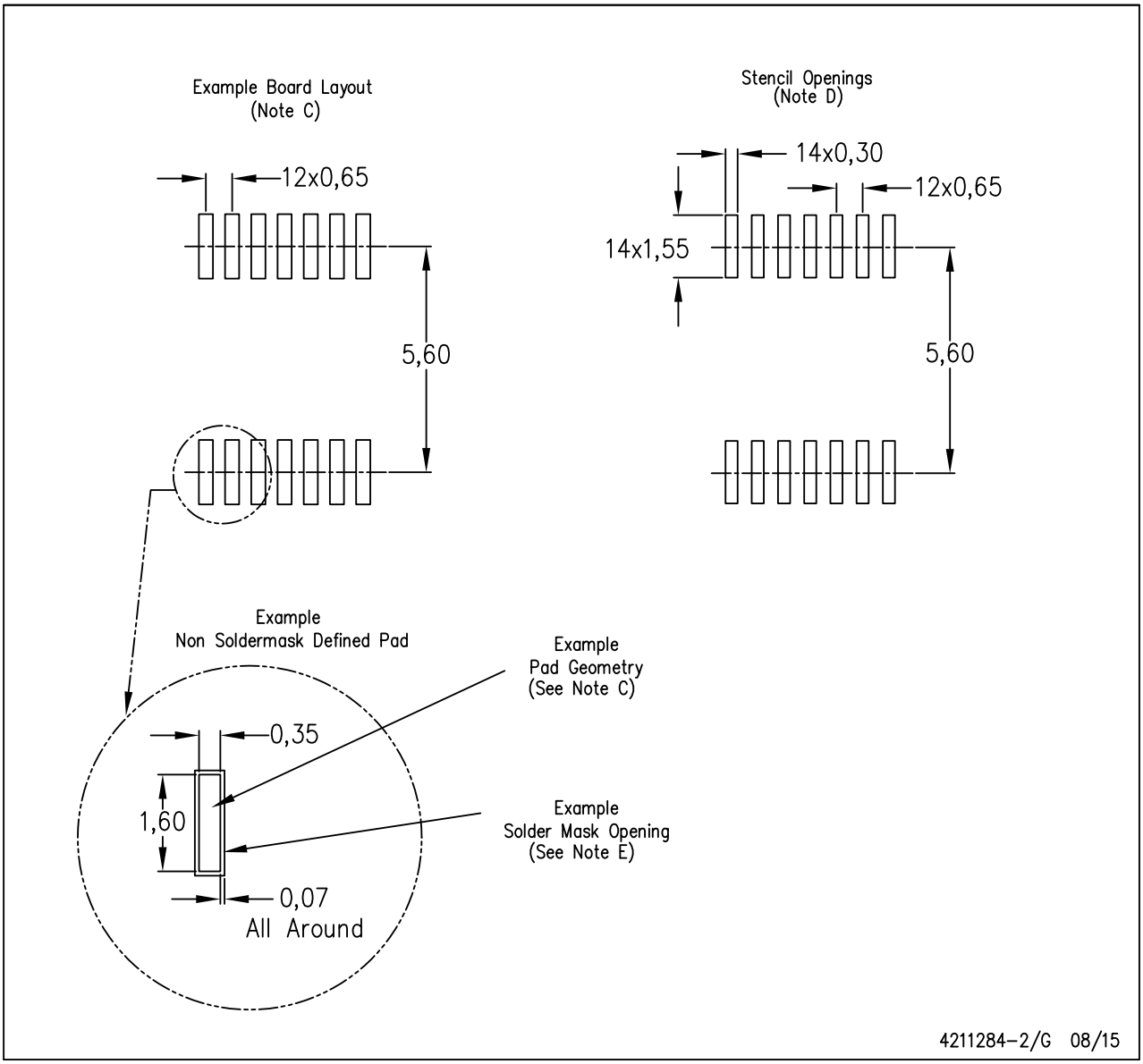
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

LAND PATTERN DATA

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

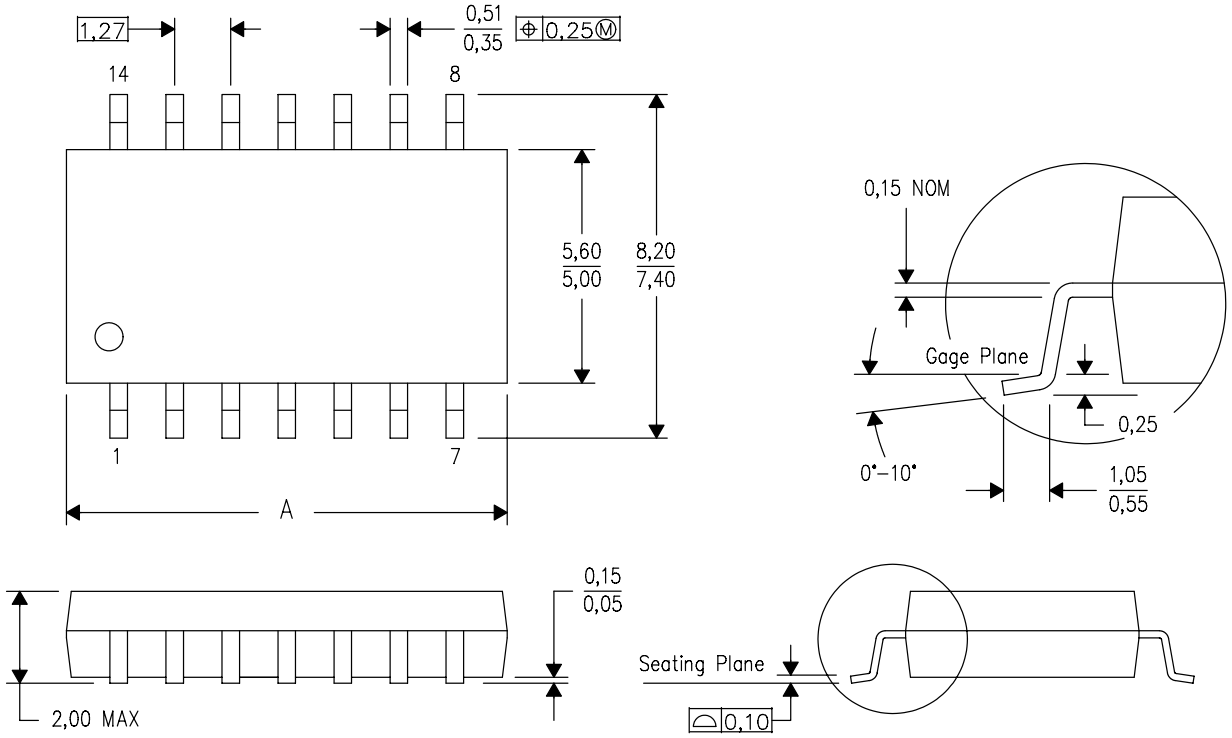


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

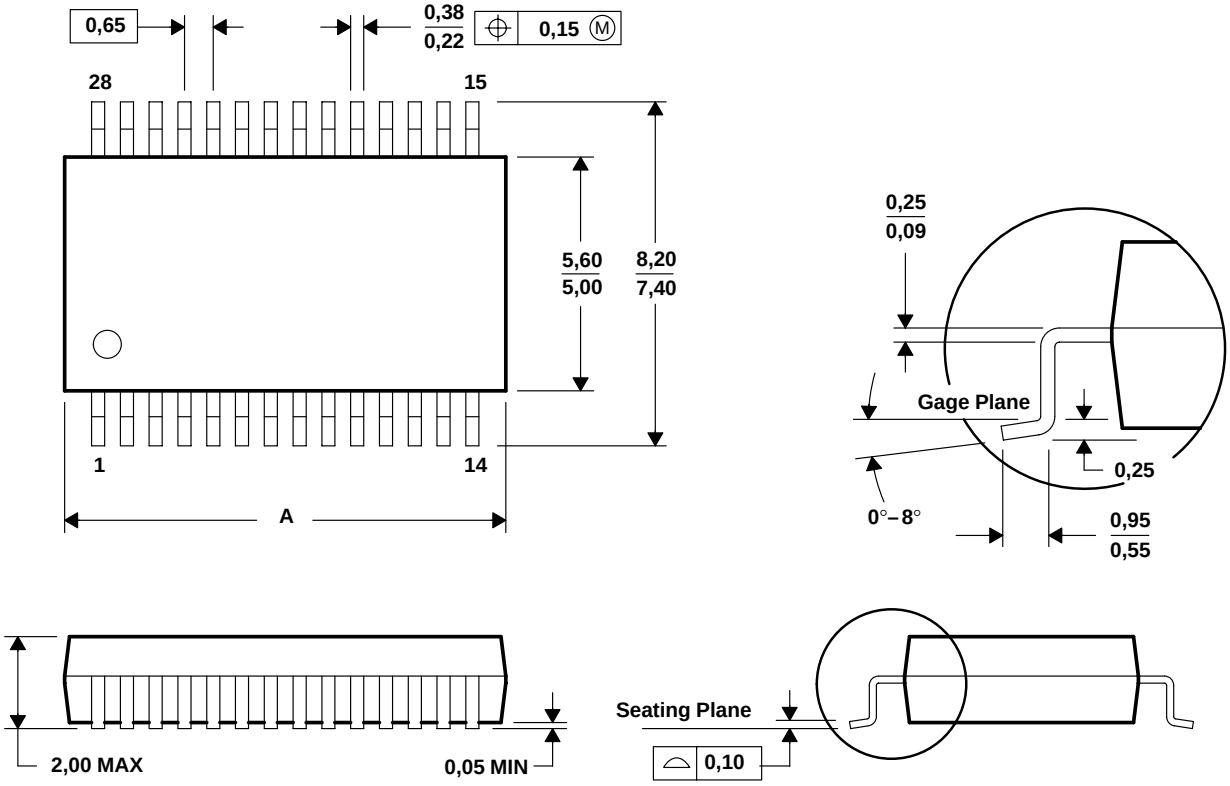
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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