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SN5414, SN54LS14,
SN7414, SN74LS14
HEX SCHMITT-TRIGGER INVERTERS

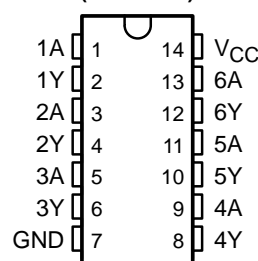SDLS049B – DECEMBER 1983 – REVISED FEBRUARY 2002

- ● **Operation From Very Slow Edges**
- ● **Improved Line-Receiving Characteristics**
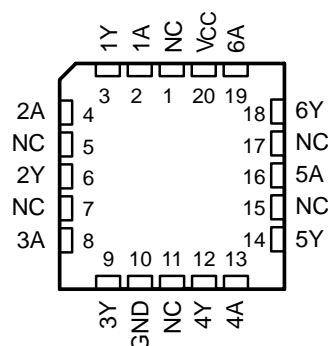- ● **High Noise Immunity**

description

Each circuit functions as an inverter, but because of the Schmitt action, it has different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

SN5414, SN54LS14 . . . J OR W PACKAGE
SN7414 . . . D, N, OR NS PACKAGE
SN74LS14 . . . D, DB, OR N PACKAGE
(TOP VIEW)

1A	1	14	V_{CC}
1Y	2	13	6A
2A	3	12	6Y
2Y	4	11	5A
3A	5	10	5Y
3Y	6	9	4A
GND	7	8	4Y

SN54LS14 . . . FK PACKAGE
(TOP VIEW)

Top pins: 1Y, 1A, NC, VCC, 6A (pins 3, 2, 1, 20, 19)

2A	4	18	6Y
NC	5	17	NC
2Y	6	16	5A
NC	7	15	NC
3A	8	14	5Y

Bottom pins: 3Y, GND, NC, 4Y, 4A (pins 9, 10, 11, 12, 13)

NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN7414N	SN7414N
		Tube	SN74LS14N	SN74LS14N
	SOIC – D	Tube	SN7414D	7414
		Tape and reel	SN7414DR	
		Tube	SN74LS14D	LS14
		Tape and reel	SN74LS14DR	
	SOP – NS	Tape and reel	SN7414NSR	SN7414
	SSOP – DB	Tape and reel	SN74LS14DBR	LS14
−55°C to 125°C	CDIP – J	Tube	SN5414J	SN5414J
		Tube	SNJ5414J	SNJ5414J
		Tube	SN54LS14J	SN54LS14J
		Tube	SNJ54LS14J	SNJ54LS14J
	CFP – W	Tube	SNJ5414W	SNJ5414W
		Tube	SNJ54LS14W	SNJ54LS14W
	LCCC – FK	Tube	SNJ54LS14FK	SNJ54LS14FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

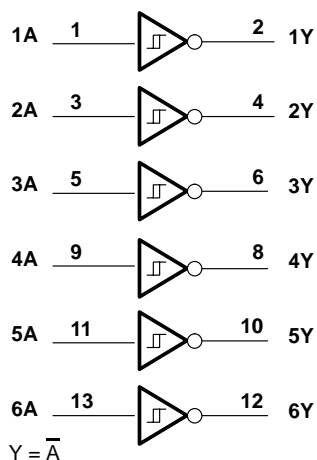POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

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SN5414, SN54LS14,
SN7414, SN74LS14
HEX SCHMITT-TRIGGER INVERTERS
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logic diagram (positive logic)

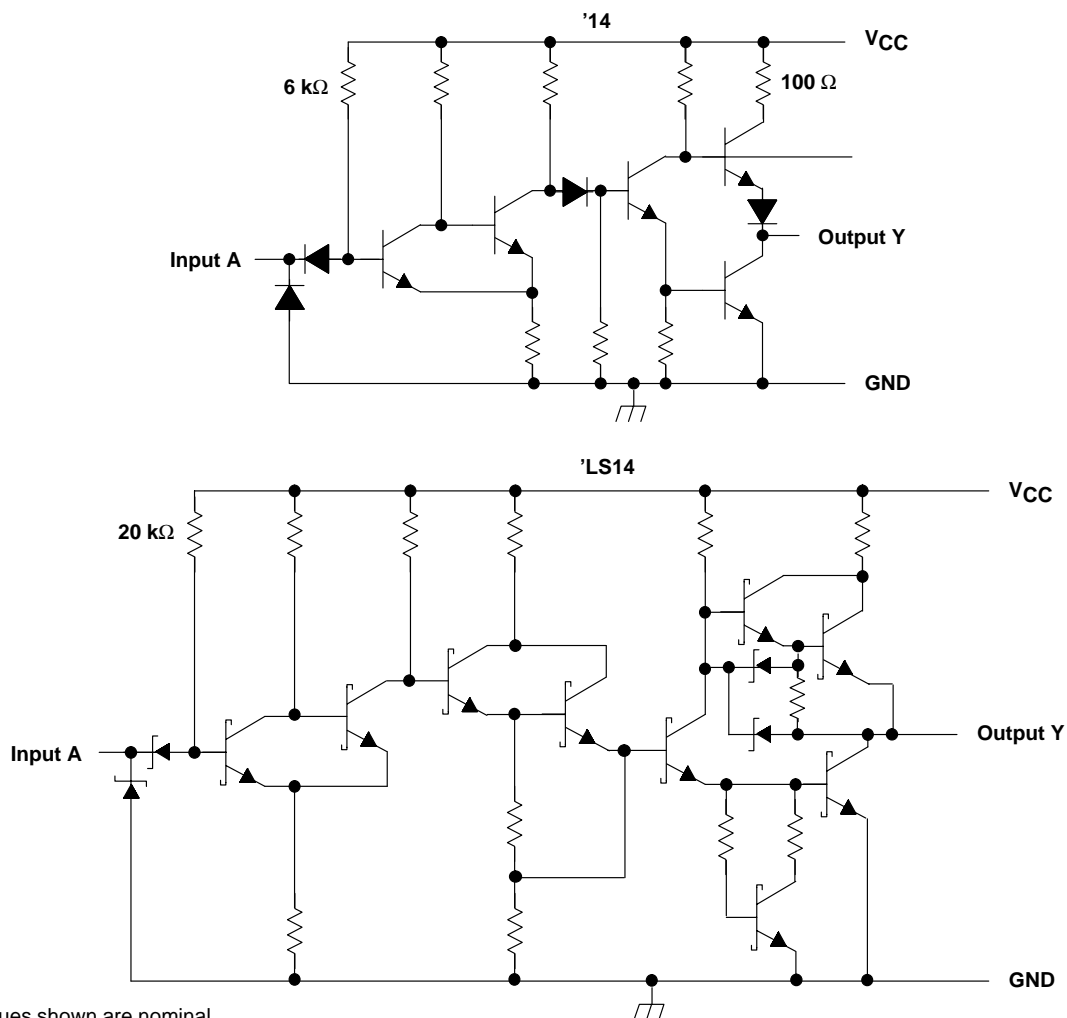|		
1A	1	2	1Y
2A	3	4	2Y
3A	5	6	3Y
4A	9	8	4Y
5A	11	10	5Y
6A	13	12	6Y

$Y = \overline{A}$

Pin numbers shown are for the D, DB, J, N, NS, and W packages.

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schematic

Resistor values shown are nominal.

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage: '14 . . . . 5.5 V
'LS14 . . . . 7 V
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . 86°C/W
DB package . . . . 96°C/W
N package . . . . 80°C/W
NS package . . . . 76°C/W
Storage temperaturerange, T_{stg} . . . . –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package termal impedance is calculated in accordance with JESD 51-7

recommended operating conditions

		SN5414			SN7414			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			–0.8			–0.8	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS[‡]			SN5414 SN7414			UNIT
				MIN	TYP[§]	MAX	
V_{T+}	$V_{CC} = 5$ V			1.5	1.7	2	V
V_{T-}	$V_{CC} = 5$ V			0.6	0.9	1.1	V
Hysteresis $(V_{T+} - V_{T-})$	$V_{CC} = 5$ V			0.4	0.8		V
V_{IK}	$V_{CC} = $ MIN,	$I_I = -12$ mA				–1.5	V
V_{OH}	$V_{CC} = $ MIN,	$V_I = 0.6$ V,	$I_{OH} = -0.8$ mA	2.4	3.4		V
V_{OL}	$V_{CC} = $ MIN,	$V_I = 2$ V,	$I_{OL} = 16$ mA		0.2	0.4	V
I_{T+}	$V_{CC} = 5$ V,	$V_I = V_{T+}$			–0.43		mA
I_{T-}	$V_{CC} = 5$ V,	$V_I = V_{T-}$			–0.56		mA
I_I	$V_{CC} = $ MAX,	$V_I = 5.5$ V				1	mA
I_{IH}	$V_{CC} = $ MAX,	$V_{IH} = 2.4$ V				40	µA
I_{IL}	$V_{CC} = $ MAX,	$V_{IL} = 0.4$ V			–0.8	–1.2	mA
I_{OS}[¶]	$V_{CC} = $ MAX			–18		–55	mA
I_{CCH}	$V_{CC} = $ MAX				22	36	mA
I_{CCL}	$V_{CC} = $ MAX				39	60	mA

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[§] All typical values are at $V_{CC} = 5$ V, $T_A = 25$°C.
[¶] Not more than one output should be shorted at a time.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN5414 SN7414			UNIT
				MIN	TYP	MAX	
t_{PLH}	A	Y	R_L = 400 Ω, C_L = 15 pF		15	22	ns
t_{PHL}					15	22	

recommended operating conditions

		SN54LS14			SN74LS14			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS[†]		SN54LS14			SN74LS14			UNIT
			MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{T+}	V_{CC} = 5 V		1.4	1.6	1.9	1.4	1.6	1.9	V
V_{T-}	V_{CC} = 5 V		0.5	0.8	1	0.5	0.8	1	V
Hysteresis $(V_{T+} - V_{T-})$	V_{CC} = 5 V		0.4	0.8		0.4	0.8		V
V_{IK}	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_I = 0.5 V, I_{OH} = −0.4 mA		2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN, V_I = −1.9 V	I_{OL}= 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.35	0.5	
I_{T+}	V_{CC} = 5 V, V_I = V_{T+}			−0.14			−0.14		mA
I_{T-}	V_{CC} = 5 V, V_I = V_{T-}			−0.18			−0.18		mA
I_I	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX, V_{IH} = 2.7 V				20			20	µA
I_{IL}	V_{CC} = MAX, V_{IL} = 0.4 V				−0.4			−0.4	mA
I_{OS}[§]	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX			8.6	16		8.6	16	mA
I_{CCL}	V_{CC} = MAX			12	21		12	21	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	R_L = 2 kΩ, C_L = 15 pF		15	22	ns
t_{PHL}					15	22	

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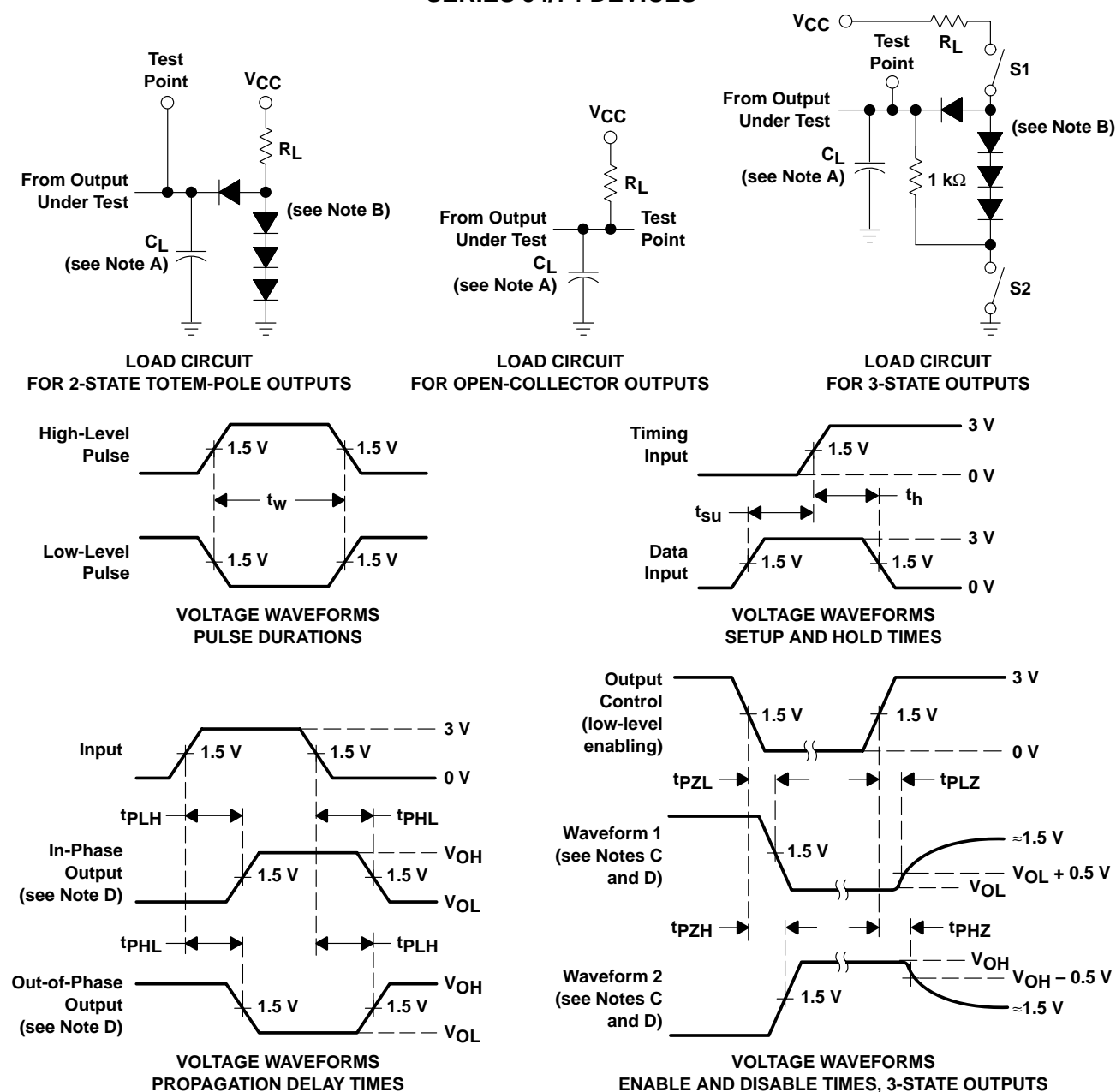POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

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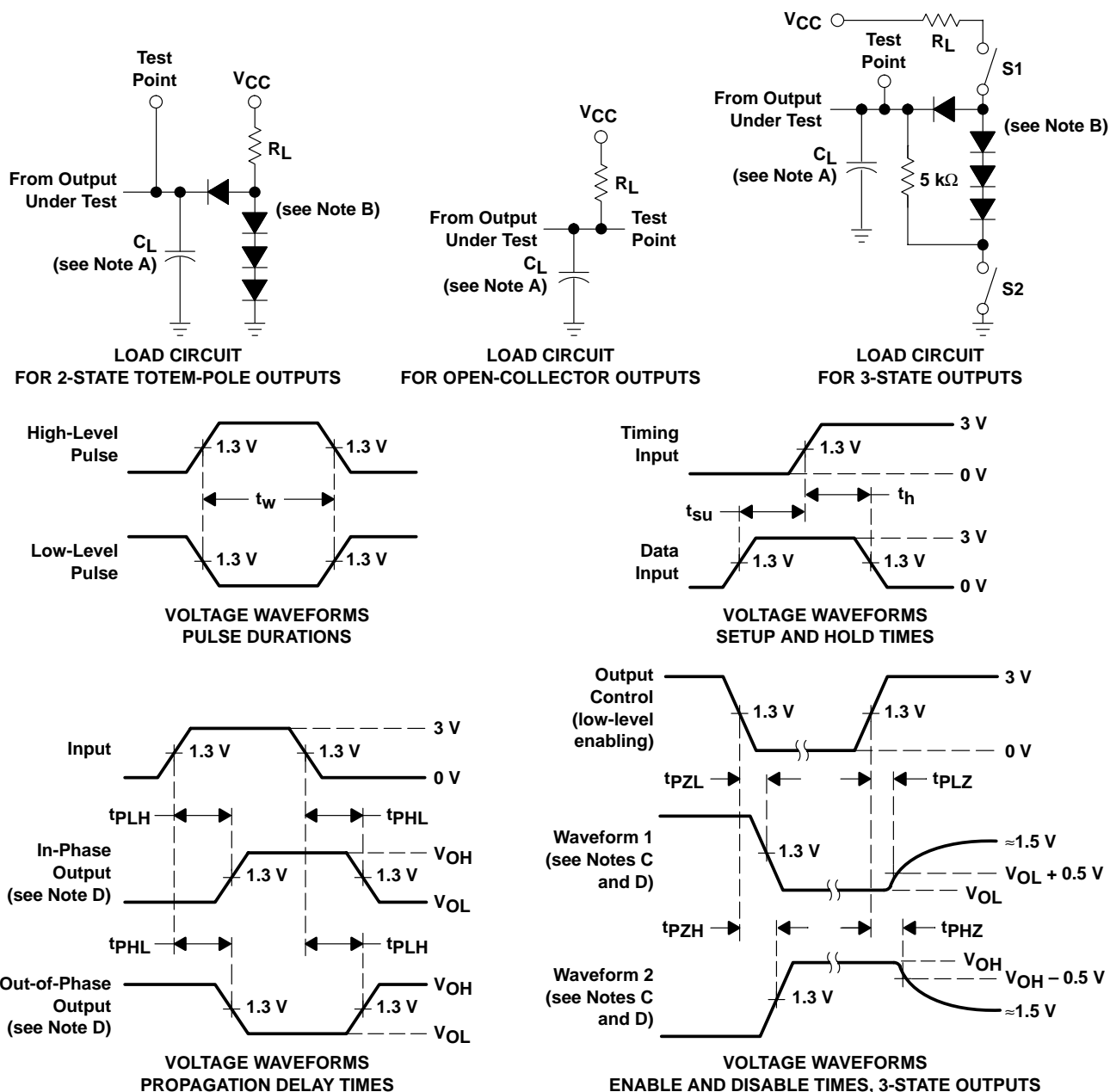## PARAMETER MEASUREMENT INFORMATION
SERIES 54/74 DEVICES

**LOAD CIRCUIT
FOR 2-STATE TOTEM-POLE OUTPUTS**

**LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS**

**LOAD CIRCUIT
FOR 3-STATE OUTPUTS**

**VOLTAGE WAVEFORMS
PULSE DURATIONS**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω; t_r and t_f ≤ 7 ns for Series
   54/74 devices and t_r and t_f ≤ 2.5 ns for Series 54S/74S devices.
F. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES

LOAD CIRCUIT
FOR 2-STATE TOTEM-POLE OUTPUTS

LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS

LOAD CIRCUIT
FOR 3-STATE OUTPUTS

VOLTAGE WAVEFORMS
PULSE DURATIONS

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω, t_r ≤ 1.5 ns, t_f ≤ 2.6 ns.
G. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

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TYPICAL CHARACTERISTICS OF '14 CIRCUITS†

POSITIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE
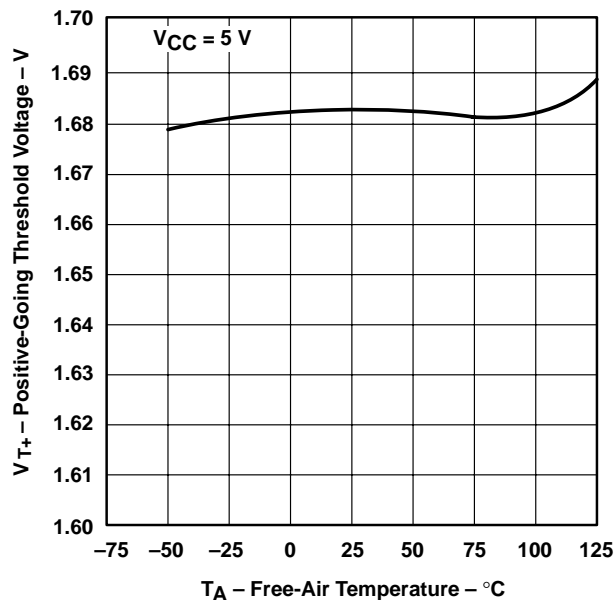
Figure 3

NEGATIVE-GOING THRESHOLD VOLTAGE
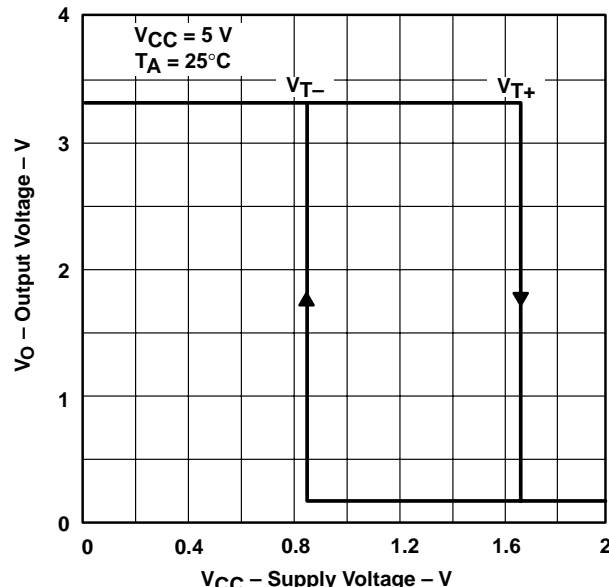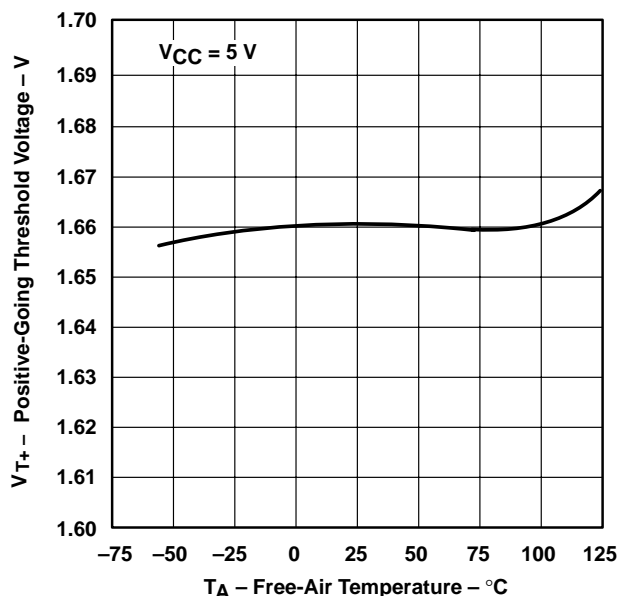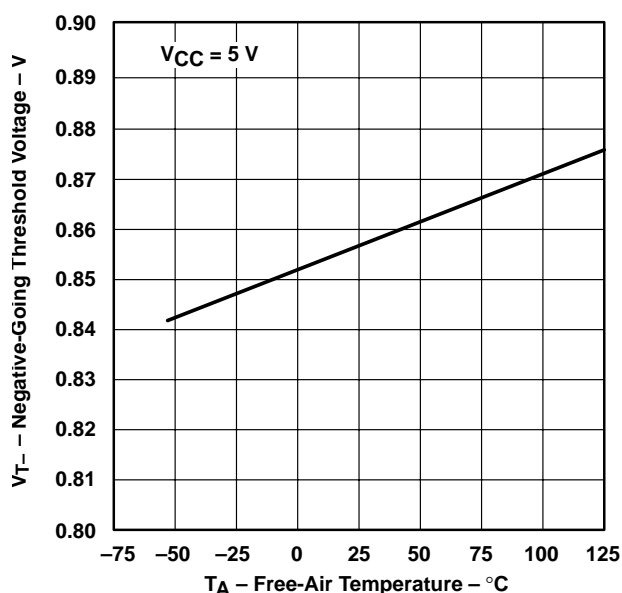vs
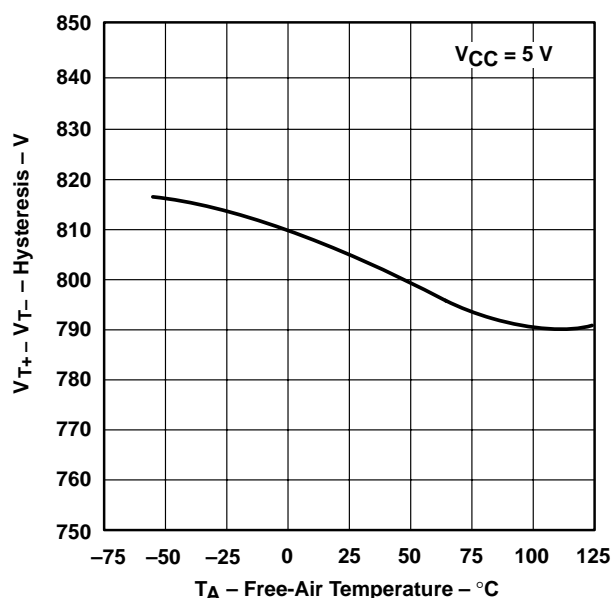FREE-AIR TEMPERATURE
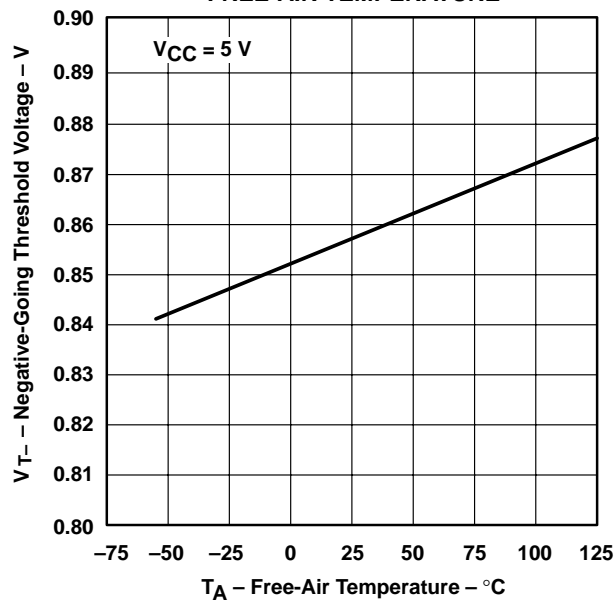
Figure 4

HYSTERESIS
vs
FREE-AIR TEMPERATURE
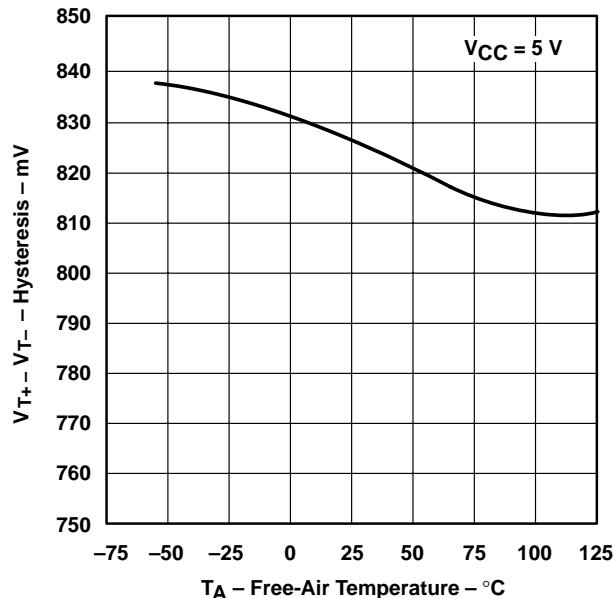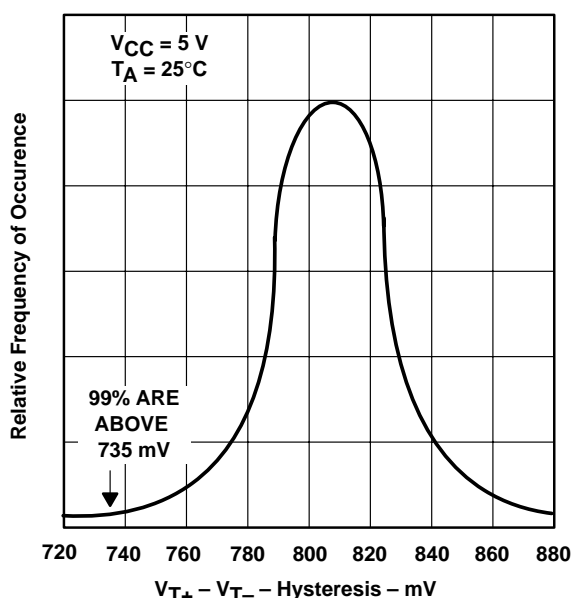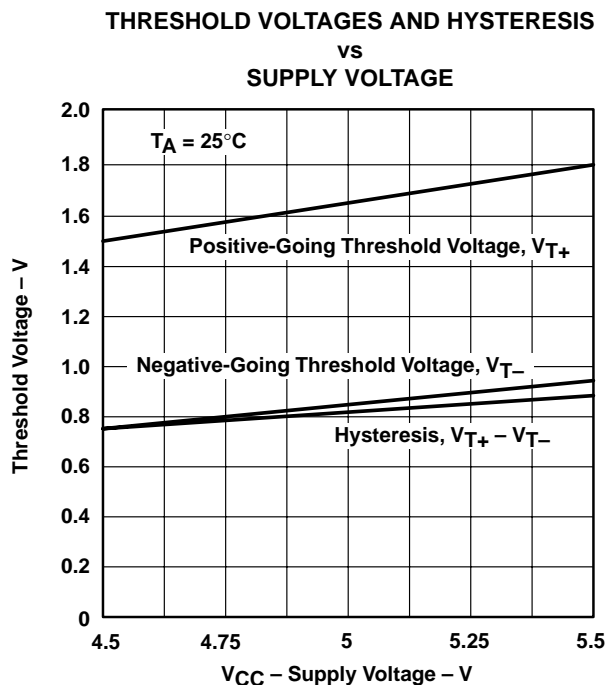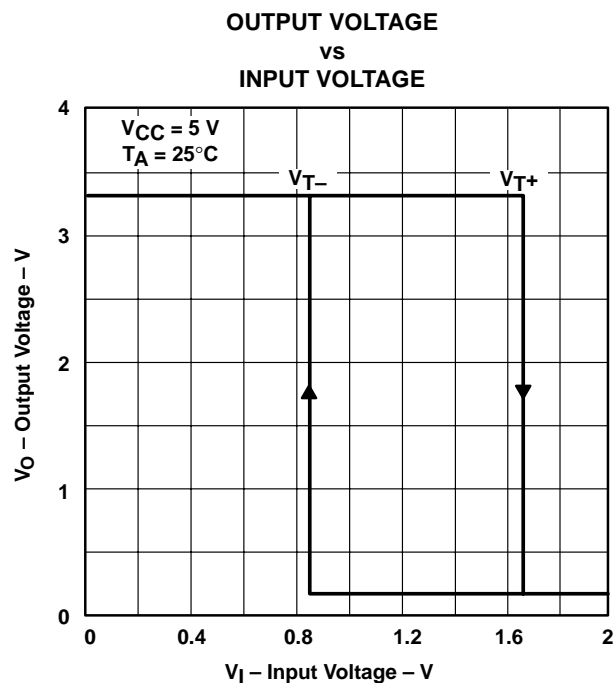
Figure 5

† Data for temperatures below 0°C and above 70°C and supply voltage below 4.75 V and above 5.25 V are applicable for SN5414 only.

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TYPICAL CHARACTERISTICS OF '14 CIRCUITS†

DISTRIBUTION OF UNITS
FOR HYSTERESIS

V_{CC} = 5 V
T_A = 25°C

Relative Frequency of Occurence

$V_{T+} - V_{T-}$ – Hysteresis – mV
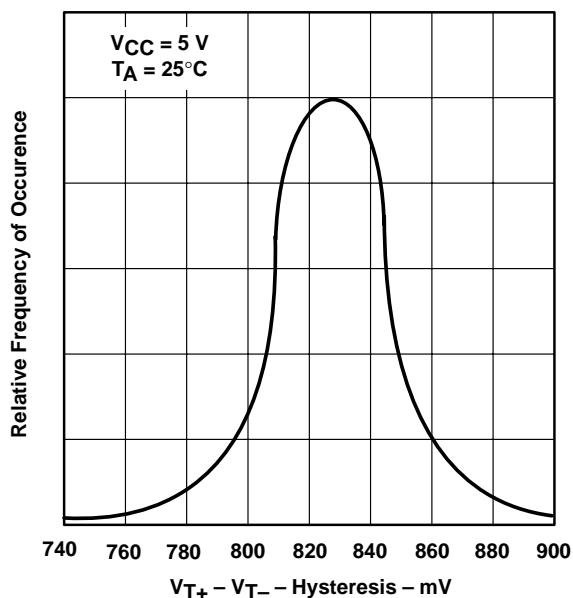
Figure 6

THRESHOLD VOLTAGES
vs
SUPPLY VOLTAGE

T_A = 25°C

Threshold Voltage — V

Positive-Going Threshold Voltage, V_{T+}

Negative-Going Threshold Voltage, V_{T-}

$V_{T+} - V_{T-}$ – Hysteresis – mV
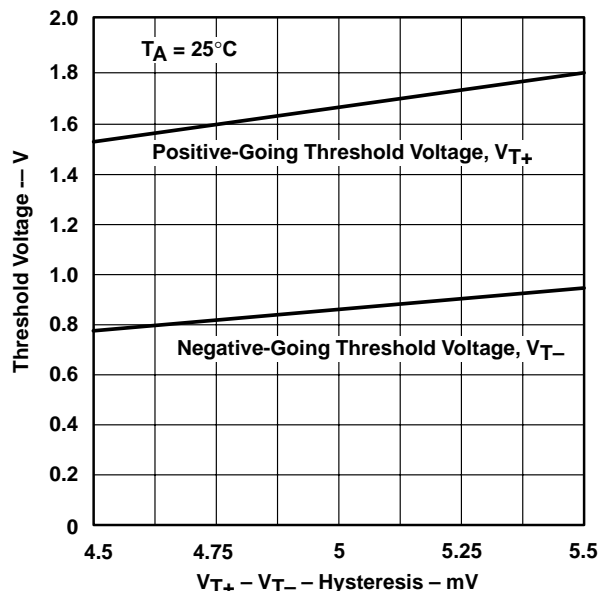
Figure 7

HYSTERESIS
vs
SUPPLY VOLTAGE

T_A = 25°C

$V_{T+} - V_{T-}$ – Hysteresis – V

V_{CC} – Supply Voltage – V
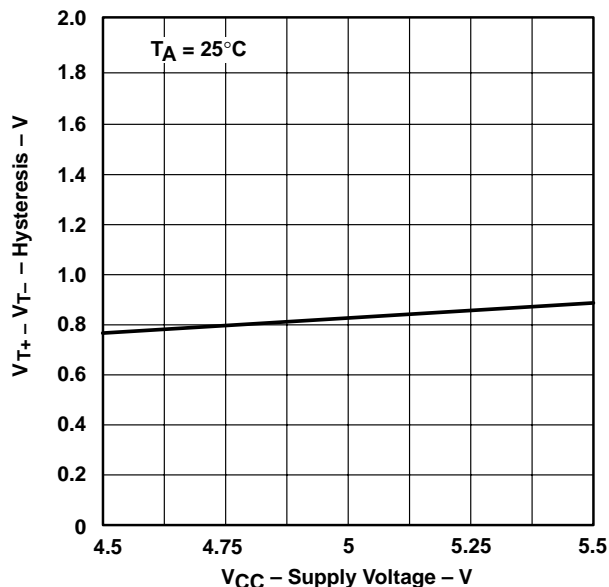
Figure 8

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

V_{CC} = 5 V
T_A = 25°C

V_{T-} V_{T+}

V_O – Output Voltage – V

V_{CC} – Supply Voltage – V

Figure 9

† Data for temperatures below 0°C and above 70°C and supply voltage below 4.75 V and above 5.25 V are applicable for SN5414 only.

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## TYPICAL CHARACTERISTICS OF 'LS14 CIRCUITS†

POSITIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 10

NEGATIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 11

HYSTERESIS
vs
FREE-AIR TEMPERATURE

Figure 12

DISTRIBUTION OF UNITS
FOR HYSTERESIS

Figure 13

† Data for temperatures below 0°C and above 70°C and supply voltage below 4.75 V and above 5.25 V are applicable for SN5414 only.

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TYPICAL CHARACTERISTICS OF 'LS14 CIRCUITS†

THRESHOLD VOLTAGES AND HYSTERESIS
vs
SUPPLY VOLTAGE

Figure 14

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

Figure 15

† Data for temperatures below 0°C and above 70°C and supply voltage below 4.75 V and above 5.25 V are applicable for SN5414 only.

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SN5414, SN54LS14,
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TYPICAL APPLICATION DATA
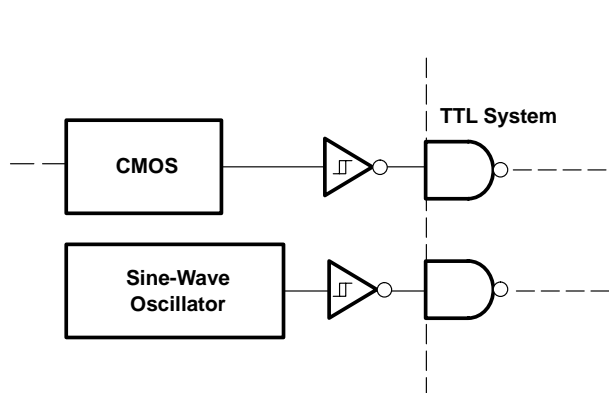
TTL System Interface
for Slow Input Waveforms

Pulse Shaper

0.1 Hz to 10 MHz

330 Ω
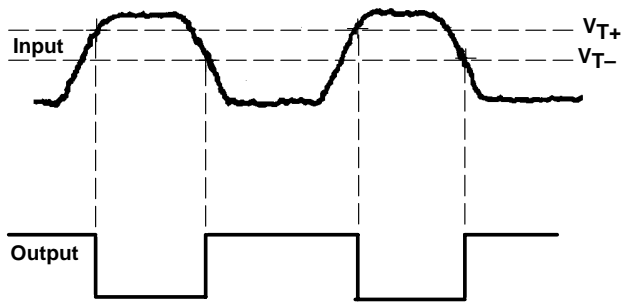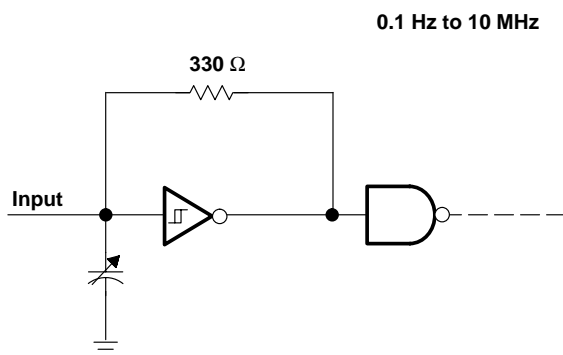
Multivibrator
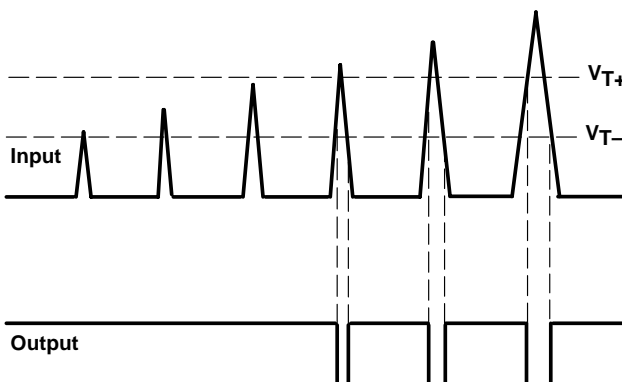
Threshold Detector

Open-Collector Output

Pulse Stretcher

PACKAGE OPTION ADDENDUM

www.ti.com   17-Dec-2015
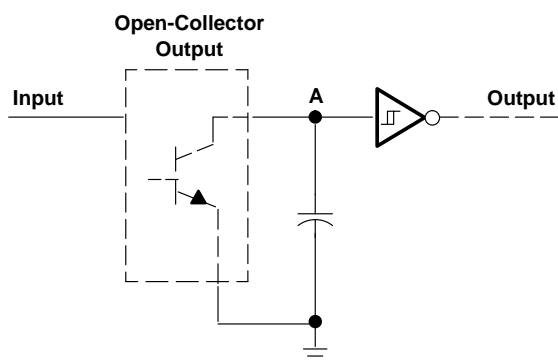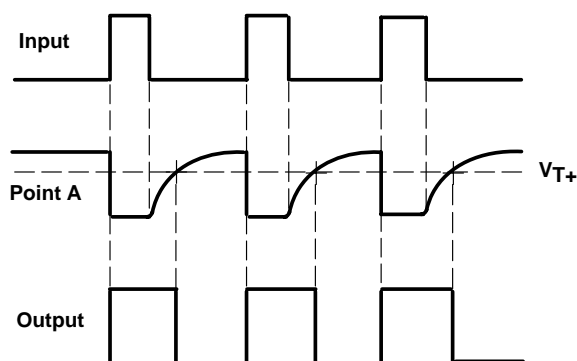
PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9665801Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9665801Q2A SNJ54LS 14FK	Samples
5962-9665801QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9665801QC A SNJ54LS14J	Samples
5962-9665801QDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9665801QD A SNJ54LS14W	Samples
5962-9665801VDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9665801VD A SNV54LS14W	Samples
JM38510/31302BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 31302BCA	Samples
M38510/31302BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 31302BCA	Samples
SN5414J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN5414J	Samples
SN54LS14J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS14J	Samples
SN7414D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7414	Samples
SN7414DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7414	Samples
SN7414DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7414	Samples
SN7414N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN7414N	Samples
SN7414N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN7414NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN7414N	Samples
SN7414NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN7414	Samples
SN74LS14D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS14	Samples

PACKAGE OPTION ADDENDUM

www.ti.com
17-Dec-2015

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS14DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS14	Samples
SN74LS14DBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS14	Samples
SN74LS14DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS14	Samples
SN74LS14DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS14	Samples
SN74LS14DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS14	Samples
SN74LS14DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS14	Samples
SN74LS14DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS14	Samples
SN74LS14N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS14N	Samples
SN74LS14N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74LS14NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS14N	Samples
SN74LS14NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS14	Samples
SNJ5414J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ5414J	Samples
SNJ5414W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ5414W	Samples
SNJ54LS14FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9665801Q2A SNJ54LS 14FK	Samples
SNJ54LS14J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9665801QC A SNJ54LS14J	Samples
SNJ54LS14W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9665801QD A SNJ54LS14W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

Addendum-Page 2

PACKAGE OPTION ADDENDUM

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LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN5414, SN54LS14, SN54LS14-SP, SN7414, SN74LS14 :

● Catalog: SN7414, SN74LS14, SN54LS14

● Military: SN5414, SN54LS14

● Space: SN54LS14-SP

PACKAGE OPTION ADDENDUM

www.ti.com   17-Dec-2015
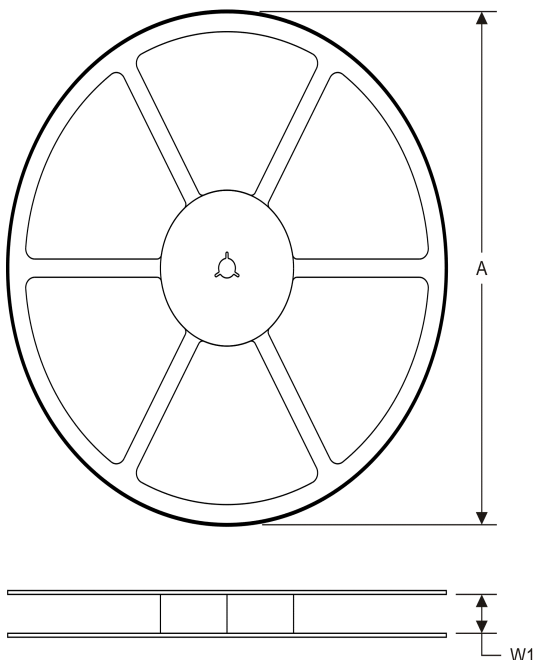
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

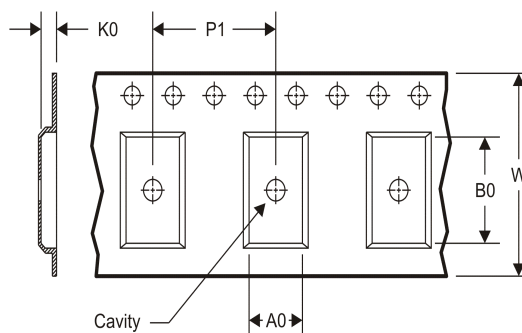- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TEXAS INSTRUMENTS

PACKAGE MATERIALS INFORMATION

www.ti.com

14-Jul-2012

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN7414DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN7414NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LS14DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LS14DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS14NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TEXAS INSTRUMENTS

PACKAGE MATERIALS INFORMATION

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14-Jul-2012

TAPE AND REEL BOX DIMENSIONS
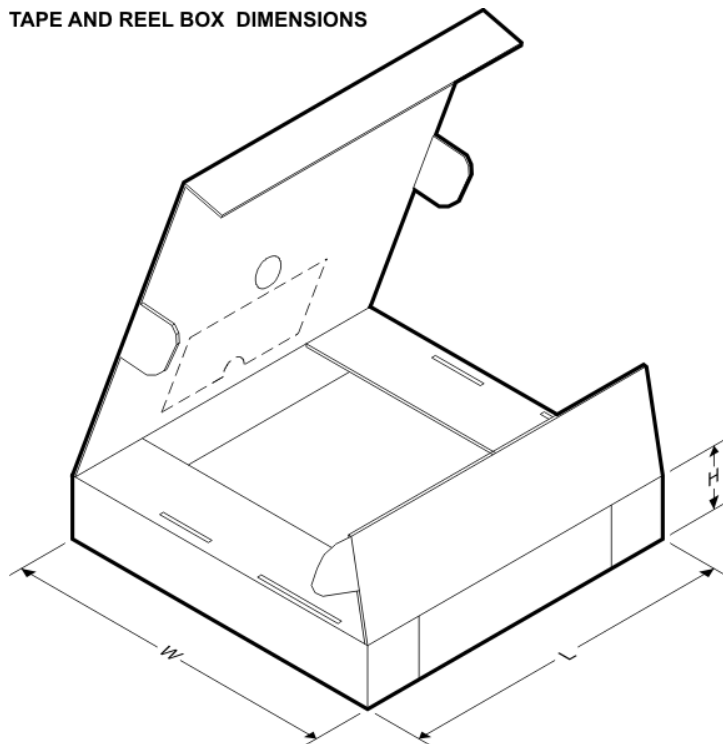
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN7414DR	SOIC	D	14	2500	367.0	367.0	38.0
SN7414NSR	SO	NS	14	2000	367.0	367.0	38.0
SN74LS14DBR	SSOP	DB	14	2000	367.0	367.0	38.0
SN74LS14DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74LS14NSR	SO	NS	14	2000	367.0	367.0	38.0

J (R−GDIP−T**)   CERAMIC DUAL IN−LINE PACKAGE

14 LEADS SHOWN
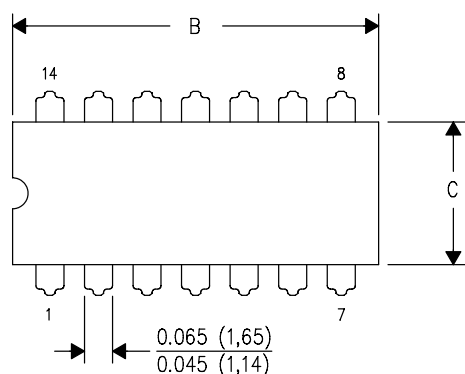
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

0°−15°

0.014 (0,36)
0.008 (0,20)
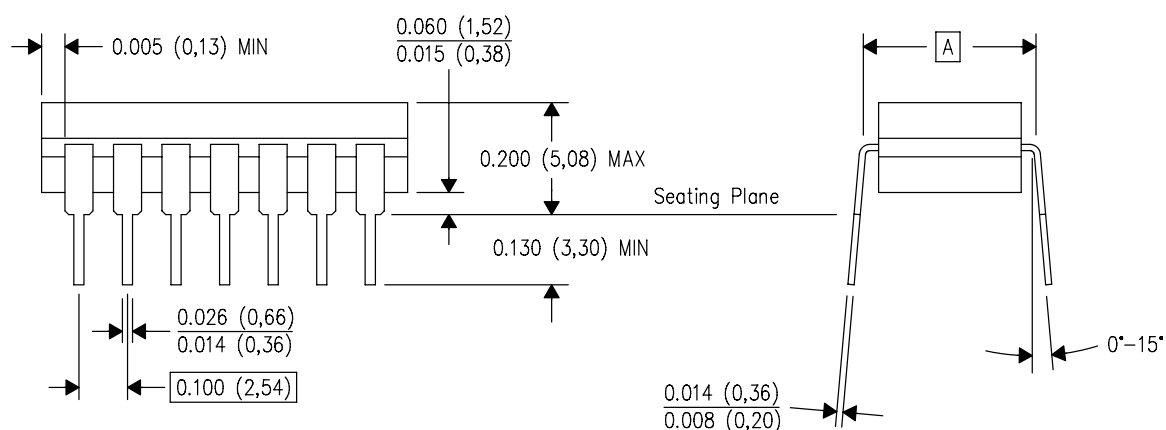
4040083/F 03/03
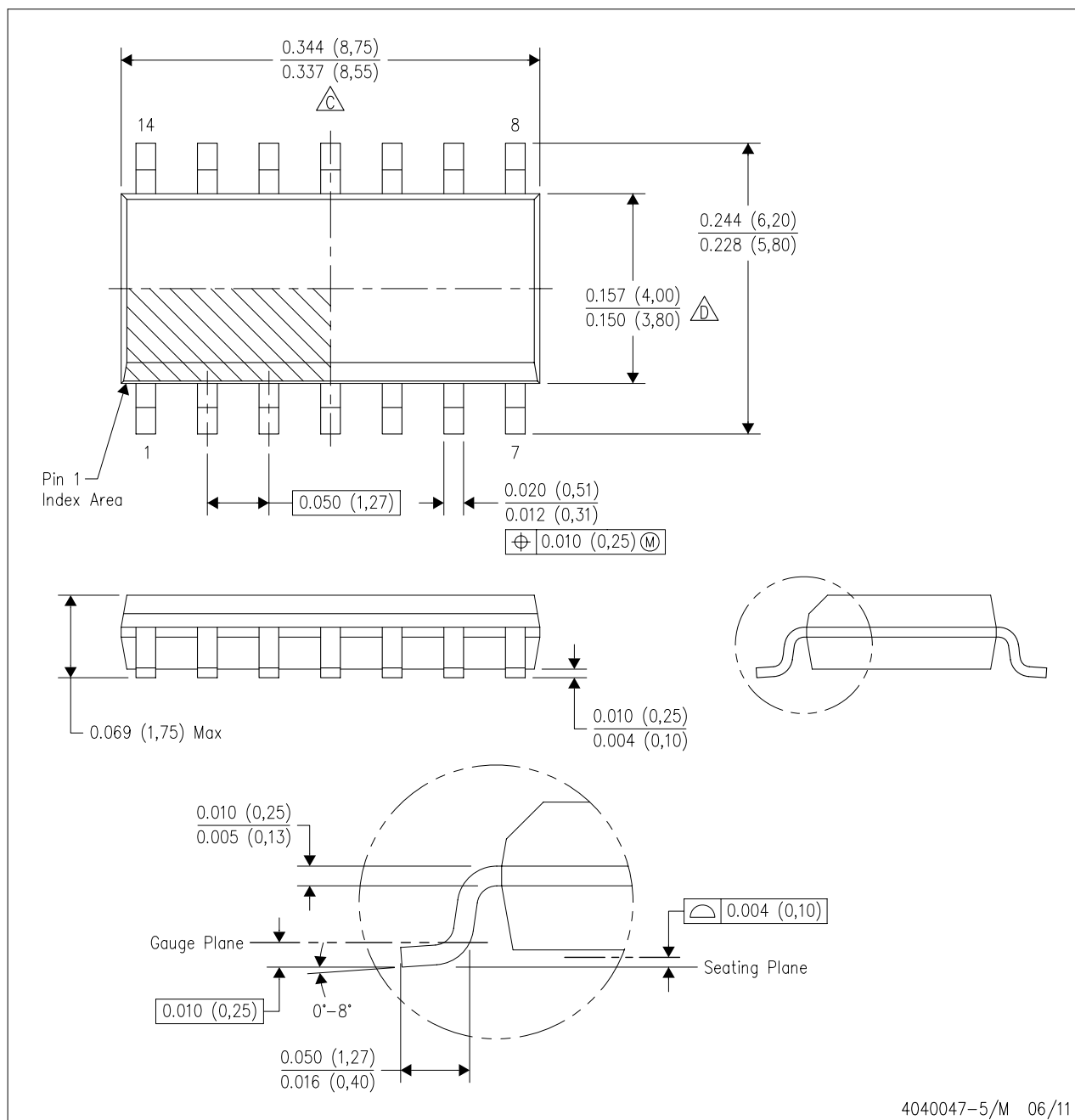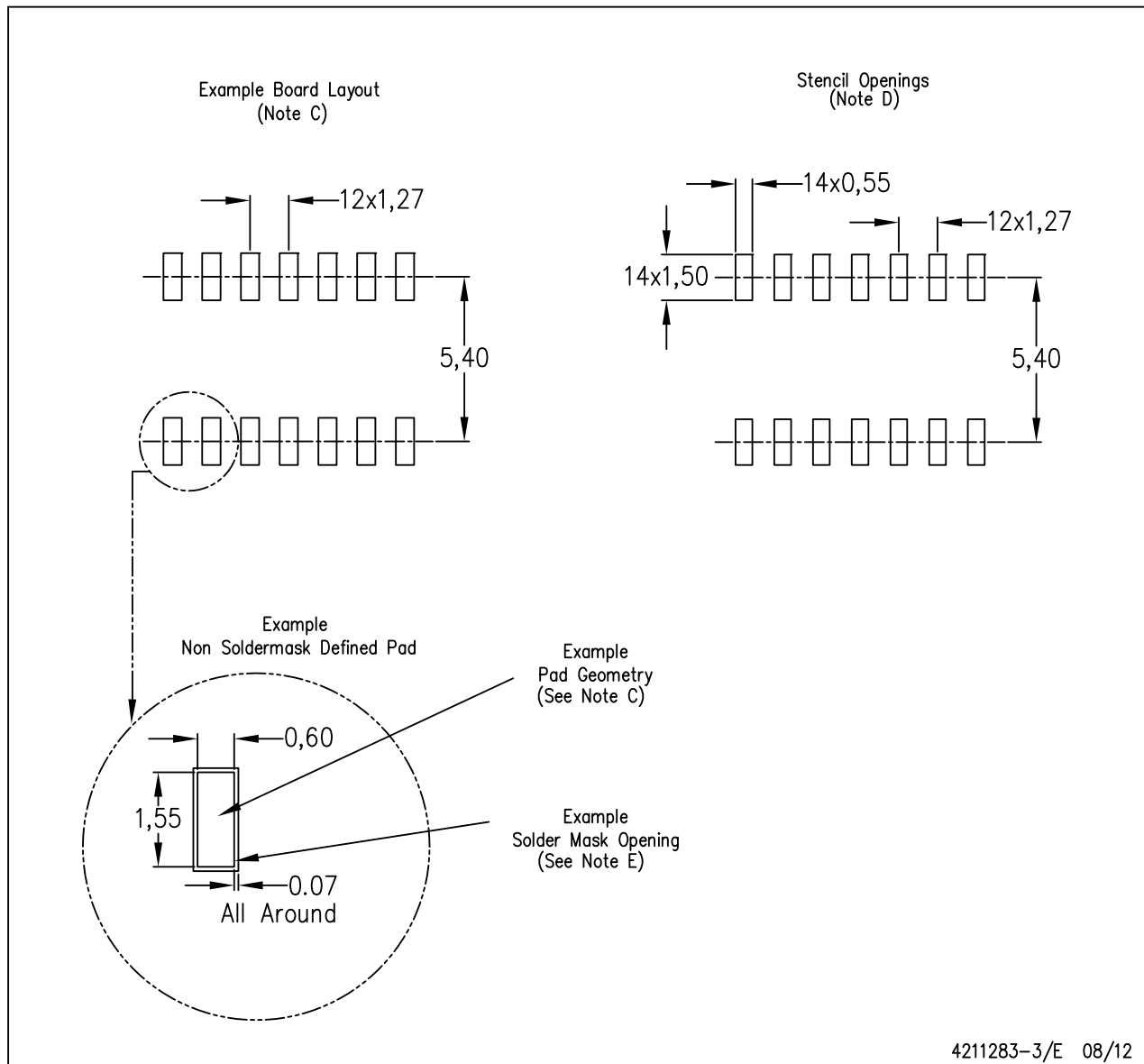
NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package is hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E.   Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

MECHANICAL DATA

W (R−GDFP−F14)   CERAMIC DUAL FLATPACK
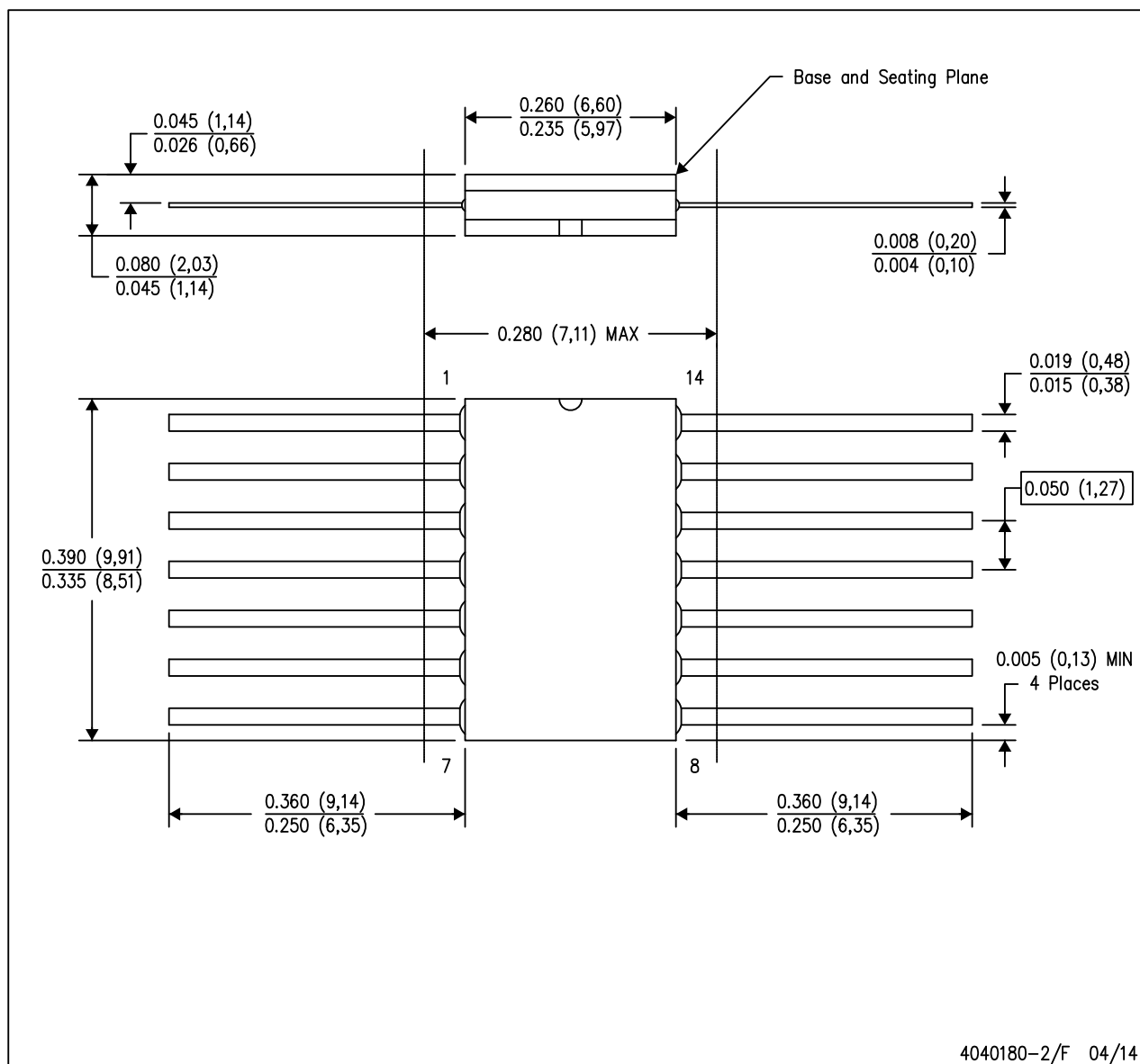
0.045 (1,14)
0.026 (0,66)

0.080 (2,03)
0.045 (1,14)

0.260 (6,60)
0.235 (5,97)

Base and Seating Plane

0.008 (0,20)
0.004 (0,10)

0.280 (7,11) MAX

1   14

0.019 (0,48)
0.015 (0,38)

0.050 (1,27)

0.390 (9,91)
0.335 (8,51)

0.005 (0,13) MIN
4 Places

7   8

0.360 (9,14)
0.250 (6,35)

0.360 (9,14)
0.250 (6,35)

4040180−2/F   04/14

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   This package can be hermetically sealed with a ceramic lid using glass frit.
          D.   Index point is provided on cap for terminal identification only.
          E.   Falls within MIL STD 1835 GDFP1−F14

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MECHANICAL DATA

FK (S−CQCC−N**)   LEADLESS CERAMIC CHIP CARRIER
28 TERMINAL SHOWN
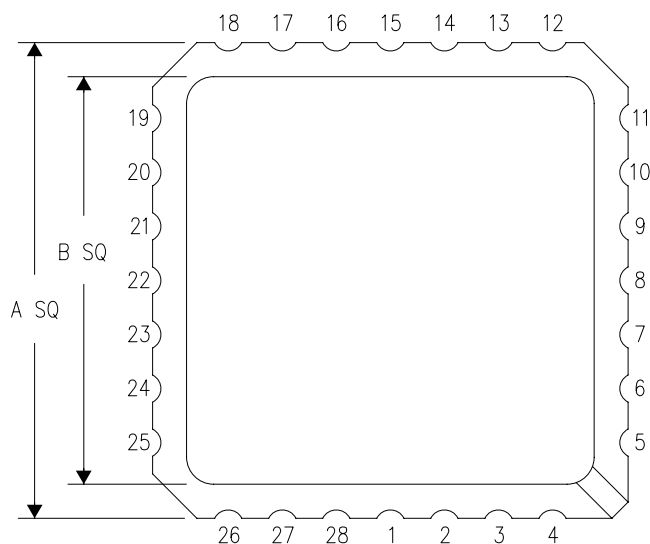
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)
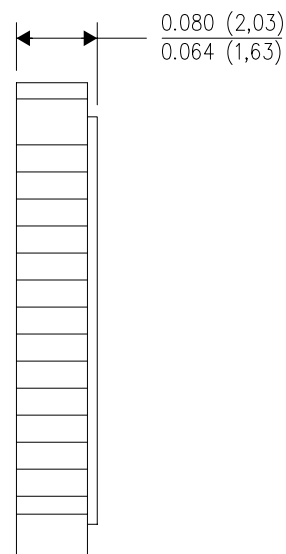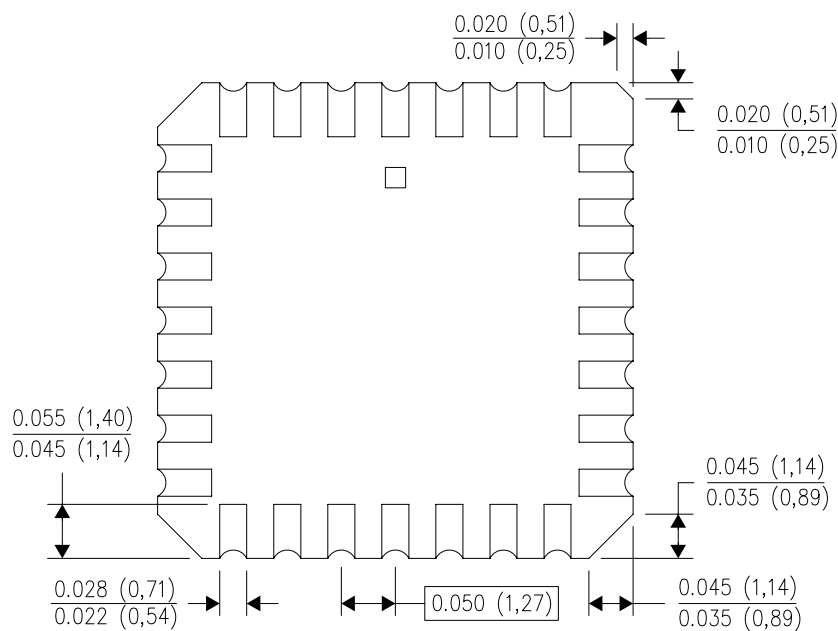
4040140/D 01/11

NOTES: A.   All linear dimensions are in inches (millimeters).
B.   This drawing is subject to change without notice.
C.   This package can be hermetically sealed with a metal lid.
D.   Falls within JEDEC MS−004

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MECHANICAL DATA

N (R-PDIP-T)**   PLASTIC DUAL-IN-LINE PACKAGE
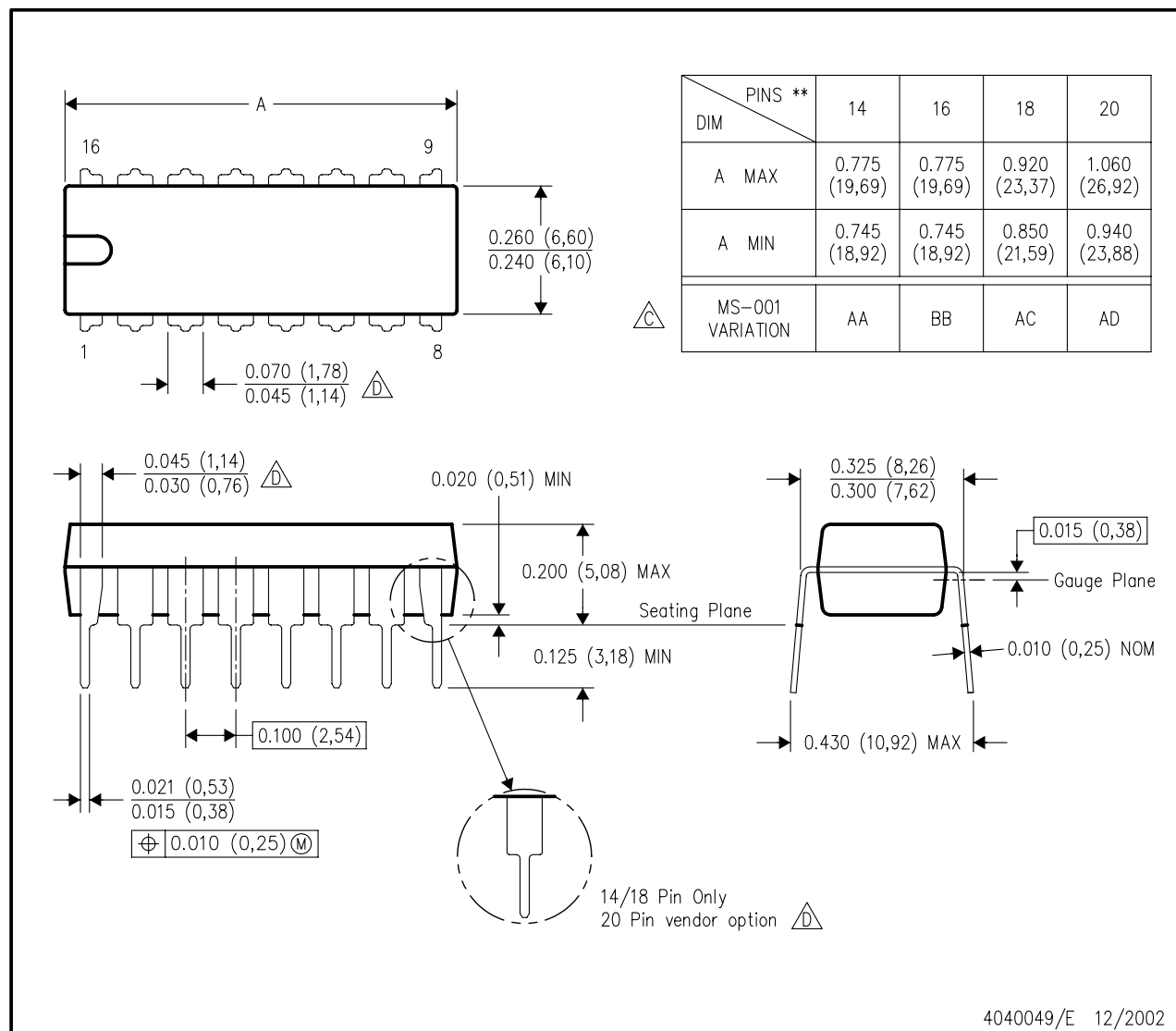
16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14) △D

0.045 (1,14)
0.030 (0,76) △D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option △D

4040049/E 12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
           B.   This drawing is subject to change without notice.
         △C   Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
         △D   The 20 pin end lead shoulder width is a vendor option, either half or full width.

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MECHANICAL DATA

D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

4040047−5/M   06/11

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
         D.   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E.   Reference JEDEC MS−012 variation AB.

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LAND PATTERN DATA

D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

12x1,27

14x0,55

14x1,50

12x1,27

5,40

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0.07
All Around

4211283−3/E   08/12

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Publication IPC−7351 is recommended for alternate designs.
          D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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MECHANICAL DATA

NS (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN
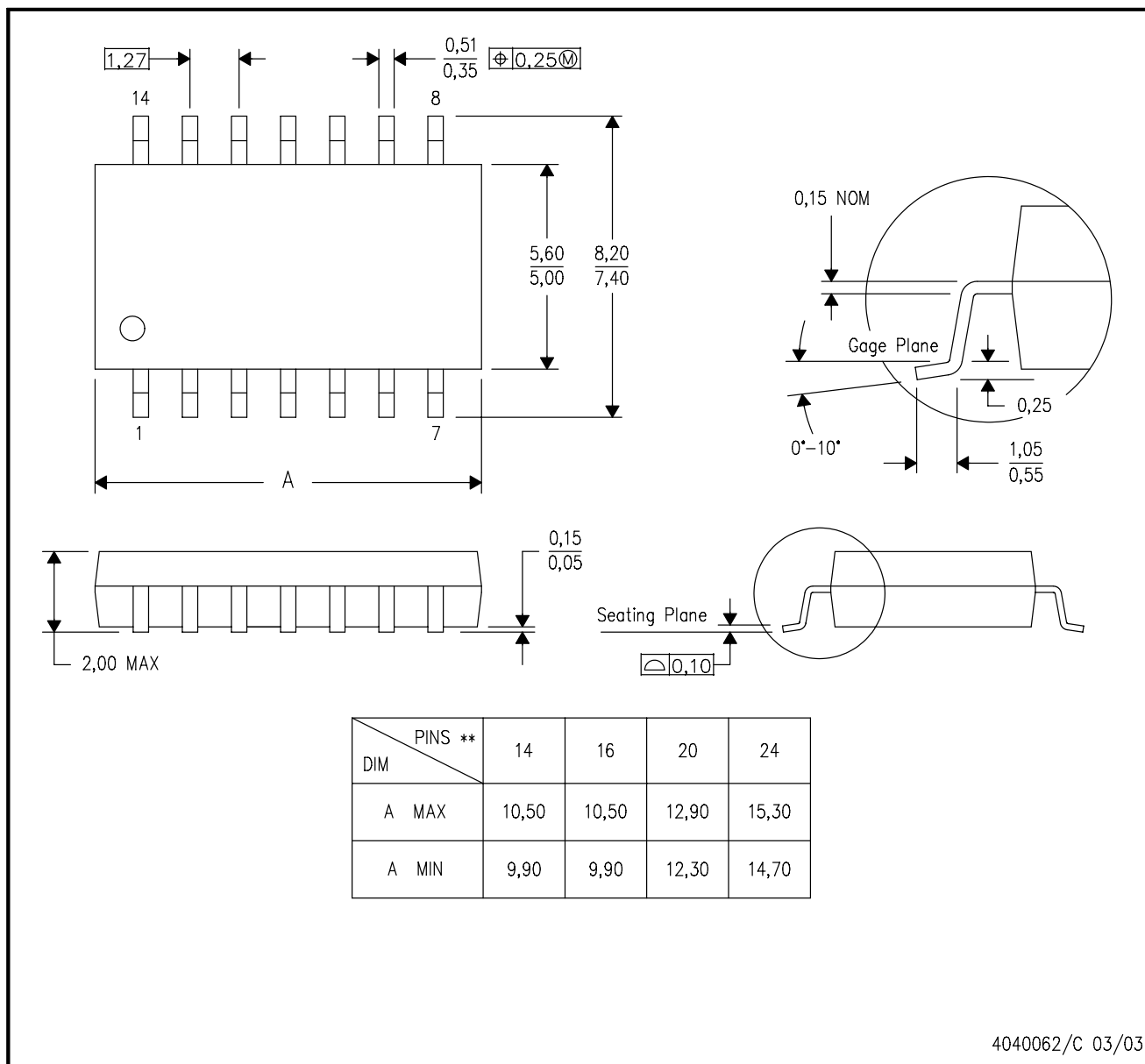
PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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MECHANICAL DATA

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G**)   PLASTIC SMALL-OUTLINE

28 PINS SHOWN
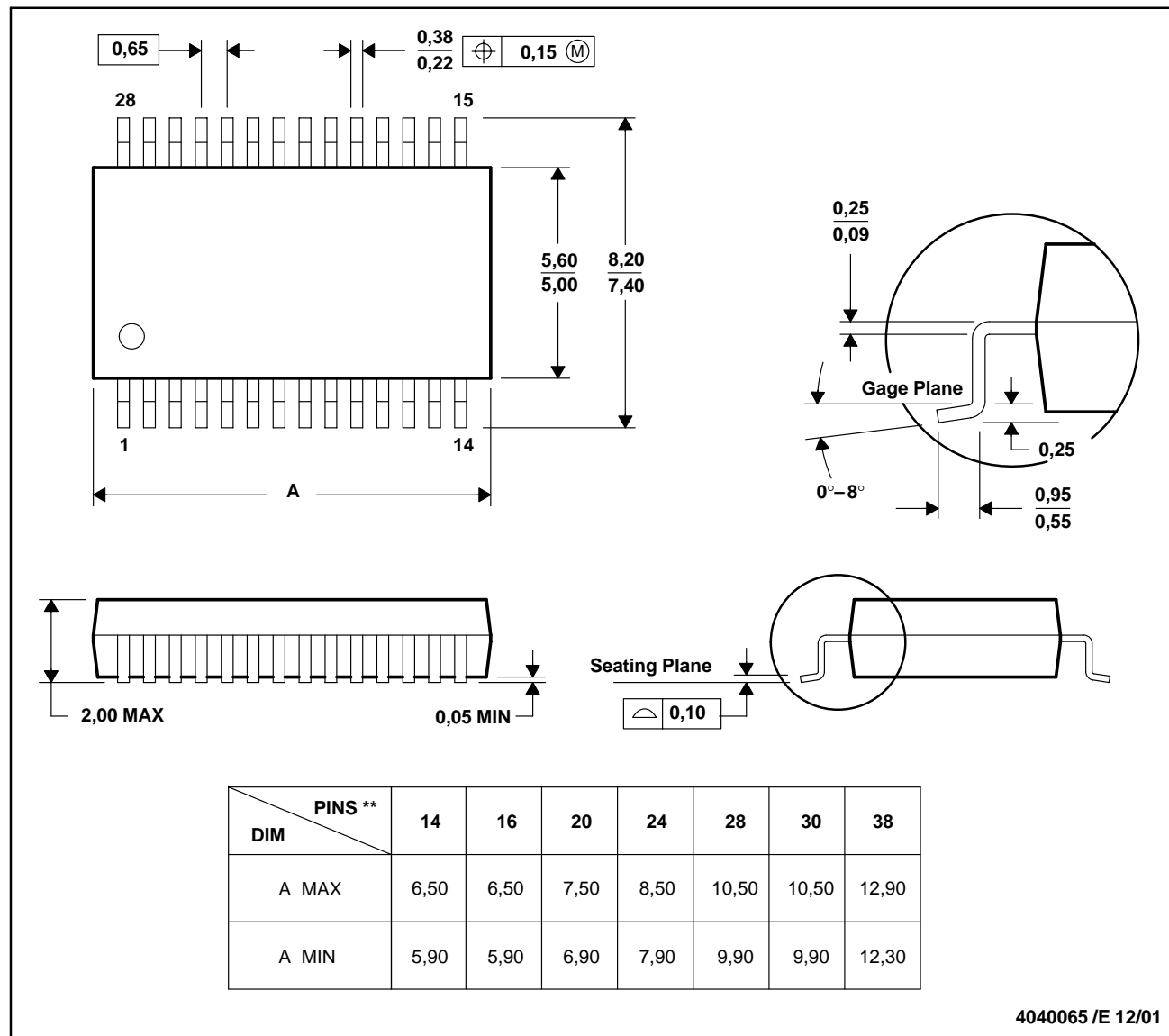
DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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