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**TEXAS INSTRUMENTS**

**SN74LV244A**

SCLS383N – SEPTEMBER 1997 – REVISED OCTOBER 2015

# SN74LV244A Octal Buffers and Drivers With 3-State Outputs

## 1 Features

- 2-V to 5.5-V $V_{CC}$ Operation
- Max $t_{pd}$ of 6.5 ns at 5 V
- Typical $V_{OLP}$ (Output Ground Bounce) <0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C
- Typical $V_{OHV}$ (Output $V_{OH}$ Undershoot) >2.3 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C
- Support Mixed-Mode Voltage Operation on All Ports
- $I_{off}$ Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250-mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## 2 Applications

- Servers and Network Switches
- LED Displays
- Telecom Infrastructure
- Motor-Drive Control Boards

## 3 Description

The SN74LV244A octal buffers and line drivers are designed for 2-V to 5.5-V $V_{CC}$ operation.

The SN74LV244A devices are designed specifically to improve both performance and density of the 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices are organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs.

**Device Information**

| PART NUMBER | PACKAGE (PIN) | BODY SIZE |
|---|---|---|
| SN74LV244ADGV | TVSOP (20) | 5.00 mm × 4.40 mm |
| SN74LV244ADW | SOIC (20) | 12.80 mm × 7.50 mm |
| SN74LV244ANS | SOP (20) | 12.60 mm × 5.30 mm |
| SN74LV244APW | TSSOP (20) | 6.50 mm × 4.40 mm |
| SN74LV244ARGY | VQFN (20) | 4.50 mm × 3.50 mm |

**Logic Diagram (Positive Logic)**
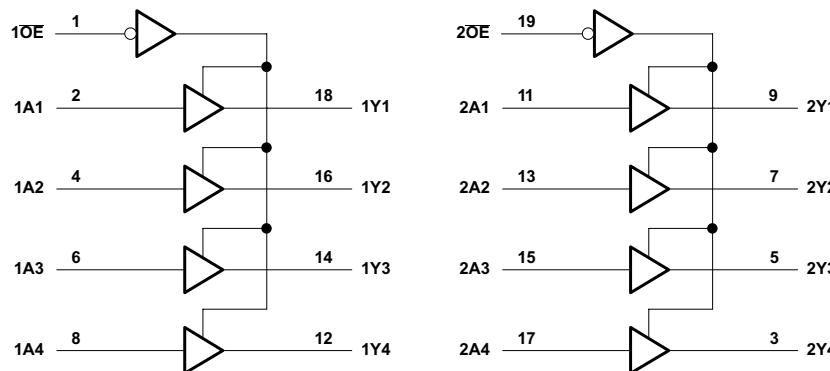
**TEXAS INSTRUMENTS**

**SN74LV244A**

SCLS383N – SEPTEMBER 1997 – REVISED OCTOBER 2015

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# Table of Contents

# 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision M (June 2013) to Revision N**     **Page**

- Added *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Detailed Description* section, *Applications and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ...... 1
- Deleted SN54LV244A part number from the data sheet ................................................................................................ 1
- Removed the $T_A$ = –40°C to 85°C test conditions with the same values as the $T_A$ = –40°C to 125°C Recommended test conditions in the *Electrical Characteristics* and *Switching Characteristics* tables .......................................... 6
- Removed the word 'Recommended' in the $T_A$ = –40°C to 125°C Recommended test conditions in the *Electrical Characteristics* and *Switching Characteristics* tables ................................................................................................ 6

**Changes from Revision L (August 2010) to Revision M**     **Page**

- Changed document format from Quicksilver to DocZone ................................................................................................ 1
- Changed Extended operating temperature range to 125°C ........................................................................................... 1

Product Folder Links: *SN74LV244A*

# 5  Pin Configuration and Functions

**DB, DGV, DW, NS, PW Package
20-Pin SSOP, TVSOP, SOIC, SO, TSSOP
Top View**

```
1OE  [ 1      20 ] V_CC
1A1  [ 2      19 ] 2OE
2Y4  [ 3      18 ] 1Y1
1A2  [ 4      17 ] 2A4
2Y3  [ 5      16 ] 1Y2
1A3  [ 6      15 ] 2A3
2Y2  [ 7      14 ] 1Y3
1A4  [ 8      13 ] 2A2
2Y1  [ 9      12 ] 1Y4
GND  [ 10     11 ] 2A1
```
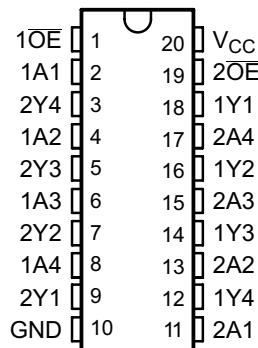
**RGY Package
20-Pin VQFN With Exposed Thermal Pad
Top View**

```
        1OE   V_CC
         1     20
1A1  2            19  2OE
2Y4  3            18  1Y1
1A2  4            17  2A4
2Y3  5            16  1Y2
1A3  6            15  2A3
2Y2  7            14  1Y3
1A4  8            13  2A2
2Y1  9            12  1Y4
        10    11
        GND   2A1
```
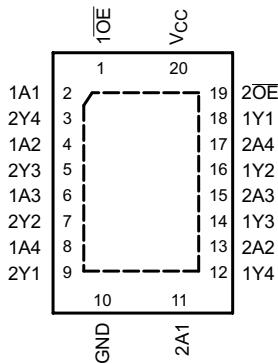
**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 1A1 | 2 | I | Input |
| 1A2 | 4 | I | Input |
| 1A3 | 6 | I | Input |
| 1A4 | 8 | I | Input |
| 1OE | 1 | I | Output enable |
| 1Y1 | 18 | O | Output |
| 1Y2 | 16 | O | Output |
| 1Y3 | 14 | O | Output |
| 1Y4 | 12 | O | Output |
| 2A1 | 11 | I | Input |
| 2A2 | 13 | I | Input |
| 2A3 | 15 | I | Input |
| 2A4 | 17 | I | Input |
| 2OE | 19 | I | Output enable |
| 2Y1 | 9 | O | Output |
| 2Y2 | 7 | O | Output |
| 2Y3 | 5 | O | Output |
| 2Y4 | 3 | O | Output |
| GND | 10 | — | Ground |
| V_CC | 20 | — | Power pin |

**TEXAS INSTRUMENTS**

**SN74LV244A**

SCLS383N – SEPTEMBER 1997 – REVISED OCTOBER 2015

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

|   |   |   | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5 | 7 | V |
| $V_I$ | Input voltage [2] | | −0.5 | 7 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state [2] | | −0.5 | 7 | V |
| $V_O$ | Output voltage [2] [3] | | −0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I < 0$ | | −20 | mA |
| $I_{OK}$ | Output clamp current | $V_O < 0$ | | −50 | mA |
| $I_O$ | Continuous output current | $V_O = 0$ to $V_{CC}$ | | ±35 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±70 | mA |
| $T_j$ | Junction temperature | | −65 | 150 | °C |
| $T_{stg}$ | Storage temperature | | −65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5-V maximum.

## 6.2 ESD Ratings

|   |   |   | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1] | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 [2] | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Product Folder Links: *SN74LV244A*

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | $V_{CC} \times 0.7$ | | |
| | | $V_{CC}$ = 3 V to 3.6 V | $V_{CC} \times 0.7$ | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | $V_{CC} \times 0.7$ | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | $V_{CC} \times 0.3$ | |
| | | $V_{CC}$ = 3 V to 3.6 V | | $V_{CC} \times 0.3$ | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | $V_{CC} \times 0.3$ | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | High or low state | 0 | $V_{CC}$ | V |
| | | 3-state | 0 | 5.5 | |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | −50 | µA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | −2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | −8 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | −16 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | µA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | 8 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 16 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 2.3 V to 2.7 V | | 200 | ns/V |
| | | $V_{CC}$ = 3 V to 3.6 V | | 100 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 20 | |
| $T_A$ | Operating free-air temperature | | −40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

## 6.4 Thermal Information

| | THERMAL METRIC[1] | SN74LV244A | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | DB (SSOP) | DGV (TVSOP) | DW (SOIC) | NS (SO) | PW (TSSOP) | RGY (VQFN) | |
| | | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 94.7 | 115.9 | 79.4 | 76.9 | 102.6 | 34.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 56.7 | 31.1 | 43.8 | 43.4 | 36.7 | 43.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 49.9 | 57.4 | 47.2 | 44.5 | 53.6 | 12.7 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 18.7 | 1.0 | 18.8 | 17.0 | 2.4 | 0.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 49.5 | 56.7 | 46.7 | 44.1 | 53.1 | 12.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | n/a | n/a | n/a | n/a | 7.8 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

**TEXAS INSTRUMENTS**

**SN74LV244A**

SCLS383N –SEPTEMBER 1997–REVISED OCTOBER 2015

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## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | $I_{OH} = -50$ μA | $T_A = -40°C$ to 125°C | 2 V to 5.5 V | $V_{CC} - 0.1$ | | | V |
| | $I_{OH} = -2$ mA | $T_A = -40°C$ to 125°C | 2.3 V | 2 | | | |
| | $I_{OH} = -8$ mA | $T_A = -40°C$ to 125°C | 3 V | 2.48 | | | |
| | $I_{OH} = 16$ mA | $T_A = -40°C$ to 125°C | 4.5 V | 3.8 | | | |
| $V_{OL}$ | $I_{OL} = 50$ μA | $T_A = -40°C$ to 125°C | 2 V to 5.5 V | | | 0.1 | V |
| | $I_{OL} = 2$ mA | $T_A = -40°C$ to 125°C | 2.3 V | | | 0.4 | |
| | $I_{OL} = 8$ mA | $T_A = -40°C$ to 125°C | 3 V | | | 0.44 | |
| | $I_{OL} = 16$ mA | $T_A = -40°C$ to 125°C | 4.5 V | | | 0.55 | |
| $I_I$ | $V_I = 5.5$ V or GND | $T_A = -40°C$ to 125°C | 0 to 5.5 V | | | ±1 | μA |
| $I_{OZ}$ | $V_O = V_{CC}$ or GND | $T_A = -40°C$ to 125°C | 5.5 V | | | ±5 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O = 0$ | $T_A = -40°C$ to 125°C | 5.5 V | | | 20 | μA |
| $I_{off}$ | $V_I$ or $V_O = 0$ to 5.5 V | $T_A = -40°C$ to 125°C | 0 | | | 5 | μA |
| $C_i$ | $V_I = V_{CC}$ or GND | $T_A = -40°C$ to 125°C | 3.3 V | | 2.3 | | pF |

## 6.6 Noise Characteristics

$V_{CC} = 3.3$ V, $C_L = 50$ pF, $T_A = 25°C$ [1]

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{OL(P)}$ | Quiet output, maximum dynamic | | 0.55 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic | | −0.5 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic | | 2.9 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2.31 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.99 | V |

(1)   Characteristics are for surface-mount packages only.

## 6.7 Operating Characteristics

$T_A = 25°C$

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L = 50$ pF, f = 10 MHz | 3.3 V | 14 | pF |
| | | | 5 V | 16 | |

## 6.8 Switching Characteristics: $V_{CC} = 2.5$ V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{pd}$ | A | Y | $C_L = 15$ pF | $T_A = 25°C$ | | 7.5 [1] | 12.5 [1] | ns |
| | | | | $T_A = -40°C$ to 125°C | 1 | | 15 | |
| $t_{en}$ | $\overline{OE}$ | Y | $C_L = 15$ pF | $T_A = 25°C$ | | 8.9 [1] | 14.6 [1] | ns |
| | | | | $T_A = -40°C$ to 125°C | 1 | | 17 | |
| $t_{dis}$ | $\overline{OE}$ | Y | $C_L = 15$ pF | $T_A = 25°C$ | | 9.1 [1] | 14.1 [1] | ns |
| | | | | $T_A = -40°C$ to 125°C | 1 | | 16 | |
| $t_{pd}$ | A | Y | $C_L = 50$ pF | $T_A = 25°C$ | | 9.5 [1] | 15.3 | ns |
| | | | | $T_A = -40°C$ to 125°C | 1 | | 18 | |
| $t_{en}$ | $\overline{OE}$ | Y | $C_L = 50$ pF | $T_A = 25°C$ | | 10.8 | 17.8 | ns |
| | | | | $T_A = -40°C$ to 125°C | 1 | | 21 | |

(1)   On products compliant to MIL-PRF-38535, this parameter is not production tested.

Product Folder Links: *SN74LV244A*

**TEXAS INSTRUMENTS**

**SN74LV244A**

## Switching Characteristics: $V_{CC}$ = 2.5 V ± 0.2 V (continued)

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{dis}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | $T_A$ = 25°C | | 13.4 | 19.2 | ns |
| | | | | $T_A$ = −40°C to 125°C | 1 | | 21 | |
| $t_{sk(o)}$ | | | $C_L$ = 50 pF | $T_A$ = 25°C | | | 2 | ns |
| | | | | $T_A$ = −40°C to 125°C | | | 2 | |

## 6.9 Switching Characteristics: $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{pd}$ | A | Y | $C_L$ = 15 pF | $T_A$ = 25°C | | 5.4[1] | 8.4[1] | ns |
| | | | | $T_A$ = −40°C to 125°C | 1 | | 10 | |
| $t_{en}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | $T_A$ = 25°C | | 6.3[1] | 10.6[1] | ns |
| | | | | $T_A$ = −40°C to 125°C | 1 | | 12.5 | |
| $t_{dis}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | $T_A$ = 25°C | | 7.6[1] | 11.7[1] | ns |
| | | | | $T_A$ = −40°C to 125°C | 1 | | 13 | |
| $t_{pd}$ | A | Y | $C_L$ = 50 pF | $T_A$ = 25°C | | 6.8 | 11.9 | ns |
| | | | | $T_A$ = −40°C to 125°C | 1 | | 13.5 | |
| $t_{en}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | $T_A$ = 25°C | | 7.8 | 14.1 | ns |
| | | | | $T_A$ = −40°C to 125°C | 1 | | 16 | |
| $t_{dis}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | $T_A$ = 25°C | | 11 | 16 | ns |
| | | | | $T_A$ = −40°C to 125°C | 1 | | 18 | |
| $t_{sk(o)}$ | | | $C_L$ = 50 pF | $T_A$ = 25°C | | | 1.5 | ns |
| | | | | $T_A$ = −40°C to 125°C | | | 1.5 | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 6.10 Switching Characteristics: $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{pd}$ | A | Y | $C_L$ = 15 pF | $T_A$ = 25°C | | 3.9[1] | 5.5[1] | ns |
| | | | | $T_A$ = −40°C to 125°C | 1 | | 6.5 | |
| $t_{en}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | $T_A$ = 25°C | | 4.5[1] | 7.3[1] | ns |
| | | | | $T_A$ = −40°C to 125°C | 1 | | 8.5 | |
| $t_{dis}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | $T_A$ = 25°C | | 6.5[1] | 12.2[1] | ns |
| | | | | $T_A$ = −40°C to 125°C | 1 | | 13.5 | |
| $t_{pd}$ | A | Y | $C_L$ = 50 pF | $T_A$ = 25°C | | 4.9 | 7.5 | ns |
| | | | | $T_A$ = −40°C to 125°C | 1 | | 8.5 | |
| $t_{en}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | $T_A$ = 25°C | | 5.6 | 9.3 | ns |
| | | | | $T_A$ = −40°C to 125°C | 1 | | 10.5 | |
| $t_{dis}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | $T_A$ = 25°C | | 8.8 | 14.2 | ns |
| | | | | $T_A$ = −40°C to 125°C | 1 | | 15.5 | |
| $t_{sk(o)}$ | | | | $T_A$ = 25°C | | | 1 | ns |
| | | | | $T_A$ = −40°C to 85°C | | | 1 | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

**TEXAS INSTRUMENTS**

**SN74LV244A**

SCLS383N –SEPTEMBER 1997–REVISED OCTOBER 2015

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## 6.11 Typical Characteristics
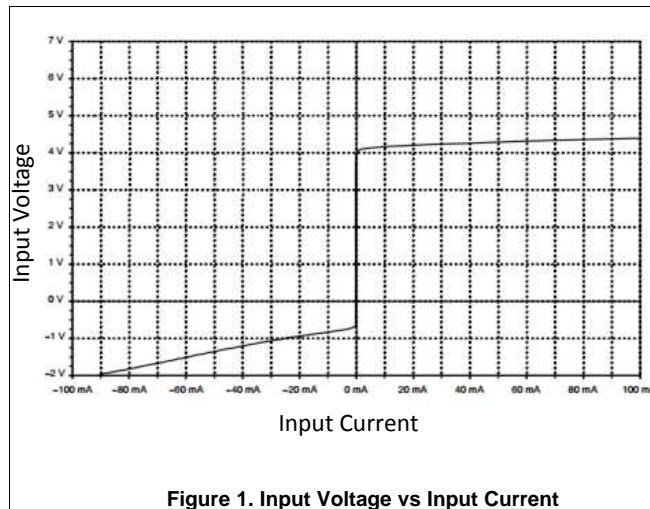


**Figure 1. Input Voltage vs Input Current**
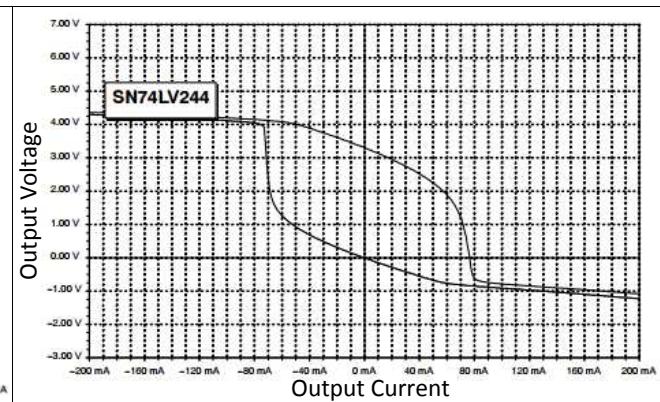


**Figure 2. Output Voltage vs Output Current**

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**SN74LV244A**
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## 7  Parameter Measurement Information
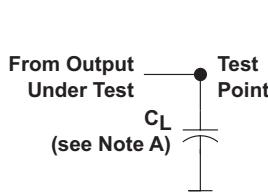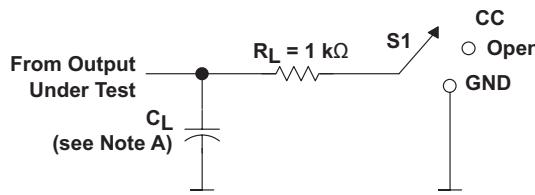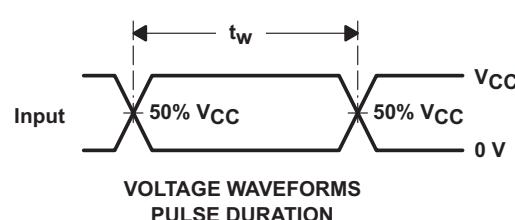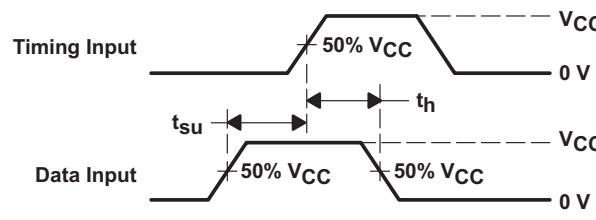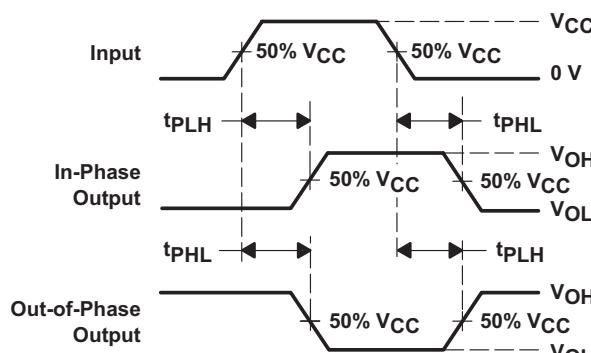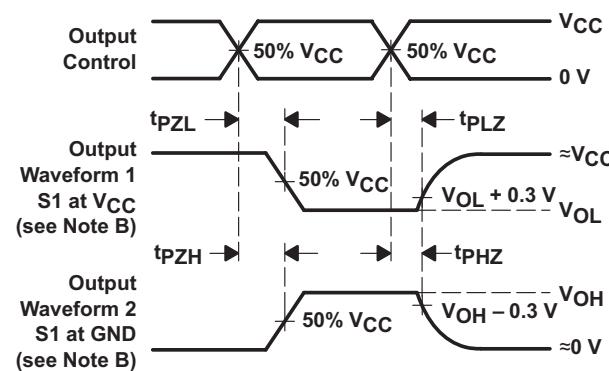


A.  $C_L$ includes probe and jig capacitance.

B.  Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
    Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C.  All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.

D.  The outputs are measured one at a time, with one input transition per measurement.

E.  $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.

F.  $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.

G.  $t_{PHL}$ and $t_{PLH}$ are the same as $t_{pd}$.

H.  All parameters and waveforms are not applicable to all devices.

**Figure 3.  Load Circuit and Voltage Waveforms**

**TEXAS INSTRUMENTS**

**SN74LV244A**

SCLS383N – SEPTEMBER 1997 – REVISED OCTOBER 2015

www.ti.com

# 8 Detailed Description

## 8.1 Overview

The SN74LV244 devices are octal buffers grouped in fours, with each group having its own enable pin. The LV family supports high current drive of about 16 mA, thus making it suitable for driving digital signals over longer board lengths. This device is generally used to buffer or incorporate delays between the signals between two microcontroller or peripheral devices.

## 8.2 Functional Block Diagram
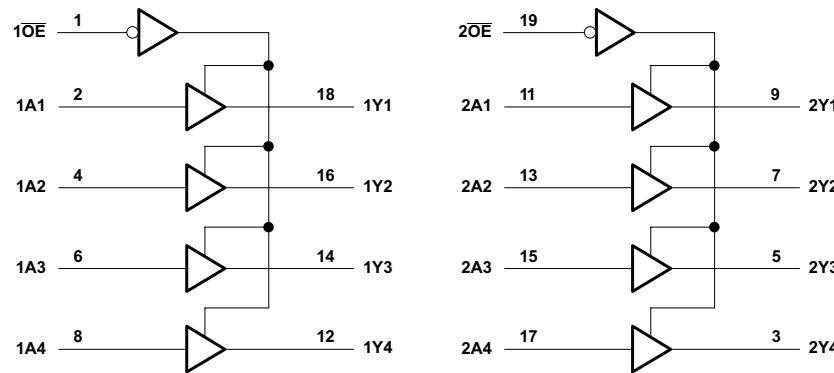


## 8.3 Feature Description

The SN74LV244A, a part of LV family, can work over a wide voltage range from 2 V to 5.5 V. The device features a very low propagation delay of about 6.5 ns when enabled for 5-V $V_{CC}$, which allows the device to be used for high-speed applications. The device supports a partial-power-down mode for low quiescent current application, thus making it the buffer of choice in power-efficient circuits. The $I_{off}$ circuitry also disables the outputs, preventing damaging current backflow through the devices when they are powered down.

## 8.4 Device Functional Modes

The SN74LV244A devices are organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state. To ensure the high-impedance state during power up or power down, $\overline{OE}$ must be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**Table 1. Function Table**

| INPUTS | | OUTPUTS |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | L | L |
| L | H | H |
| H | X | Z |

Product Folder Links: *SN74LV244A*

## 9    Application and Implementation

**NOTE**
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1    Application Information

The SN74LV244A device can be used as an 8-channel buffer to drive signals from one controller to another device. Buffers are typically used for signals running on long traces on printed circuit boards or going through connectors linking two printed circuit boards together. Buffers are also used to create delay between the lines to match the edges of two clock or data signals. The high-current capability of the SN74LV244A device also allows a controller to drive LEDs up to 16 mA.

### 9.2    Typical Application
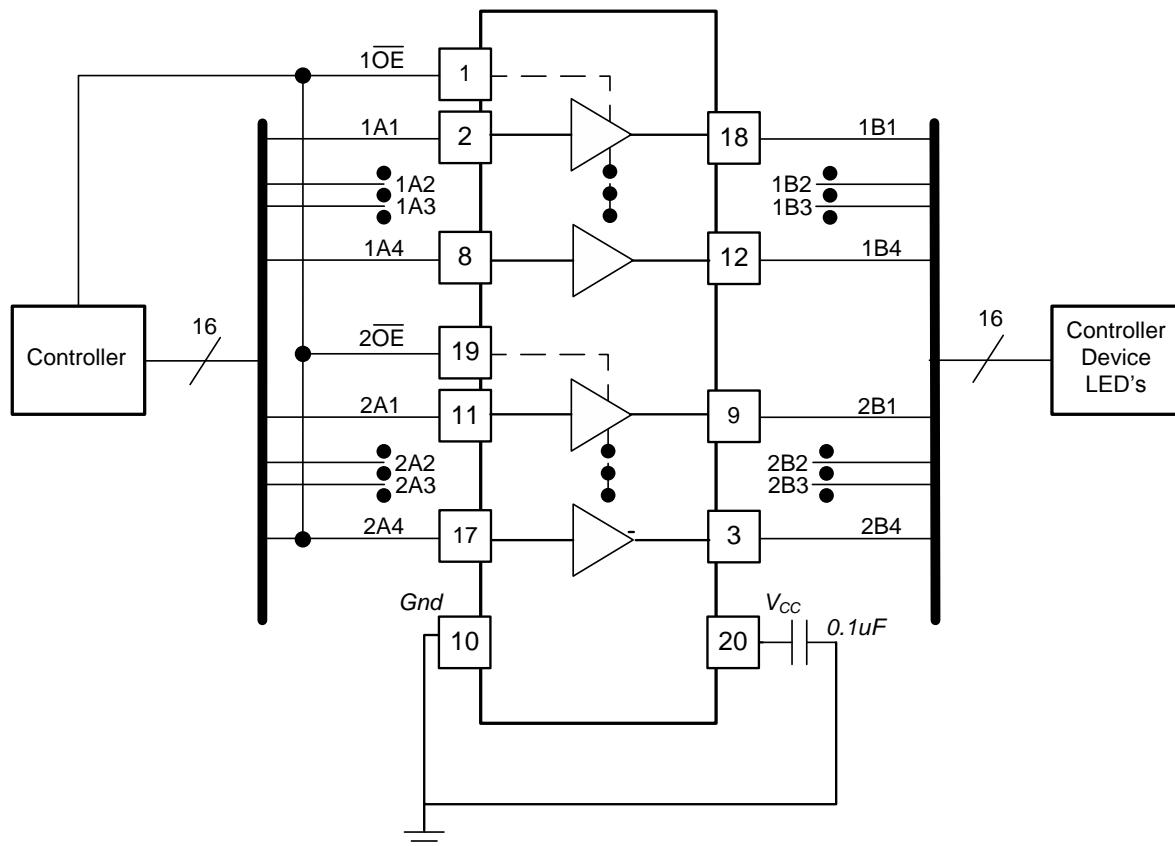


**Figure 4.  Typical Application Diagram**

Product Folder Links: *SN74LV244A*

## Typical Application (continued)

### 9.2.1 Design Requirements

A 0.1-µF bypass capacitor must be placed between each $V_{CC}$ pin and GND. For best results, each capacitor must be placed as close as possible to the SN74LV244A device.

### 9.2.2 Detailed Design Procedure

1. Recommended input conditions:
   – For specified high and low levels, see $V_{IH}$ and $V_{IL}$ in *Recommended Operating Conditions*
   – Inputs and outputs are overvoltage tolerant, which allows them to go as high as 5.5 V at any valid $V_{CC}$
2. Recommended output conditions:
   – Load currents must not exceed limits as mentioned in Recommended Operating Conditions
3. Frequency selection criterion:
   – Added trace resistance or capacitance can reduce maximum frequency capability; use layout practices as directed in *Layout Guidelines*

### 9.2.3 Application Curve
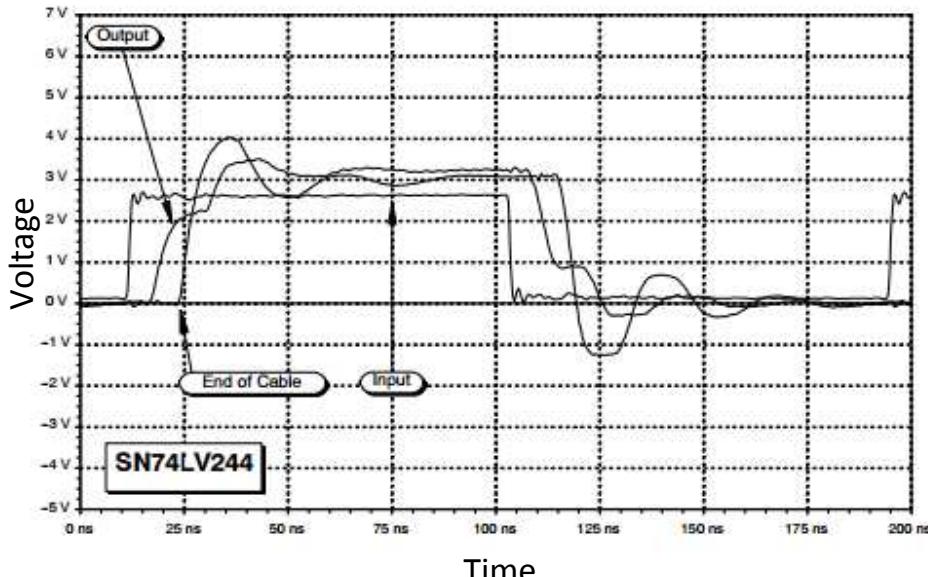


**Figure 5. SN74LV244A Transient response**

# 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply-voltage rating listed in the *Absolute Maximum Ratings* table.

Each $V_{CC}$ terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF bypass capacitor is recommended. If multiple pins are labeled $V_{CC}$, then a 0.01-µF or 0.022-µF capacitor is recommended for each $V_{CC}$ because the $V_{CC}$ pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example $V_{CC}$ and $V_{DD}$, a 0.1-µF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 µF and 1 µF are commonly used in parallel. For best results, the bypass capacitor must be installed as close as possible to the power terminal.

# 11 Layout

## 11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace, which results in the reflection. Not all PCB traces can be straight; therefore, some traces must turn corners. Figure 6 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

## 11.2 Layout Example
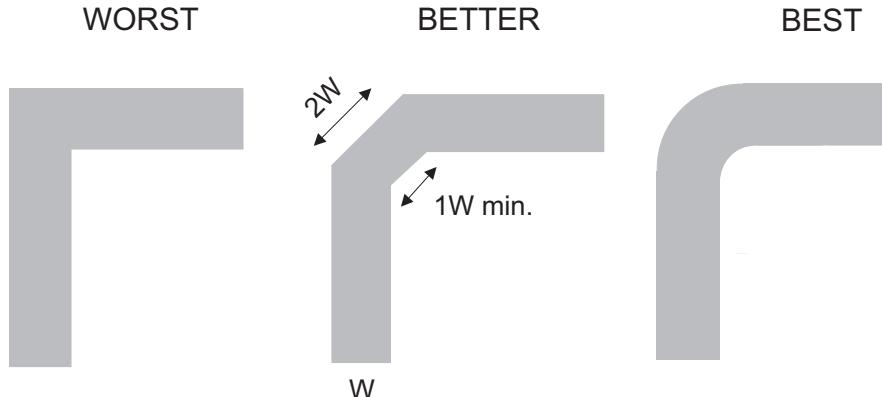


**Figure 6. Trace Example**

Product Folder Links: *SN74LV244A*

**TEXAS INSTRUMENTS**

**SN74LV244A**
SCLS383N – SEPTEMBER 1997 – REVISED OCTOBER 2015

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## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation, see the following:
*Implications of Slow or Floating CMOS Inputs*, SCBA004

### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.5 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: *SN74LV244A*

**PACKAGE OPTION ADDENDUM**

www.ti.com

10-Jun-2014

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV244ADBLE | OBSOLETE | SSOP | DB | 20 | | TBD | Call TI | Call TI | -40 to 125 | | |
| SN74LV244ADBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV244A | Samples |
| SN74LV244ADBRE4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV244A | Samples |
| SN74LV244ADBRG4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV244A | Samples |
| SN74LV244ADGVR | ACTIVE | TVSOP | DGV | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV244A | Samples |
| SN74LV244ADW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV244A | Samples |
| SN74LV244ADWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV244A | Samples |
| SN74LV244ADWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV244A | Samples |
| SN74LV244ADWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV244A | Samples |
| SN74LV244ADWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV244A | Samples |
| SN74LV244ANSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 74LV244A | Samples |
| SN74LV244APW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV244A | Samples |
| SN74LV244APWG4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV244A | Samples |
| SN74LV244APWLE | OBSOLETE | TSSOP | PW | 20 | | TBD | Call TI | Call TI | -40 to 125 | | |
| SN74LV244APWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | CU SN | Level-1-260C-UNLIM | -40 to 125 | LV244A | Samples |
| SN74LV244APWRE4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV244A | Samples |
| SN74LV244APWRG3 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LV244A | Samples |
| SN74LV244APWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV244A | Samples |

**PACKAGE OPTION ADDENDUM**

www.ti.com

10-Jun-2014

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV244APWT | ACTIVE | TSSOP | PW | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV244A | Samples |
| SN74LV244ARGYR | ACTIVE | VQFN | RGY | 20 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LV244A | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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10-Jun-2014

**OTHER QUALIFIED VERSIONS OF SN74LV244A :**

• Enhanced Product: SN74LV244A-EP

NOTE: Qualified Version Definitions:

    • Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TEXAS INSTRUMENTS**

# PACKAGE MATERIALS INFORMATION

www.ti.com                                                                                                    27-Dec-2014

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**
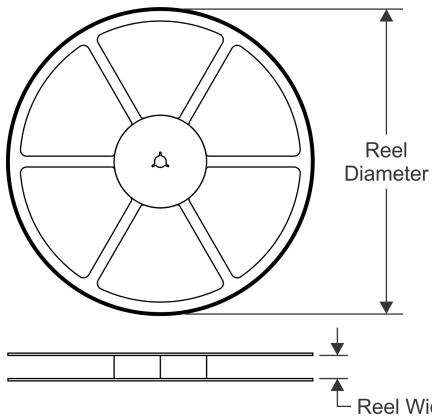


**TAPE DIMENSIONS**
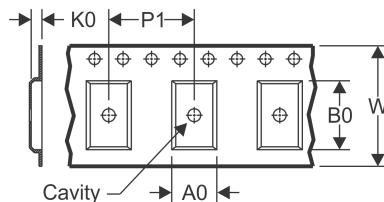


| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**
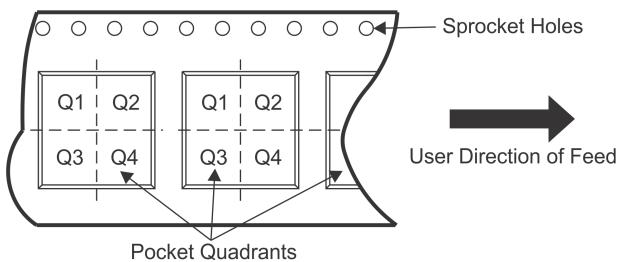


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV244ADBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LV244ADGVR | TVSOP | DGV | 20 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV244ADWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LV244ANSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 9.0 | 13.0 | 2.4 | 4.0 | 24.0 | Q1 |
| SN74LV244APWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LV244APWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LV244APWRG3 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LV244APWT | TSSOP | PW | 20 | 250 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LV244ARGYR | VQFN | RGY | 20 | 3000 | 330.0 | 12.4 | 3.8 | 4.8 | 1.6 | 8.0 | 12.0 | Q1 |

**TEXAS INSTRUMENTS**

# PACKAGE MATERIALS INFORMATION

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27-Dec-2014

**TAPE AND REEL BOX  DIMENSIONS**
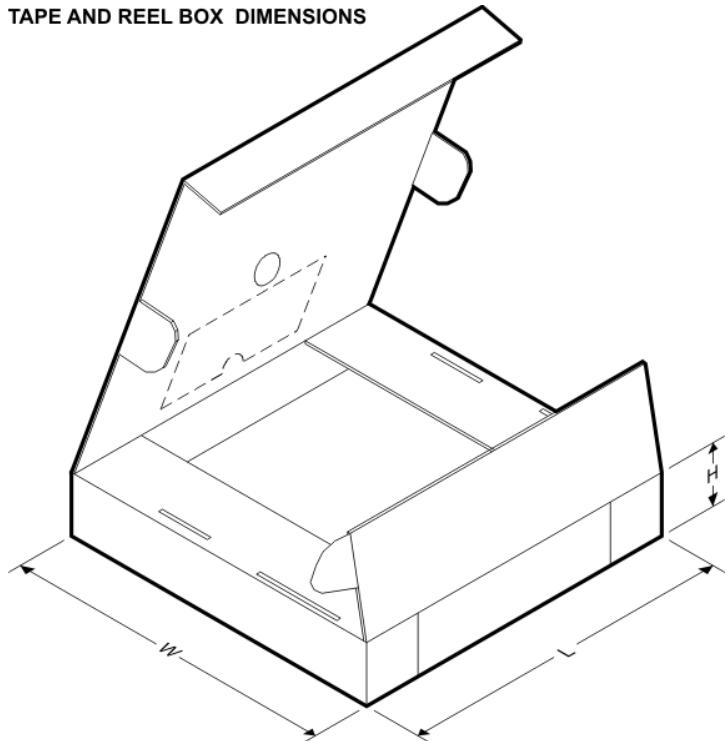


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LV244ADBR | SSOP | DB | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LV244ADGVR | TVSOP | DGV | 20 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LV244ADWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LV244ANSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LV244APWR | TSSOP | PW | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LV244APWR | TSSOP | PW | 20 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74LV244APWRG3 | TSSOP | PW | 20 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74LV244APWT | TSSOP | PW | 20 | 250 | 367.0 | 367.0 | 38.0 |
| SN74LV244ARGYR | VQFN | RGY | 20 | 3000 | 367.0 | 367.0 | 35.0 |

## MECHANICAL DATA

MPDS006C – FEBRUARY 1996 – REVISED AUGUST 2000

**DGV (R-PDSO-G**)**                                                      **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**
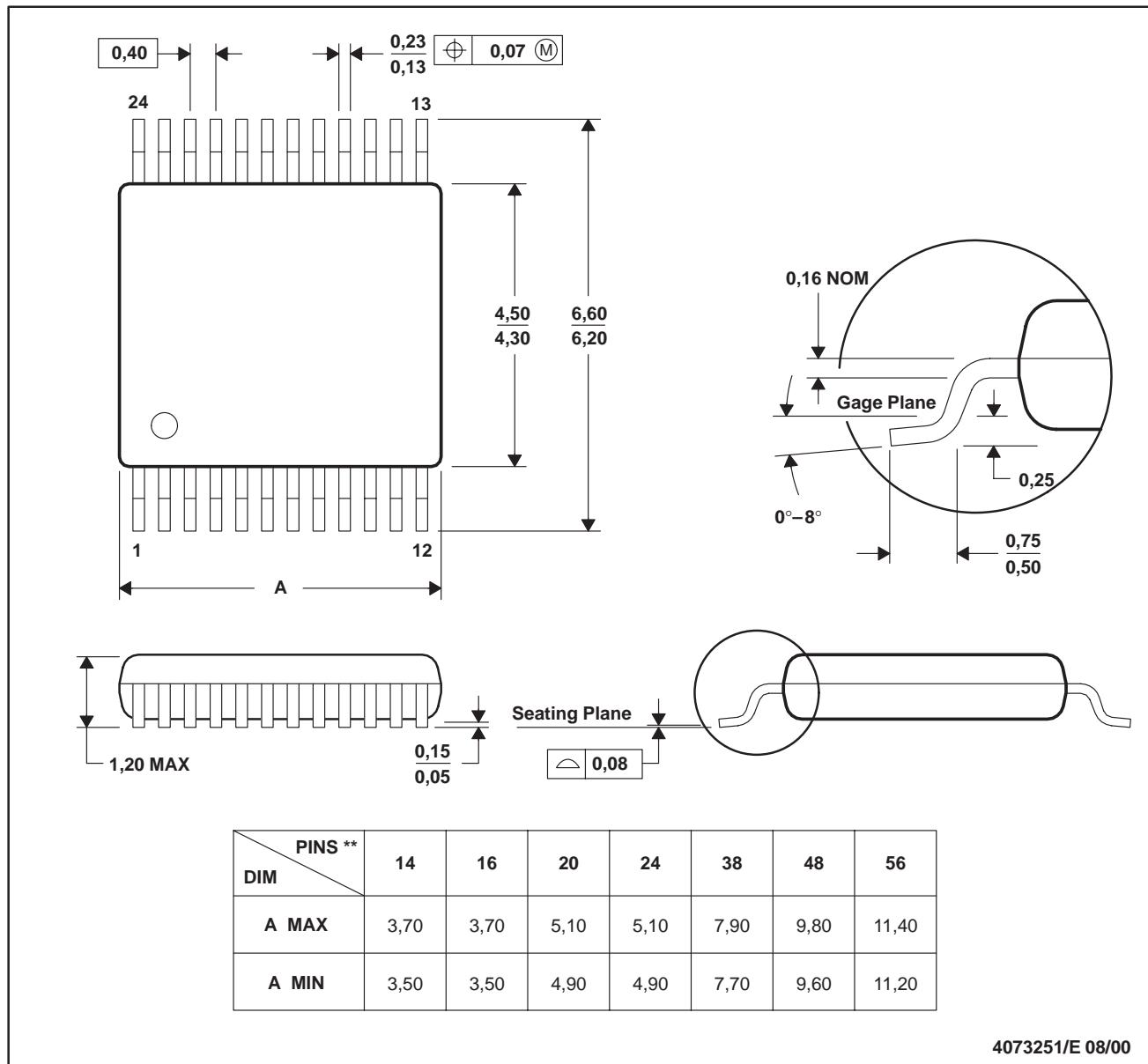
| PINS ** DIM | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC:  24/48 Pins – MO-153
                        14/16/20/56 Pins – MO-194

**TEXAS INSTRUMENTS**
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

**PACKAGE OUTLINE**

## DW0020A

**SOIC - 2.65 mm max height**

SOIC



10.63 / 9.97 TYP

PIN 1 ID AREA

A

1

18X 1.27

20

13.0 / 12.6 NOTE 3

2X 11.43

10

11

B

7.6 / 7.4 NOTE 4

20X 0.51 / 0.31

⌖ 0.25 Ⓜ C A B

C

SEATING PLANE

△ 0.1 C

2.65 MAX

SEE DETAIL A

0.33 / 0.10 TYP

0.25
GAGE PLANE

0° - 8°

1.27 / 0.40

0.3 / 0.1

**DETAIL A**
TYPICAL
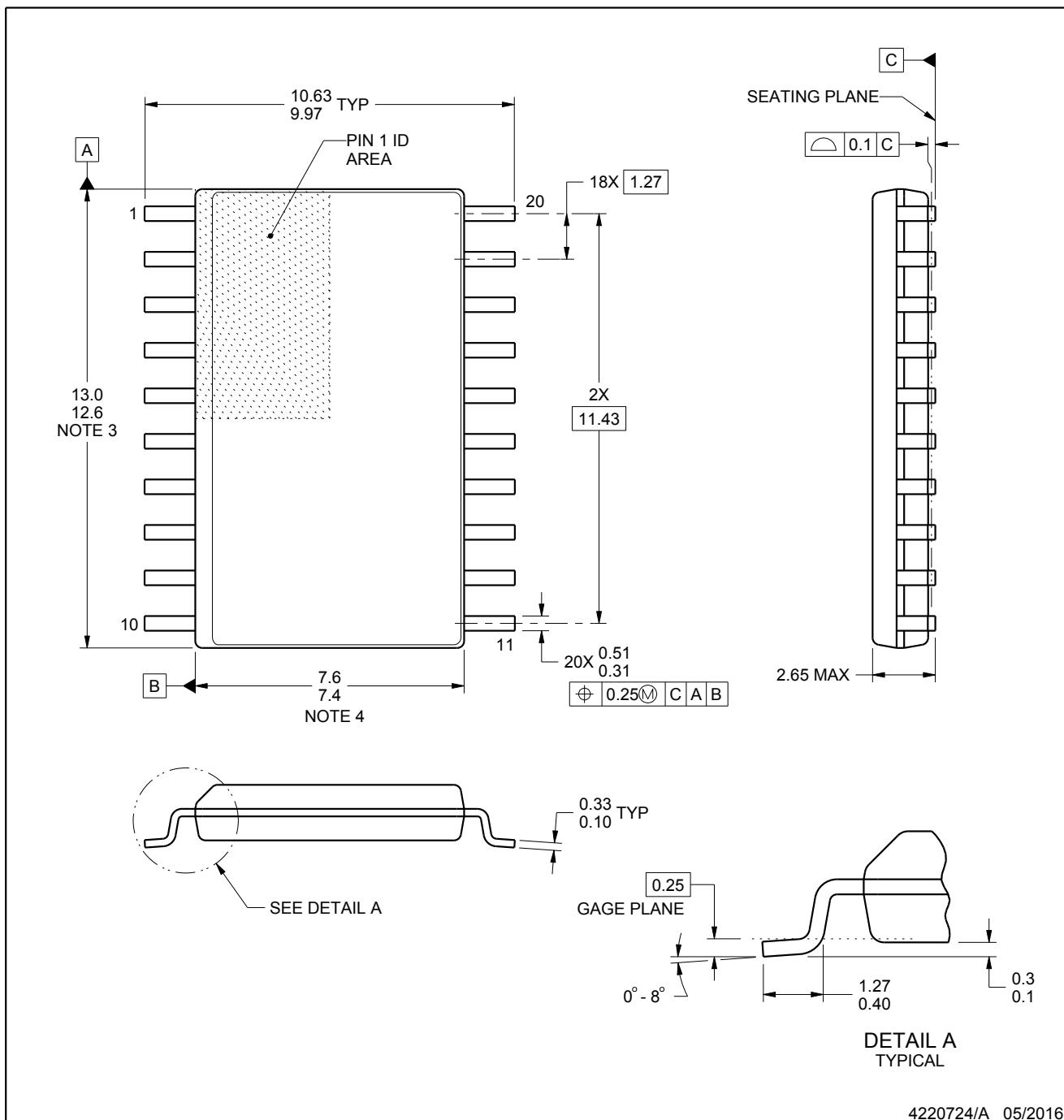
4220724/A   05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

**TEXAS INSTRUMENTS**
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# EXAMPLE BOARD LAYOUT

## DW0020A

### SOIC - 2.65 mm max height

SOIC
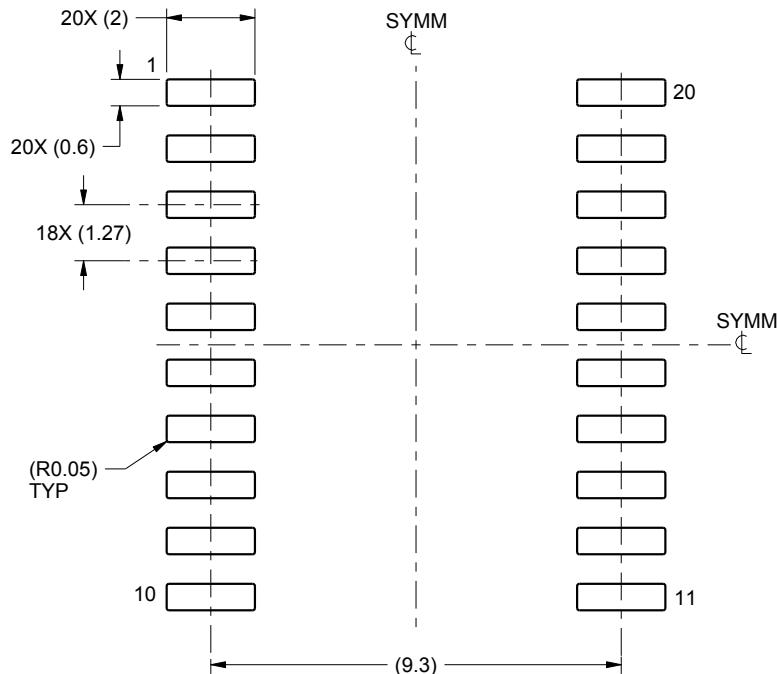


LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK OPENING

METAL

0.07 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MIN
ALL AROUND

SOLDER MASK
DEFINED
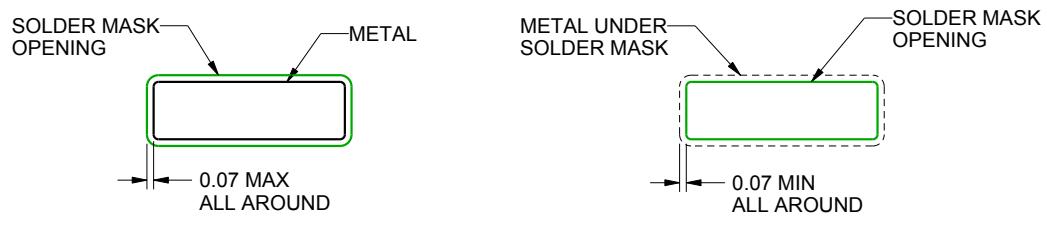
SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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# EXAMPLE STENCIL DESIGN

## DW0020A

### SOIC - 2.65 mm max height

SOIC
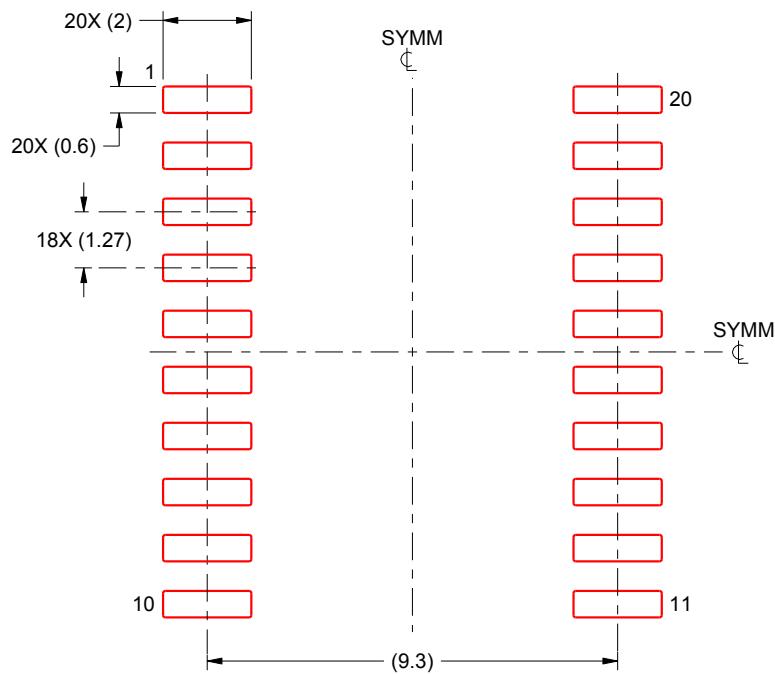


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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**MECHANICAL DATA**

PW (R−PDSO−G20)                                        PLASTIC SMALL OUTLINE
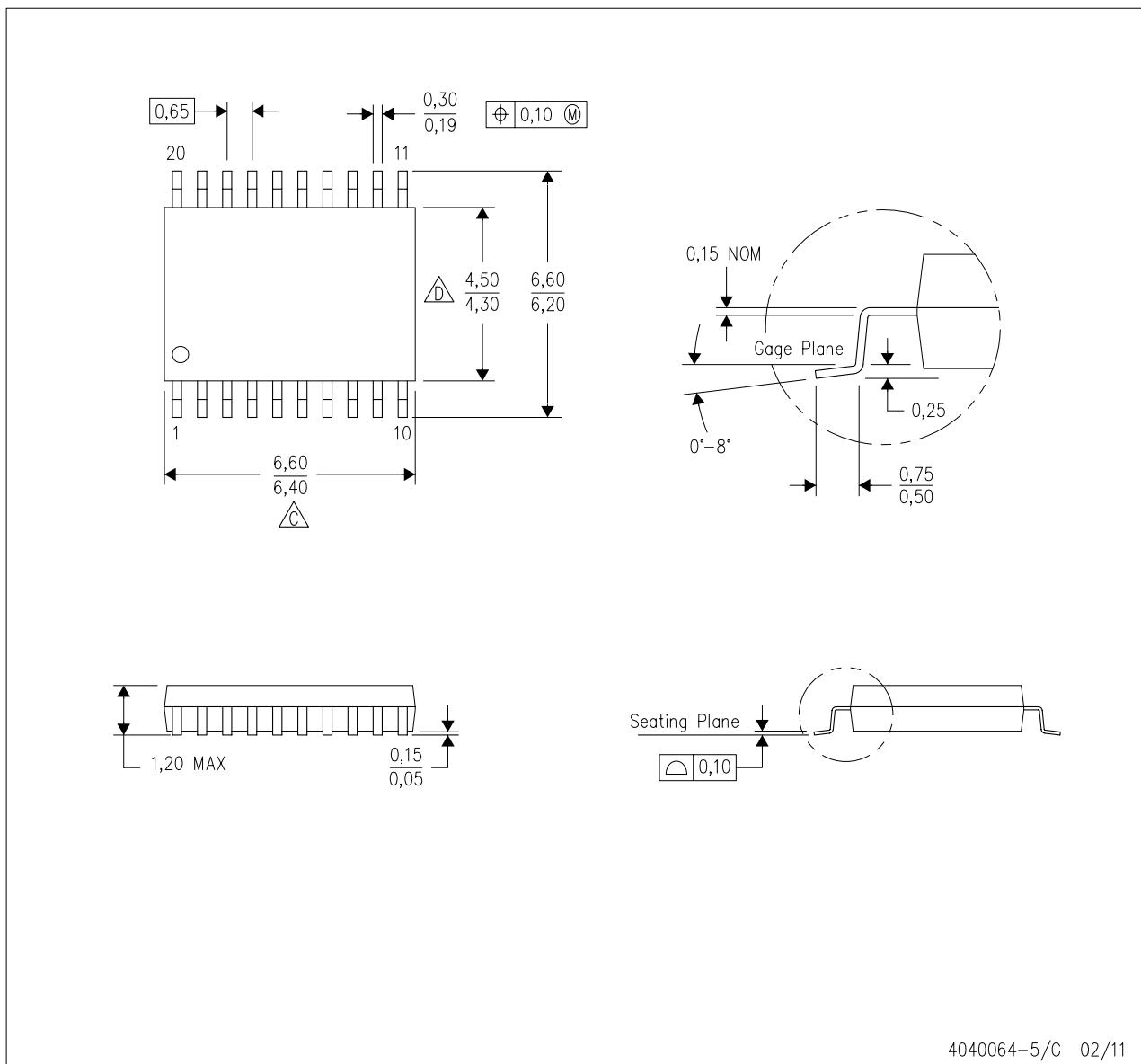


4040064−5/G   02/11

NOTES:   A.   All linear dimensions are in millimeters.  Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
              not exceed 0,15 each side.
         D.   Body width does not include interlead flash.  Interlead flash shall not exceed 0,25 each side.
         E.   Falls within JEDEC MO−153

**LAND PATTERN DATA**

PW (R-PDSO-G20)                    PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).

18x0,65

20x0,25

5,6

5,6

1,55

18x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

0,3

1,6

Pad Geometry

0,07
All Around
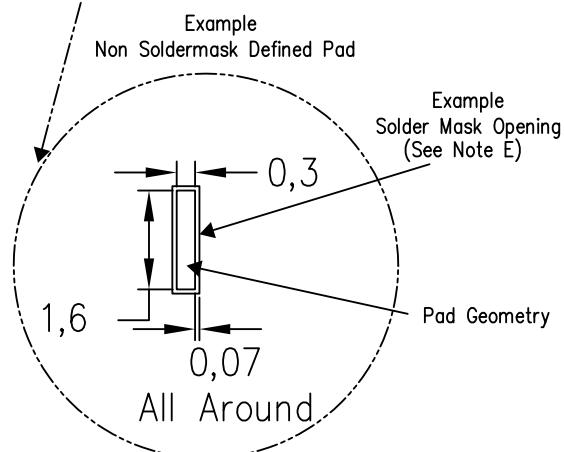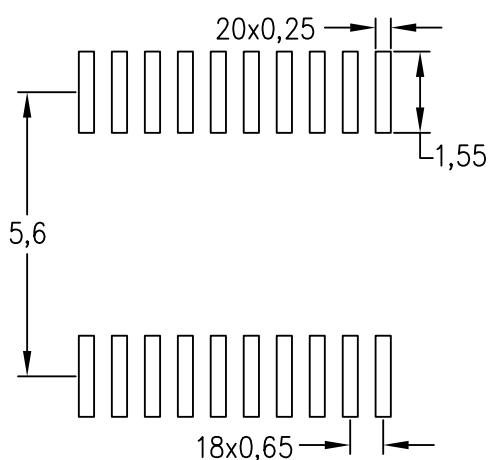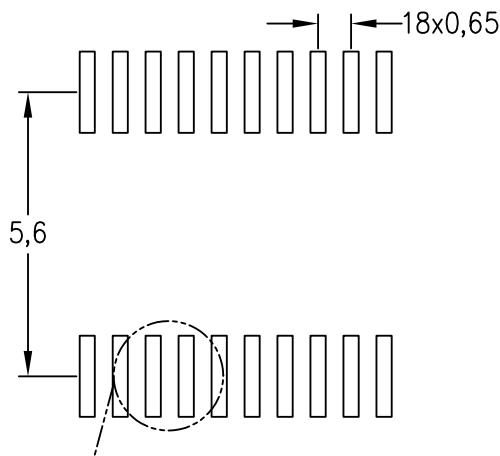
4211284-5/G   08/15

NOTES:   A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC–7351 is recommended for alternate design.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
         E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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# MECHANICAL DATA

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

## DB (R-PDSO-G**)                                    PLASTIC SMALL-OUTLINE
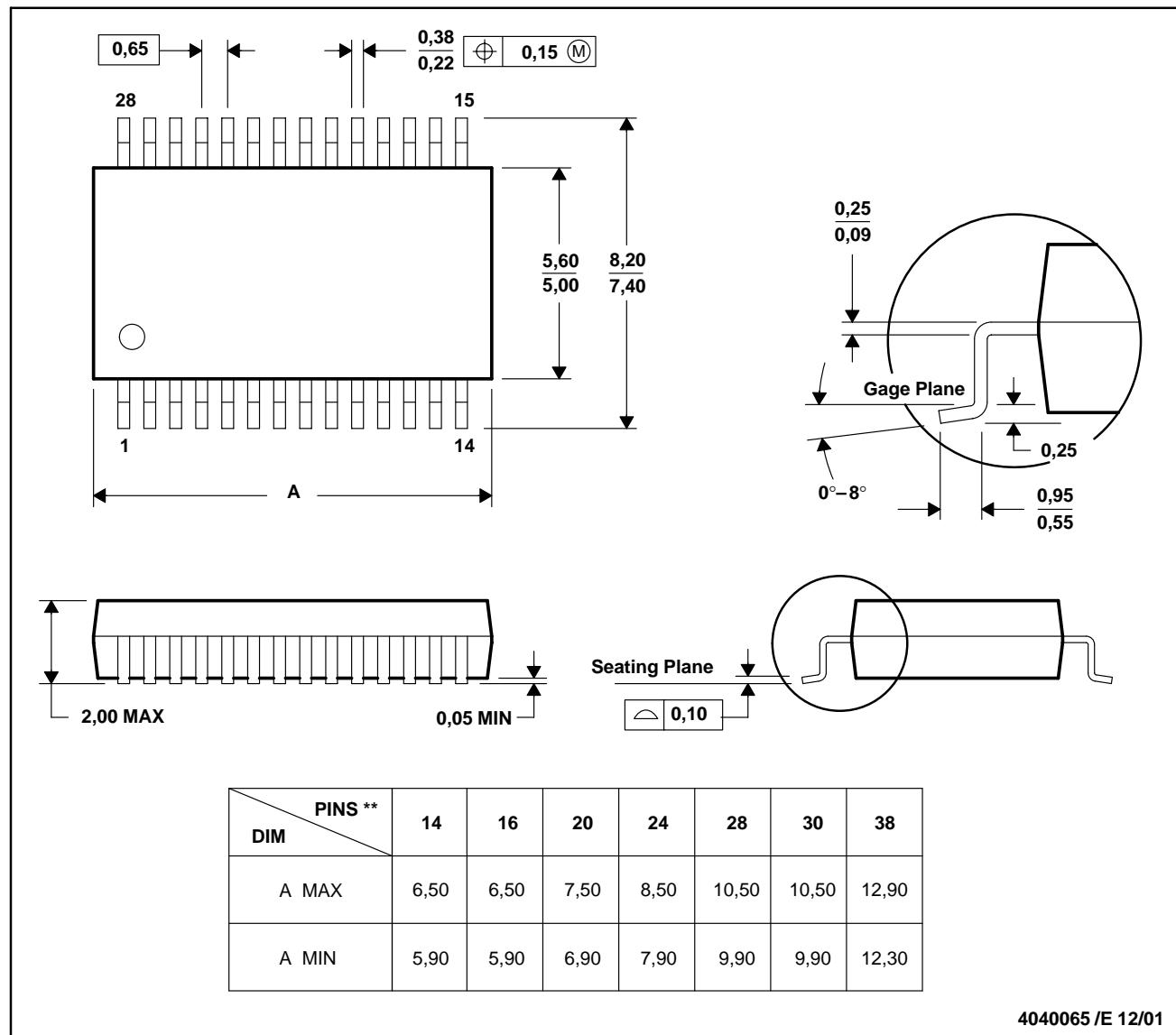
**28 PINS SHOWN**



| | PINS ** | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|---|
| DIM | | | | | | | | |
| A MAX | | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

4040065 /E 12/01

NOTES:  A.  All linear dimensions are in millimeters.
        B.  This drawing is subject to change without notice.
        C.  Body dimensions do not include mold flash or protrusion not to exceed 0,15.
        D.  Falls within JEDEC MO-150

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## MECHANICAL DATA

RGY (R-PVQFN-N20)                    PLASTIC QUAD FLATPACK NO-LEAD



Pin 1 Index Area
Top and Bottom
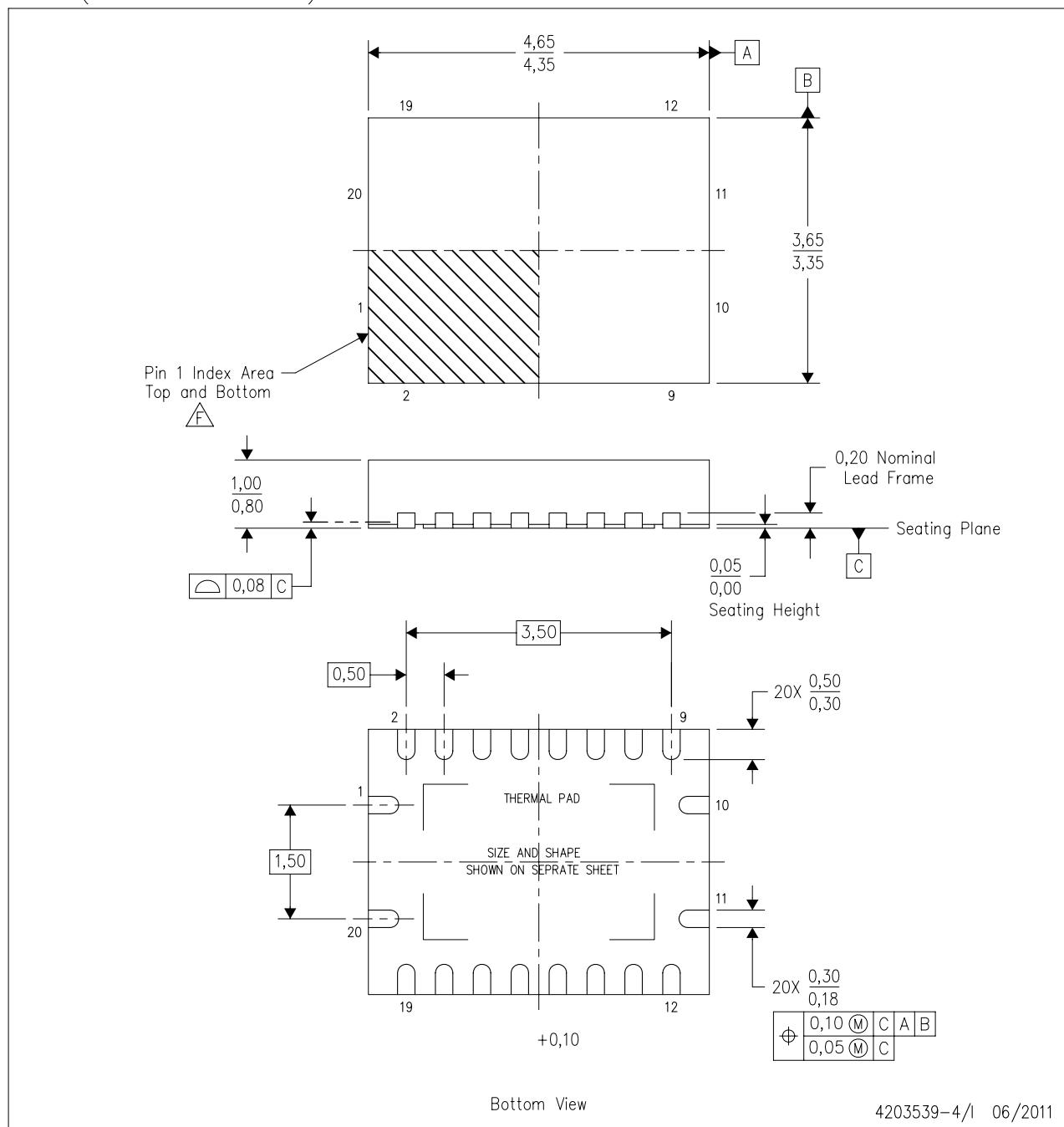
Bottom View

4203539-4/I   06/2011

NOTES:   A.  All linear dimensions are in millimeters.  Dimensioning and tolerancing per ASME Y14.5M-1994.
         B.  This drawing is subject to change without notice.
         C.  QFN (Quad Flatpack No-Lead) package configuration.
         D.  The package thermal pad must be soldered to the board for thermal and mechanical performance.
         E.  See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
         F.  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
             The Pin 1 identifiers are either a molded, marked, or metal feature.
         G.  Package complies to JEDEC MO-241 variation BA.

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## THERMAL PAD MECHANICAL DATA

RGY (R−PVQFN−N20)                    PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.
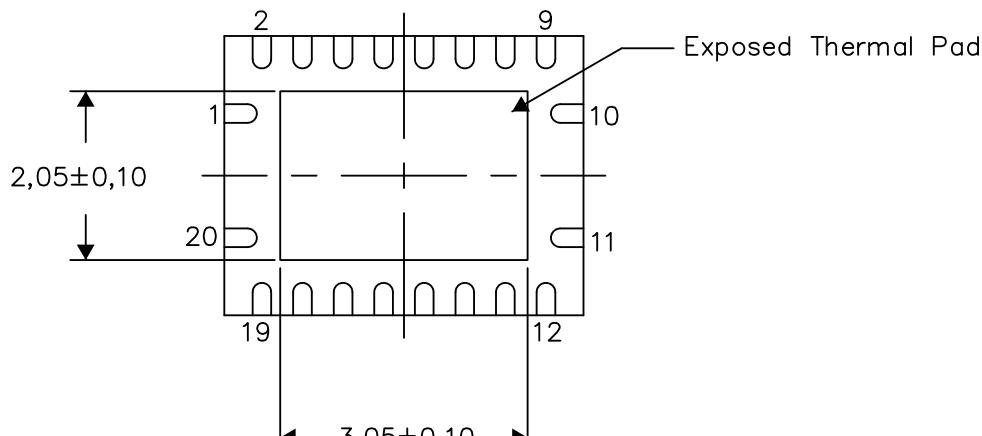


Bottom View

Exposed Thermal Pad Dimensions

4206353−4/P   03/14

NOTE:   All linear dimensions are in millimeters

# LAND PATTERN DATA

## RGY (R–PVQFN–N20)  PLASTIC QUAD FLATPACK NO–LEAD
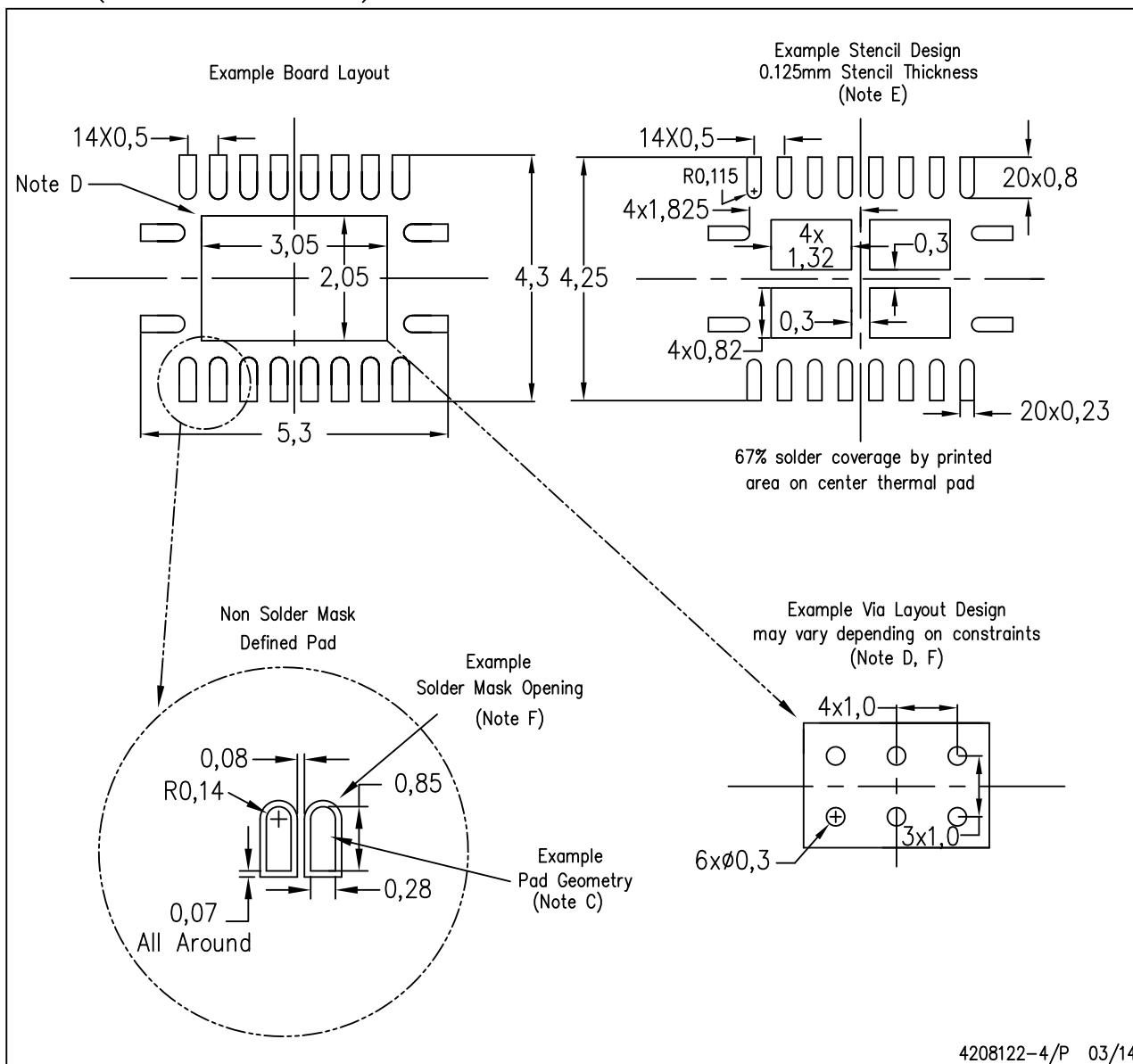
Example Board Layout

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

14X0,5

Note D

3,05

2,05

4,3 4,25

5,3

14X0,5

R0,115

4x1,825

4x
1,32

0,3

0,3

4x0,82

20x0,8

20x0,23

67% solder coverage by printed
area on center thermal pad

Non Solder Mask
Defined Pad

Example
Solder Mask Opening
(Note F)

0,08

R0,14

0,85

0,28

0,07

All Around

Example
Pad Geometry
(Note C)

Example Via Layout Design
may vary depending on constraints
(Note D, F)

4x1,0

6x⌀0,3

3x1,0

4208122–4/P  03/14

NOTES:  A.  All linear dimensions are in millimeters.
B.  This drawing is subject to change without notice.
C.  Publication IPC–7351 is recommended for alternate designs.
D.  This package is designed to be soldered to a thermal pad on the board.  Refer to Application Note, Quad Flat–Pack
QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
for specific thermal information, via requirements, and recommended board layout.
These documents are available at www.ti.com <http://www.ti.com>.
E.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
contact their board assembly site for stencil design recommendations.  Refer to IPC 7525 for stencil design considerations.
F.  Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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# MECHANICAL DATA

**NS (R-PDSO-G**)**                                          **PLASTIC SMALL-OUTLINE PACKAGE**
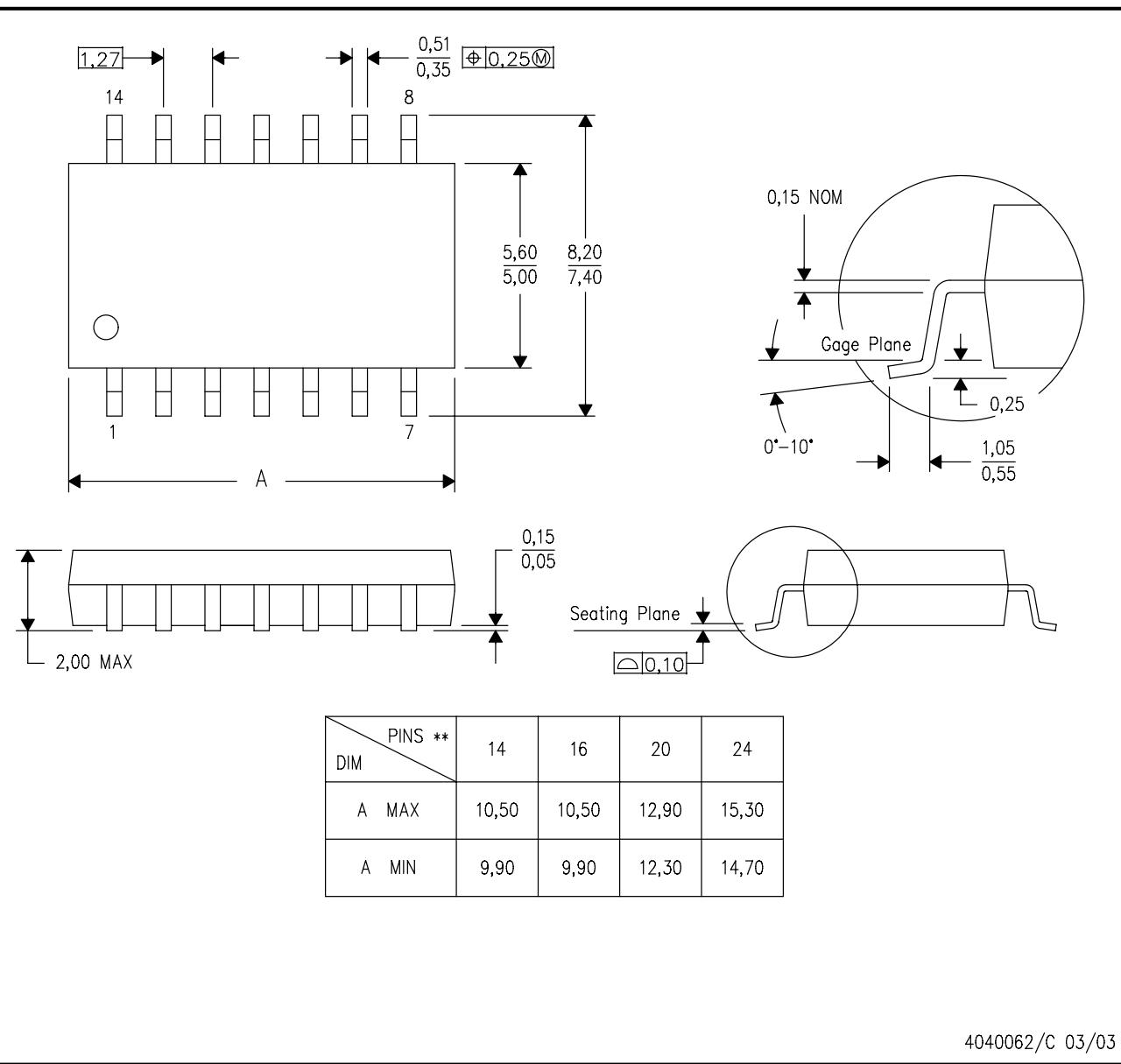
**14-PINS SHOWN**



| PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| DIM |  |  |  |  |
| A  MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A  MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:   A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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